# Stage Number Optimization for Switched Capacitor Power Converters in Micro-Scale Energy Harvesting

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***Abstract*** **– Micro-scale energy harvesting has become an increasingly viable and promising option for powering ultra-low power systems. A power converter is a key component in micro-scale energy harvesting systems. Various design parameters of the power converter, most notably the number of stages in a multi-stage power converter, play a crucial role in determining the amount of electrical power that can be extracted from a micro-scale energy transducer such as a miniature solar cell. Existing stage number optimization techniques for switched capacitor power converters, when used for energy harvesting systems, result in a substantial degradation in the amount of harvested electrical power. To address this problem, this paper proposes a new stage number optimization technique for switched capacitor power converters that maximizes the net harvested power in micro-scale energy harvesting systems. The proposed technique is based on a new figure-of-merit that is well suited for energy-harvesting systems. We have validated the proposed technique through circuit simulations using IBM 65nm technology. Our simulation results demonstrate that the proposed stage number optimization technique results in an increase of 60% - 290% in net harvested power, compared to existing stage number optimization techniques.**

## I. INTRODUCTION

Rapid advances in computing, communication, and integration have resulted in the emergence of a new class of ultra-low power applications. Examples of such systems include implantable biomedical devices [1], smart dust sensors [2], etc. Despite the severe constraint on size, these systems are required to operate for several months to years without battery replacement. As a result, a key challenge in these systems is to conveniently provide the power required for long-lived, maintenance-free operation. Environmental energy harvesting, which refers to the process of generating electrical energy from other energy sources in the immediate vicinity of the system (e.g., solar radiation, thermal gradients, wind currents), is an attractive option and has the potential to result in perpetual system operation [3-4].

Figure 1 shows the block diagram of a micro-scale energy harvesting system. It consists of four main blocks: the energy transducer that converts power from another modality into electrical power, the power converter that conditions the power output from the transducer, the energy buffer that stores harvested energy, and the load system/application that dissipates the harvested power. In these systems, the power converter, which is the focus of this paper, is a crucial component that boosts the output voltage of the energy transducer to a suitable level that enables energy storage in an energy buffer. Since high quality inductors are difficult and/or expensive to fabricate on chip in standard CMOS processes, switched capacitor power converters (SCPCs) are a popular option due to their low cost and ease of on-chip integration.

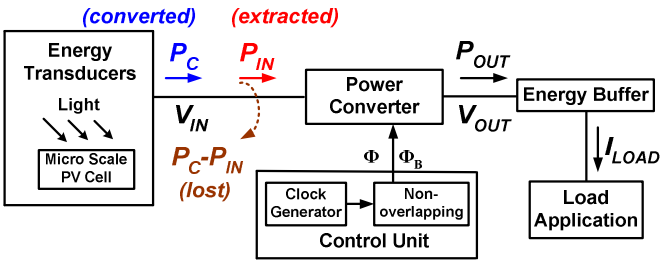


Figure 1. Block diagram of a micro-scale energy harvesting system

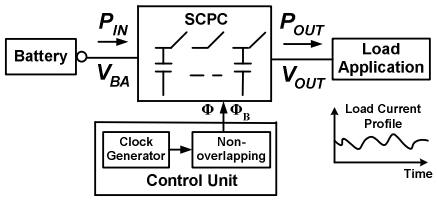


Figure 2. Block diagram of a battery-powered system

Even though SCPCs have been used extensively in battery-powered systems, the design objective in those systems is very different from micro-scale energy harvesting systems. A battery can be thought of as a capacity-limited energy source (i.e., a storehouse of energy with fixed total capacity and some non-idealities). In battery-powered systems, the SCPC translates the power demand of the load system, $P_{OUT}$, into a power demand on the battery, $P_{IN}$, as shown in Figure 2. The objective of the SCPC is to waste as little power as possible in this conversion process, which translates into a design goal of maximizing the power conversion efficiency (i.e., $P_{OUT}/P_{IN}$) of the SCPC. Higher power conversion efficiency implies that less power is lost in the power converter, resulting in more energy available for use by the load system.

However, energy transducers such as photovoltaic cells cannot be viewed as capacity-limited energy sources because they will never run out of energy as long as the environmental energy source (e.g., light) is present. Further, unlike batteries, energy transducers are not capable of storing energy. At any given point in time, a transducer is capable of producing a certain amount of electrical power, shown by $P_C$ in Figure 1. If all of this power cannot be extracted from the transducer immediately, it will be lost forever (unlike in batteries where

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any unused energy remains in the battery and is available for later use). Therefore, in order to reap the maximum benefit from energy harvesting, it is necessary to extract as much power as possible from the transducer at any point in time. Consequently, the goal of an SCPC in energy harvesting systems is to maximize the net harvested power. This means that an SCPC that operates at a lower efficiency but extracts higher net output power from the transducer is preferable to an SCPC that operates at a higher efficiency, but is only able to extract little net output power from the transducer.

The output power capability of an SCPC depends on its implementation technology, input and output voltages, circuit topology, transistor sizing, and the number of stages it has. Of these, the last three factors are fully determined by the circuit design of the SCPC. Prior work has attempted to improve the net output power of SCPCs through topology optimization and transistor sizing [10-12]. In [10], an exponential topology SCPC was proposed to extract energy from ultra-low voltage energy transducers. The authors of [11] proposed a tree topology SCPC that further improves the maximum output power. In [12], various power loss components inside an SCPC were modeled and an analytical design methodology was presented for optimal transistor sizing.

However, the problem of optimizing the number of stages in an SCPC for energy-harvesting systems has not yet been addressed. Existing stage number optimization techniques are targeted at battery-powered systems and attempt to maximize the power conversion efficiency of the SCPC [13-14]. As we will show, these approaches, when used for energy-harvesting systems, result in a substantial degradation in the total harvested power and hence, represent sub-optimal solutions. To address this problem, the focus of this paper is on SCPC stage number optimization for micro-scale energy harvesting systems. This paper makes the following contributions:

- We demonstrate that existing stage number optimization techniques for SCPCs result in a substantial degradation in net harvested power, and therefore, are not suitable for micro-scale energy harvesting systems.
- We propose a new stage number optimization technique for SCPCs that maximizes the net harvested power in micro-scale energy harvesting systems. The optimization is based on maximizing a new figure-of-merit (net output power per unit hardware cost) that is more appropriate for micro-scale energy harvesting systems.
- We have validated the proposed optimization technique by implementing several SCPCs using IBM 65nm technology to quantify the benefits of the proposed approach. Our simulation results demonstrate that SCPCs designed using the proposed stage number optimization technique provide an increase of 60% - 290% in net harvested power, compared to SCPC designs optimized using existing stage number selection approaches.

The remainder of this paper is organized as follows. Section II discusses related work in micro-scale energy transducers and existing SCPC design techniques for maximizing power conversion efficiency. Section III describes the proposed technique for SCPC stage number selection that maximizes the net harvested power from a transducer. Section IV presents various circuit simulation results to validate our proposed technique, while Section V concludes the paper.

## II. Related Work

### A. Micro-Scale Energy Transducers

Environmental energy sources, such as solar radiation, mechanical vibrations, or thermal gradients, are ubiquitous in our surroundings. A variety of micro-scale energy transducers have been developed to convert energy from other modalities into electrical energy [7-8, 15-16]. A non-stacked photovoltaic (PV) cell and a thermo-electric generator were characterized in [11]. Their electrical circuit models, I-V characteristics, and output power were studied. Note that certain energy transducers behave as voltage-limited current sources. For instance, a PV cell's photocurrent is proportional to the light intensity, while its open circuit voltage varies only slightly with changes in light intensity. This significantly increases the difficulty of efficiently extracting and transferring power from very low voltage energy transducers.

### B. Existing Stage Number Optimization Techniques

The authors of [13] proposed a methodology to design an SCPC with maximum power conversion efficiency (i.e., maximum $P_{OUT}/P_{IN}$). After extensive modeling and analysis, the authors derived the optimal number of stages ($N_{OP}$) for the SCPC as:

$$N_{OP} = (1+\sqrt{\frac{\alpha}{1+\alpha}})(\frac{V_{OUT}}{V_{IN}}-1) \quad (1)$$

where $\alpha$ is a technology-dependent parameter and is defined as the ratio of the parasitic capacitance of a stage capacitor to the stage capacitance itself. $V_{IN}$ and $V_{OUT}$ are the input and output voltages of the SCPC, respectively.

Another technique for optimizing the design of an SCPC with only capacitive loads was presented in [14]. The number of stages to obtain maximum power conversion efficiency was estimated as:

$$N_{OP} = \frac{1+4\alpha}{1+3\alpha}(\frac{V_{OUT}}{V_{IN}}-1) \quad (2)$$

Since the value of $\alpha$ is usually very small, expressions (1) and (2) can both be approximated as:

$$N_{OP} = \frac{V_{OUT}}{V_{IN}}-1 \quad (3)$$

Taking into account the actual hardware implementation, the optimal number of SCPC stages should be an integer close to the value computed using (3). As discussed in [13-14], equation (3) corresponds to the number of stages to obtain the best power conversion efficiency. However, as we will show later, this value of the number of stages results in a sub-optimal value for the output power. As discussed in Section I, in micro-scale energy harvesting systems, the eventual goal is

to maximize the net harvested power, which is different from maximizing the power conversion efficiency of the SCPC. Therefore, in contrast to existing work, this paper proposes techniques to optimize the number of SCPC stages with the goal of maximizing net harvested power.

## III. System Description and Analysis

Figure 1 shows the generic block diagram of an SCPC-based micro-scale energy harvesting system. The control unit provides non-overlapped clock signals ($\Phi$ and $\Phi_B$) to drive the SCPC stages. Based on the input voltage level, the control unit may be powered either by the energy transducer itself or by the energy buffer.

If the energy transducer is composed of multiple-stacked units, it's output voltage $V_{IN}$ will be high enough (e.g., 2V) to support the normal operation of the control unit. Thus, the control unit will be directly powered by the energy transducer, and the SCPC output power ($P_{OUT}$) is the net power flowing into the energy buffer. We consider and analyze this scenario as case *I*. However, if the energy transducer is of non-stacked type, its output voltage $V_{IN}$ will be too low (e.g., 0.3V) to maintain the normal operation of control unit. Thus, the energy buffer has to act as the power supply for the control unit and enables the initial bootstrapping of the entire system [10]. If the power loss in the control unit is given by $P_{LOSS}$, the goal of the optimization should be to maximize the net harvested power (i.e., $P_{OUT}$ - $P_{LOSS}$), instead of $P_{OUT}$ itself. This scenario will be considered and discussed as case *II*.

For a given amount of hardware cost (i.e., on-chip transistor count and capacitor size), system designers may use all of the hardware to architect an SCPC with a single long branch (i.e., more number of stages), or may build multiple parallel branches with each of them having less number of stages. Assume that an SCPC consists of multiple parallel branches. Then, the total output harvested power can be modeled as:

$$P_{TOTAL} = Number\ of\ Branches \times P_{BRANCH} = \frac{Hardware_{TOTAL}}{Hardware_{BRANCH}} \times P_{BRANCH} \quad (4)$$

where $P_{BRANCH}$ is the net output power of each branch, and $P_{TOTAL}$ is the total net output power for a given hardware cost. The expression (4) can be further organized as:

$$P_{TOTAL} = Hardware_{TOTAL} \times \frac{P_{BRANCH}}{Hardware_{BRANCH}} \quad (5)$$

From (5), it can be inferred that for a given total hardware cost, maximizing the total net output power is equivalent to maximizing the ratio of net output power per branch to the corresponding hardware cost of each branch. We define this ratio as our primary figure-of-merit (*FOM*). In the next subsections, we will take into account both design cases defined above and optimize the number of stages in each branch. We assume that linear topology SCPCs [5, 9] are used in each branch. The schematic of an *N*-stage linear topology SCPC is shown in Figure 3. During each clock cycle ($\Phi$, $\Phi_B$), the charge from the previous stage is stored on a capacitor and is then transferred to the subsequent stage. At the final stage, the total harvested charge is dumped into the energy buffer. We picked the linear topology mainly because its hardware cost is proportional to the number of stages and hence is easy to model in a generic expression. However, note that the actual derivation and design flow can also be applied to other topologies.

### A. Stage Number Optimization for Case I

In this subsection, we model the output behavior of an SCPC and derive an equation for the best number of stages for case *I*.

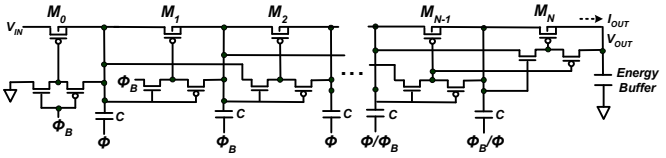


Figure 3. *S*chematic view of an N-stage linear topology SCPC

According to [6, 9, 13], the average output current of an *N*-stage linear step-up SCPC with ideal switches is given by:

$$I_{OUT} = \frac{fC}{N}[(N+1)V_{IN} - V_{OUT}] \quad (6)$$

where *N* is the number of stages, *C* is the capacitance used in each stage, and *f* is the switching frequency. This equation indicates that in energy harvesting systems, the output current of a SCPC does not vary with the load application current ($I_{LOAD}$ in Figure 1). As a result, in the rest of this paper, the variation of loading current will not be taken into account. For a linear topology, the hardware cost is proportional to the number of stages. Therefore, the figure-of-merit can be modeled as:

$$FOM = \frac{V_{OUT}I_{OUT}}{N} = \frac{fC}{N^2}[(N+1)V_{IN} - V_{OUT}]V_{OUT} \quad (7)$$

System designers usually know the input voltage (i.e., energy transducer's voltage) and output voltage (energy buffer's voltage) before designing the power converter. Therefore, for a given set of input and output voltage levels, in order to maximize the figure-of-merit, we take the derivative of (7) with respect to the number of stages and set the result to zero. Thus, we can obtain the optimal number of stages as:

$$N_{OP} = 2\left(\frac{V_{OUT}}{V_{IN}} - 1\right) \quad (8)$$

Substituting (8) back into (7), we can estimate the figure-of-merit for our proposed optimization strategy as:

$$FOM = \frac{fCV_{OUT}V_{IN}^2}{4(V_{OUT} - V_{IN})} \quad (9)$$

In contrast with the expression (3), it is clear that the number of stages for maximizing the output power per unit hardware cost is twice the number of stages for maximizing

the power conversion efficiency. In addition, substituting the expression (3) into (7) results in a much smaller value for the figure-of-merit than expression (9).

Note that when we take the derivative of (7) with respect to the number of stages $N$, the calculated optimal number of stages is not restricted to be an integer. In reality, the number of stages can only be an integer, so we take the ceiling of the computed value. Moreover, some non-idealities such as output current saturation, etc., are ignored in the derivation. As a result, the expression (8) can be viewed as an approximate, yet easy to derive analytical estimation for the optimal number of stages. Next, we will refine the exact optimal number of stages further through transistor-level circuit simulations.

### B. Stage Number Optimization for Case II

In this subsection, we focus on the analysis of case *II*, where the energy transducer voltage is very low and therefore, the energy buffer powers the control unit. The power loss due to the control unit should be deducted from the SCPC output power to calculate the net harvested power. As addressed in [11], the dynamic power consumption dominates the total power loss of the control unit. The total power loss of an $N$-stage linear topology SCPC can be modeled as:

$$P_{LOSS} = NC_L f V_{OUT}^2 \quad (10)$$

where $C_L$ is the equivalent switched capacitance per stage, which varies with the switch transistor sizing. The net output power of an SCPC is equal to:

$$\begin{aligned} P_{OUT,NET} &= P_{OUT} - P_{LOSS} \\ &= \frac{fC}{N}[(N+1)V_{IN} - V_{OUT}]V_{OUT} - NC_L f V_{OUT}^2 \\ &= fV_{OUT}[\frac{C}{N}(N+1)V_{IN} - (\frac{C}{N} + NC_L)V_{OUT}] \quad (11) \end{aligned}$$

The figure-of-merit is, therefore, modeled as:

$$FOM = \frac{fV_{OUT}}{N}[\frac{C}{N}(N+1)V_{IN} - (\frac{C}{N} + NC_L)V_{OUT}] \quad (12)$$

To maximize the *FOM*, we take the derivative of (12) with respect to the number of stages and set the result to zero. Thus, we calculate the optimal number of stages as:

$$N_{OP} = 2(\frac{V_{OUT}}{V_{IN}} - 1) \quad (13)$$

Substituting (13) back into (12), we can estimate the figure-of-merit for our proposed optimization strategy as:

$$FOM = \frac{fCV_{OUT}V_{IN}^2}{4(V_{OUT} - V_{IN})} - fC_L V_{OUT}^2 \quad (14)$$

The expression (13) reveals that the optimal number of stages in case *II* is the same as that in case *I*. The optimal number of stages in case *II* does not vary with the power loss component ($P_{LOSS}$) as well as the switched transistor capacitance ($C_L$). However, compared to (9), the expression (14) represents a lower figure-of-merit due to its second term. This is because the power loss component degrades the amount of net output power in case *II*.

### C. Design Examples

To better understand and refine the analytical results in the prior subsections, we consider two typical design examples to make an in-depth investigation of our proposed strategy.

The first example is used to analyze design case *I*, where the output power of an SCPC is exactly the net output power. For this example, assume that the energy transducer voltage is 1V and the energy buffer voltage is 1.9V. If the number of stages is calculated based on the design approach in [13-14], according to the expression (3), the optimal integer number $N$ is 1. Substituting $N = 1$ back into (7), we get:

$$FOM_{N=1} = 0.19\,fC \quad (15)$$

On the other hand, if the stage number is based on our proposed design approach, according to the expression (8), the optimal stage number $N$ is calculated to be 1.8. Since $N$ must be an integer number, its approximate solution is 2. Substituting $N = 2$ back into (7), we obtain

$$FOM_{N=2} = 0.5225\,fC \quad (16)$$

To make a complete comparison, we also calculated the *FOM* for $N = 3$, 4, 5, and 6. Figure 4 shows how the analytical results of the figure-of-merit vary with the number of stages.

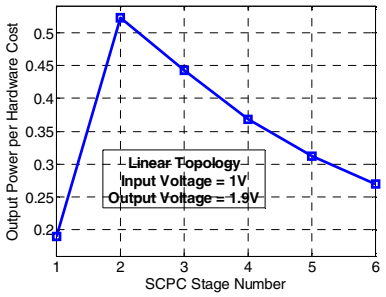


Figure 4. Analytical results of *FOM* vs. number of stages in example one

From the above figure, we can observe that the number of stages has a significant impact on the figure-of-merit and a value of two is the optimal value in this specific design example. Our proposed design strategy ($N$ = 2) exhibits an increase of around 175% in the figure-of-merit, compared to the design strategy ($N$ = 1) in [13-14]. As we show in Section IV, this analytical result will be validated by transistor-level circuit simulations.

The second example is to investigate design case *II*. The input and output voltages are 0.3V and 1V, respectively. The switch transistor per stage is assumed to be 30μm/60nm, thus, $C_L$ is approximated to be 0.22pF. The capacitor $C$ has a size of 20pF for each stage. Since the input voltage is too low to support the operation of the control unit, the energy buffer provides power for the control unit. According to (13), the estimated optimal number of stages is:

$$N_{OP} = 4.667 \quad (17)$$

Since $N$ must be an integer, we take the ceiling of the computed value to obtain an integer value of 5. Substituting it back into (14), we obtain the figure-of-merit as:

$$FOM_{N=5} = 0.42f \quad (18)$$

According to the expression (3), $N = 3$ is the optimal number of stages for achieving the best power conversion efficiency, and the calculated figure-of-merit for $N = 3$ is

$$FOM_{N=3} = 0.2244f \quad (19)$$

We also calculated the figure-of-merit from $N = 4$ to $N = 8$ and plotted the results in Figure 5. We can observe that the optimal value for the number of stages is five in this specific example. In contrast with the design strategy ($N = 3$) in [13-14], our proposed design ($N = 5$) shows an increase of around 87% in the figure-of-merit. This analytical result will be verified by transistor-level circuit simulations in section IV.

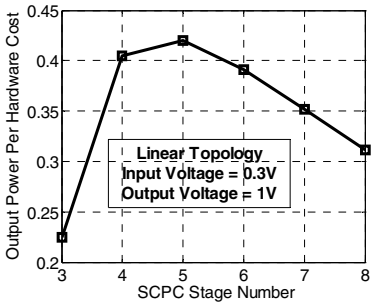


Figure 5. Analytical results of FOM vs. number of stages in example two

Figure 6 plots a 3D graph showing the relationship between the optimal number of stages and the input and output voltages. Since we only consider voltage-boosting power conversion in this paper, when the input voltage is higher than the output voltage, the optimal number of stages is zero. As input voltage decreases or output voltage increases, we can observe a significant difference between the optimal number of stages computed using the existing approach and our proposed approach.

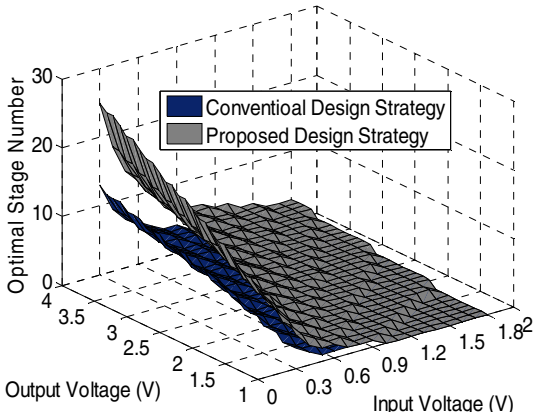


Figure 6. Optimal no. of stages using existing and proposed approaches

## IV. Simulation Results

In order to validate our proposed analysis and design approach, we have designed and simulated several SCPCs using IBM 65nm CMOS technology. HSPICE simulations were carried out using the BSIM models.

Our first simulation was to verify the proposed expressions for design case *I*, where the energy transducer provides power to the control unit, and the output power of the SCPC is the net output harvested power. The simulation environment was set up as follows. The input and output voltages were 1V and 1.9V, respectively. The switch transistor was set to 3µm/60nm and a 20pF capacitor was used in each stage. Four switched-capacitor power converters with number of stages varying from one to four were implemented for simulations. The clock switching frequency to the SCPCs was varied from 2MHz to 50MHz.

Figure 7 shows the result of our simulation and plots the output power per unit hardware cost (our figure-of-merit) as a function of the switching frequency for several values of $N$. It is evident from the figure that, for any value of switching frequency, the highest output power per unit hardware cost is obtained by using an SCPC with $N = 2$ stages. Given a hardware budget that a system designer has at his/her disposal (say K times the unit hardware cost), the total harvested power from the energy transducer can be computed by scaling up each curve in Figure 7 by a factor of K. Note, for any energy harvesting system, the output power of an SCPC is limited by the maximum power converted by the energy transducer. With the increase of parallel branches, the total harvested power will be restricted and never goes to infinity.

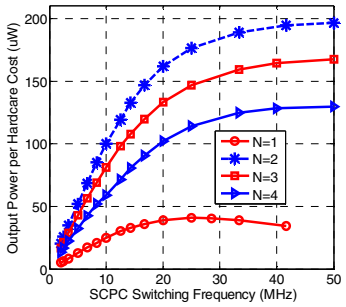


Figure 7. Output power per unit hardware cost versus switching frequency

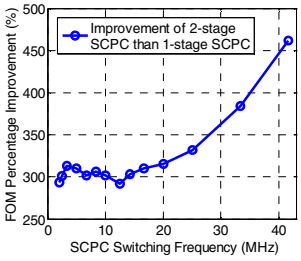


Figure 8. Percentage improvement in the figure-of-merit

Figure 8 shows the percentage improvement obtained in the figure-of-merit by the proposed approach, compared to the

existing approach of maximizing the power-efficiency of the SCPC. The figure shows that our proposed strategy achieves at least 290% improvement in net harvested power per unit hardware cost compared to the existing stage number optimization technique.

The second circuit simulation evaluated the energy harvesting performance and figure-of-merit for design case *II*. For this simulation, the input and output voltages were set to 0.3V and 1V, respectively. The switch transistor per stage was designed to be 30µm/60nm. The capacitor $C$ has a size of 20pF for each stage. Six different SCPCs with number of stages ranging from three to eight were implemented and the clock frequency was varied from 2MHz to 100MHz.

Figure 9 plots the net output power per unit hardware cost as a function of the switching frequency. This figure clearly illustrates that an SCPC design with $N = 4$ or $N = 5$ has the highest net output power per unit hardware cost compared to SCPC designs with other values of $N$. Figure 10 shows the percentage improvement obtained in the figure-of-merit by the proposed approach, compared with the existing approach of maximizing the power-efficiency of the SCPC, which would pick an SCPC with $N = 3$. As can be seen in this figure, our design with $N = 5$ results in an improvement of 60% - 110% in the figure-of-merit compared to a design with $N = 3$.

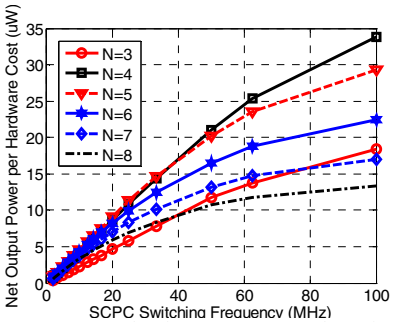


Figure 9. Output power per hardware cost versus the switching frequency

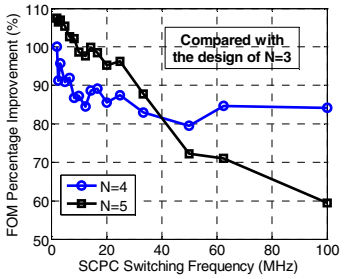


Figure 10. Percentage improvement in the figure-of-merit

## V. CONCLUSION

Environmental energy harvesting represents a promising approach to powering ultra-low power systems in a variety of emerging applications. Maximizing the amount of harvested power from an energy transducer is one of the primary design goals in micro-scale energy harvesting systems. In this paper, we showed that the conventional approach to SCPC stage number selection, which aims to maximize power conversion efficiency of the SCPC, results in a substantially sub-optimal value for the total harvested power from the transducer. We proposed a new technique to estimate the optimal number of stages for an SCPC to maximize the amount of harvested power. We designed and implemented multiple SCPCs using IBM 65nm CMOS technology based on the proposed stage number selection technique. HSPICE simulation results were used to verify our proposed SCPC stage number optimization technique. Simulation results demonstrated that our proposed technique results in an increase of 60% - 290% in the net harvested power, compared to existing approaches.

## ACKNOWLEDGEMENT

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