Low-Power Smart Industrial Control

Attila Bilgic, Vincent Pichot, Michael Gerding
KROHNE Messtechnik GmbH
Ludwig-Krohne-Str. 5
47058 Duisburg, Germany
{a.bilgic,v.pichot,m.gerding}@krohne.com

Felix Bruns
Ruhr-Universität-Bochum
Universitätsstr. 150
44801 Bochum, Germany
felix.bruns@ruhr-uni-bochum.de

Abstract—Measurement equipment for process control in the chemical industry has to face severe restrictions due to safety concerns and regulations. In this work, we discuss the challenges raised by safety concerns and explain how they lead to strong power and energy constraints in the design of industrial measurement equipment. We argue that a comprehensive strategy in the design and implementation of hardware and software on one hand, and power management on the other hand is required to satisfy these constraints. Furthermore we demonstrate solutions for the power efficient design of the computing system and bus topology in an industrial environment.

I. INTRODUCTION

In many production processes in the chemical industry, a significant environmental, financial and personal risk is involved. Hence, great caution and safety measures are required in order to control the risk. This is particularly the case for processes which can accidentally or invariably lead to the generation of explosive gases. In these environments, a strict set of norms[1][2] regulate the deployment of safety measures[3] and the requirements which electronic equipment has to fulfill. These requirements pose strong challenges to the design of electronic control and sensor devices.

There are multiple methods of protection against explosion. The preferred solution differs between industries and countries. For example, in the petrochemical industry, the most common safety concept is the encapsulation of devices and interconnects in pressurized housings, which are strong enough to detain an explosion. In other chemical industries, devices and interconnects which are *intrinsically safe*[4] are frequently employed. This means, that the electric and thermal energy stored in devices and interconnects are limited to small amounts, which are too low to cause an ignition of an explosive atmosphere.

Depending on the realization of power supply and communication interface, measurement equipment can roughly be separated into two classes of devices. On one hand, so-called *four-wire* equipment, which has dedicated and separate power supply and communication connections. On the other hand, in *two-wire* equipment, power supply and communication use the same wire.

Using two-wire technology, the measurement equipment and the control station are connected point-to-point by use of a current loop. The measurement equipment is able to adjust the current in a range between 4 and 20 mA and encodes

the measured value in this way. The control station delivers the energy for the current loop and reads the measurement value by monitoring the current consumption. As a result of this design, the power density available inside devices and interconnects can be limited to uncritical levels and the communication is extremely robust against interference. On the other hand, a minimal current of 4 mA at a minimum voltage of 12 V results in a minimal power input of 48 mW for a sensor device. Consequently, two-wire devices have to operate under extreme power constraints which require attention at all levels of the systems design.

In contrast to four-wire equipment, two-wire measurement equipment is suitable for intrinsic safety concepts due to the power limitations. Therefore two-wire measurement equipment is the most flexible and preferred solution for deployment in hazardous areas.

In this paper we demonstrate basic concepts for the design of power efficient two-wire measurement equipment. In Section II we introduce the architecture of two-wire sensor platforms and detail the constraints under which the device has to operate. In Section III we demonstrate solutions for the power management of the sensor platform with focus on the computing system. We discuss the power consumption of the device-internal communication in Section IV and conclude this work in Section V.

II. PLATFORM ARCHITECTURE

A typical two-wire sensor platform is shown in Fig. 1. It can be divided into the sensor component, which measures a physical value and transforms it to a digital representation, and the converter, which controls the state of the system and the communication with the control station. The sensor and converter components communicate over an internal bus.

The sensor utilizes a physical effect to measure one or several parameters of an industrial process, executes all data processing which is relevant to the measurement and forwards the result to the converter. The field of application are e.g. measurement of flow, temperature, pressure or tank gauging. Depending on the field of application and on the measurement principle, the processing power which is required in the sensor varies strongly. Whereas a simple filtering algorithm or an estimation of a maximum peak suffices in many applications, others e.g. measurement of a tank level by radar, require the calculation of a fast fourier transform and several filtering
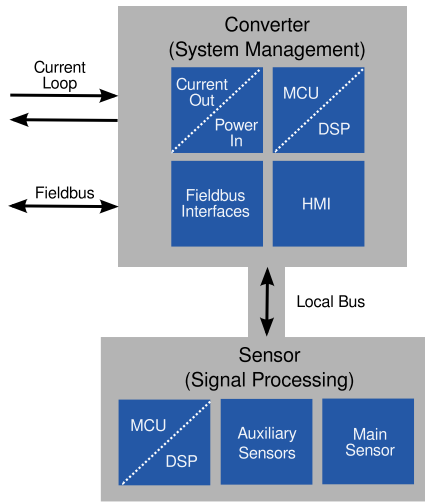
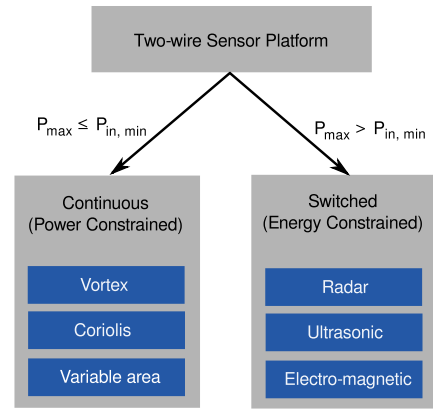Fig. 1.   Schema of a two-wire sensor platform

Fig. 2.   Classification of two-wire sensor platforms. Devices operating continuously are power constrained, whereas switched devices are energy constrained.

algorithms. Thus, some sensors are equipped with a small Micro-Control Unit (MCU), whereas powerful Digital Signal Processors (DSP) are required in other applications.

The tasks of system management and communication are performed by the converter. It handles the communication with the control station via the current loop or attached fieldbusses. It collects information about the system state, checks the consistency of the measurement value[5] and it is responsible for the system power management. In addition, it provides a Human Machine Interface (HMI) for maintenance and control tasks which consists of display, keypad and a service input. Frequently, the converter has to handle a large number of parallel tasks under real-time constraints. Furthermore, it can be a computing intensive task to check the data for consistency. Therefore, at least one MCU and sometimes several MCUs or DSPs are required in the converter.

As a result, a single two-wire sensor platform consists of two or more MCUs and forms a complex, power restricted distributed system, which is part of a larger distributed system in the control network of the chemical process.

A. Standardization and Safety requirements

In order to protect against explosion, it has to be prevented that a spark or heat from the sensor equipment ignites an hazardous atmosphere. As already mentioned in Section I, there are multiple ways of providing protection against explosion. Unfortunately, it is frequently required to combine several safety concepts to realize a single measurement device. For example, the sensor frequently has to be placed remotely from the converter and it is a high effort to provide explosion proof housing for the sensor and wiring. In this case, it is advantageous to provide an intrinsically safe sensor and intrinsically safe communication between sensor and converter. Then it is necessary to decouple the two protection domains by the use of suitable barriers, which ensure that the intrinsic safety is not compromised. To achieve this, it has to be prevented that a malfunctioning converter transmits a large electrical charge

into the intrinsically safe domain. This is usually achieved by the use of a safety barrier which can consist of diodes to limit voltages and resistors to limit current. Unfortunately, these devices cause a significant power loss.

Additional safety measures for electromagnetic compatibility require that the device is galvanically isolated. The galvanic isolation usually consists of transformers for the power supply and optocouplers or capacitative coupling for fieldbus lines. Again these elements cause a significant loss of power. Finally, power is lost in the conversion to a lower voltage, which is required by the computing system. As a result of these losses, a power budget of only $P_{in.min} \approx 30 \ mW$ is available for sensor, display, communication and the various MCUs.

B. Classification of Sensor Devices

The different measurement principles that are applied in two-wire sensor platforms exhibit large differences in the power consumption of the sensor due to physical differences in the measurement principles. Some sensors consume a higher instantaneous power than the power which can be be provided by the current input. Therefore the power has to be accumulated in a capacitance in the sensor platform. The accumulated energy is used to periodically activate the sensor. However, adding an energy buffer to the device increases the effort for safety certification.

We exemplify this approach with a radar sensor for level measurement. A complete sensor typically consumes roughly $750 \ mW$ of power and requires about $15 \ ms$ for one measurement. If a measurement has to be executed at least once a second, the sensor has to be supplied with a mean power of $11.25 \ mW$. Hence the radar platform's energy buffer has to accumulate at least $E = P \cdot t = 11.25 \ mJ$. In the dimensioning of the capacitor it has to be taken into account that the sensor platform has to operate in harsh industrial environments with large temperature ranges. In addition, the degradation of the capacitor due to aging effects has to be expected.

Other devices, especially those which measure flow, operate continuously. As a result, the measurement principles of two-

wire sensor platforms can be distinguished between continuous and switched operation as shown in Fig. 2.

III. Power Management

Since power consumption $P_{cont,max}$ of continuously operating devices has to be smaller than $P_{in,min}$, these devices operate under strict power constraints. Hence, great care has to be taken in the design and choice of sensor, computing system and peripherals to ensure that the power consumption stays in the permitted range.

In switched devices, the energy buffer can compensate a temporary power peak $P_{sw,max}$. However, the power management has to observe the amount of energy stored in the capacitor and adjust the system's measurement rate accordingly, in order to avoid a failure of the power supply. Since an acceptable measurement rate has to be guaranteed even at the minimal input current, the system has to be designed for energy efficiency. In case a higher input current is available, it is desirable to increase the measurement rate and thereby improve the measurement response time. Consequently, switched systems have to provide a high energy efficiency and a high computing performance at hard real-time constraints.

A straight forward way to safe energy is to deactivate unused peripherals and components[6], when they are not required. Consequently, the system's peripherals have to provide stand-by modes with very low power consumption. Since it takes a certain amount of time to activate and deactivate peripherals, the converter has to operate highly predictable not to violate real-time constraints[7].

A. Computing System

A predictable and proven scheduling mechanism is required in order to guarantee real-time behavior and predictable power management. This can for example be achieved with rate-monotonic scheduling[8].

In a continuously running system, the instantaneous power consumption of the processor should be as low as possible. Ideally, the processor's performance should fit exactly to the requirements of the application. If the processor is too fast, it consumes more power than necessary in its active time interval and is idle afterward. A complete utilization of the processor under real-time constraints can be achieved by use of rate-monotonic scheduling in combination with harmonic periods[9]. Fig. 3 shows an example of a harmonic, rate-monotonic schedule for two tasks. The task parameters are given in (1) and (2), where P is the period, T is the worst-case execution time and U is the processor utilization caused by the respective task. As can be seen in Figure 3, the total processor utilization is $U_{total} = 0.75$. Since the task periods are harmonic, both tasks will finish within their period and thus meet their deadline as long as $U_{total} \leq U_{max} = 1$.

$$P_1 = 2 \ ms \qquad T_1 = 0.5 \ ms \qquad U_1 = \frac{T_1}{P_1} = 0.25 \quad (1)$$

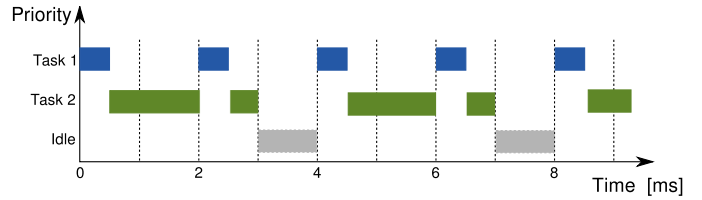$$P_2 = 4 \ ms \qquad T_2 = 2 \ ms \qquad U_2 = \frac{T_2}{P_2} = 0.5 \quad (2)$$

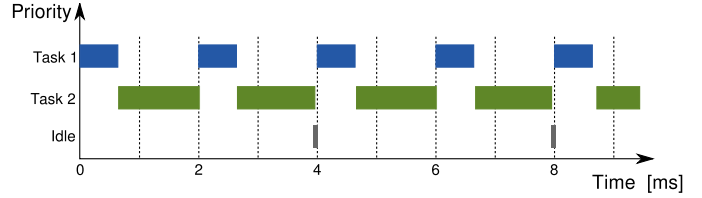Fig. 3. A rate monotonic schedule consisting of two tasks with a total utilization of 0.75

Fig. 4. Rate monotonic schedule, with processor frequency scaled by $\alpha = 0.75 + e$ to minimize idle times

$$U_{total} = U_1 + U_2 = 0.75 \quad (3)$$

The processor frequency can thus be scaled by a factor of $\alpha = \frac{U}{U_{max}} = 0.75 + e$ in order to maximize the processor utilization, where e is small safety factor which accounts for operating system overhead and non-deterministic effects. As a result, the processor runs less energy efficient due to a higher amount of static energy consumption. However, the power consumption is scaled almost linearly to the factor α. The resulting schedule with $T_1 = 0.66 \ ms$ and $T_2 = 2.66 \ ms$ is shown in Figure 4. The processors supply voltage can often be lowered to achieve a further decrease in power consumption[10][11] at the cost of additional complexity in the power supply.

In contrast to continuously running systems, the processor should achieve a maximum of energy efficiency in a switched system. Energy efficient processors usually provide a low power mode, in which they consume only about $0.1 \ \% - 1 \ \%$ of their active power consumption. Hence, static energy consumption can be decreased by running the processor at a maximum clock frequency, and thereby change to the processors low power mode as soon as possible. This has the additional benefit, that enough spare processor capacity is available if the measurement rate has to be increased.

Another way to increase the energy efficiency is to use specialized DSPs for signal processing tasks such as filtering algorithms. A DSP can compute such algorithms extremely fast and efficient, but might not provide a sufficient low power mode. In this case, the power manager can disconnect the DSP from the supply voltage when it is unused. Consequently, to obtain an optimal solution it is necessary to incorporate the global power management strategy into the choice and design of hardware components.

Finally, huge differences in the energy efficiency of a specific algorithm exist between different processors. An analytical comparison is cumbersome due to differences in

	Architecture	Clk. Frequency [MHz]	Mean Current [mA]	Energy [pJ]
MCU16	16 bit	18	1.3	390
MCU32	32 bit	14	0.275	75

the processors power consumption, performance, low power modes and peripheral configuration. Table I shows the results of a benchmark between two widely employed low power MCUs, which were used in the digital signal processing of a flow sensor. MCU16 is a 16 bit microcontroller which provides an optimized set of low power peripherals which can be used in the processors low power mode. MCU32 is a 32 bit microcontroller which runs at a lower clock frequency than MCU16, but which has a more powerful instruction set that provides a bigger computational performance for signal processing algorithms.

The signal processing algorithm is executed with a period of $100\ ms$. During each interval, it reads a number of values with the processors Digital-to-Analog Converter (DAC), filters the values, and transforms them to a digital representation of the measured flow. In order to avoid an unfair disadvantage to MCU16, the algorithm uses 16 bit data representation. In MCU16, the algorithm uses the processor's DMA controller to read DAC values and to shift filter delay lines. Since the DMA on MCU16 can be used in the processors low power mode, the processor core can be kept longer in low power mode and has to be woken up less frequently. Using MCU32, the DMA is not used. However, since MCU32 has a larger performance, it finishes the signal processing earlier and achieves a lower duty cycle. A measurement of the mean input current shows, that MCU32 achieves a five- times lower energy consumption. Hence, in this case the benefit of larger computational power surpasses the benefit of low complexity and better peripheral configuration. However, the comparison is highly dependent on the specific software characteristics. The experimental comparison illustrates, that a high amount of energy can be saved by a comprehensive analysis of a given task and choice of the most optimal processor.

IV. BUS TOPOLOGY

Due to the nature of the sensor platform as a distributed system, a large amount of data has to be transferred between the various MCUs. The communication can lead to significant consumption of power, which is shown with the physical layer of an I^2C-bus in Fig. 5.

The physical layer consists of a clock line and a data line for serial transmission. Transistors function as open-collector output to force the low state on the data and clock line. If a transistor is deactivated, the pull-up resistors R_P pull the lines into high state. The main contributor to power consumption are the pull-up resistors which, depending on the bus capacitance, typically have a value in the range of several kilo-ohms. At a
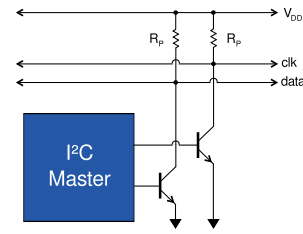
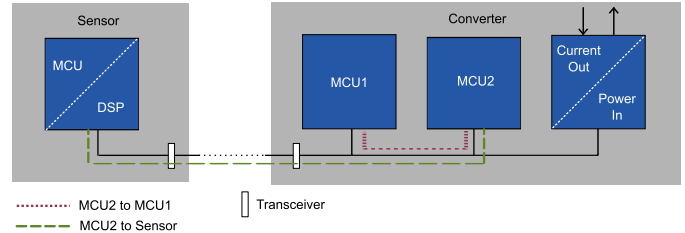

Fig. 5.   Physical layer of an I^2C-bus

Fig. 6.   Bus topology of a two-wire sensor platform

voltage $V_{DD} = 3\ V$, the power consumption of the resistors during low state can reach up to $10\ mW$.

Fig. 6 shows a simplified bus topology of a two-wire platform. A single bus line connects the functional units and various MCUs in sensor and converter. A suitable physical design of the sensor electronics ensures, that the bus line is kept as short as possible. Then resistors with larger values can be chosen, since they have to drive a smaller bus capacitance. As a result, the power consumption is reduced.

Furthermore, for high energy efficiency of the communication, the number of bus transmissions should be as low as possible, and require a minimum of protocol overhead. To achieve this, an optimal distribution of tasks among the MCUs and a protocol design which is specialized for the needs of a sensor platform, is required. For example, a token ring bus is not well suited, since the forwarding of the token causes bus activity and wakes a client from low power mode, even when the client does not have data to transfer.

The communication between sensor and converter can still be an especially power consuming burden. Frequently, the converter has to be placed separately from the sensor, since the sensor is difficult to access. Consequently, the bus line has to be long, which requires smaller and more power consuming resistances and a termination of the bus in order to prevent signal reflection and interference. Furthermore the information has to cross safety barriers, galvanic isolation and driver stages. Therefore it is appropriate to avoid unnecessary bus transactions between sensor and converter.

An architecture with a split bus topology[12] is shown in Fig. 7. The converter possesses a private bus for internal communication. Communication between sensor and converter can only occur through MCU1. Hence, additional routing functionality is required in MCU1 to enable a communication between MCU2 and the sensor. However, unnecessary activity on the long bus line which connects the sensor is avoided and
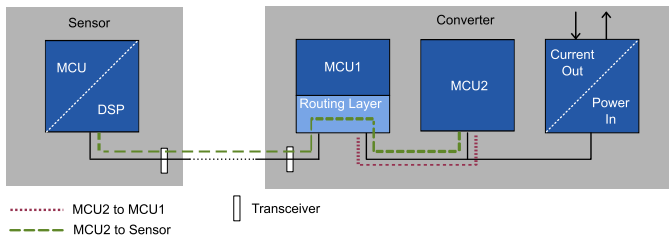
Fig. 7.   Improved bus topology for energy efficiency

for inverter internal communication, a much shorter bus length has to be driven. Therefore larger pull-up resistors can be used and the power and energy consumption is reduced accordingly.

V. CONCLUSION

The design of two-wire measurement equipment requires to pay extreme attention to power and energy consumption. A conclusive, system wide strategy of power management and power aware design is required to fulfill power and performance constraints. In this work, we argue that using current processor technology, it is not possible to close the gap between low power modes and high computation mode in two-wire sensor devices. As a result, several processors at different performance levels are required and complex power management schemes have to be applied in order to meet the power and energy constraints.

We show, that large differences exist in the optimization for low power and low energy consumption and demonstrate possible optimizations for both in the computing system. Finally, we demonstrate how the power consumption can be reduced by an optimization of the bus topology.

REFERENCES

[1] *IEC 60069 - Electrical apparatus for explosive gas atmospheres*, International Electrotechnical Commission, 2008.

[2] *ATEX 94/9/EC - Appareils destins tre utiliss en ATmosphres EXplosibles*, Directive of the European Union, 1994.

[3] *IEC 61508 - Functional Safety of Electrical/Electronic/Programmable Electronic Safety-Related Systems*, International Electrotechnical Commission, 2009.

[4] D. Wolf-Dieter, *Explosionsschutz durch Eigensicherheit*. Vieweg, 1993.

[5] *NAMUR NE43 - Standardization of the Signal Level for the Failure Information of Digital Transmitters*, NAMUR, 2003.

[6] S.-M. Kang, "Elements of low power design for integrated systems," in *Proceedings of the 2003 international symposium on Low power electronics and design*, ser. ISLPED '03.   New York, NY, USA: ACM, 2003, pp. 205–210. [Online]. Available: http://doi.acm.org/10.1145/871506.871558

[7] P. Kumar and M. Srivastava, "Predictive strategies for low-power rtos scheduling," in *Proceedings of the 2000 IEEE International Conference on Computer Design: VLSI in Computers & Processors*, ser. ICCD '00.   Washington, DC, USA: IEEE Computer Society, 2000, pp. 343–. [Online]. Available: http://portal.acm.org/citation.cfm?id=557517.846902

[8] C. L. Liu and J. W. Layland, "Scheduling algorithms for multiprogramming in a hard-real-time environment," *J. ACM*, vol. 20, pp. 46–61, January 1973. [Online]. Available: http://doi.acm.org/10.1145/321738.321743

[9] G. Buttazzo, "Rate monotonic vs. edf: Judgment day," in *Embedded Software*, ser. Lecture Notes in Computer Science.   Springer Berlin / Heidelberg, 2003.

[10] G. Magklis, M. L. Scott, G. Semeraro, D. H. Albonesi, and S. Dropsho, "Profile-based dynamic voltage and frequency scaling for a multiple clock domain microprocessor," in *Proceedings of the 30th annual international symposium on Computer architecture*, ser. ISCA '03. New York, NY, USA: ACM, 2003, pp. 14–27. [Online]. Available: http://doi.acm.org/10.1145/859618.859621

[11] J. Luo and N. K. Jha, "Static and dynamic variable voltage scheduling algorithms for real-time heterogeneous distributed embedded systems," in *Proceedings of the 2002 Asia and South Pacific Design Automation Conference*, ser. ASP-DAC '02.   Washington, DC, USA: IEEE Computer Society, 2002, pp. 719–. [Online]. Available: http://portal.acm.org/citation.cfm?id=832284.835506

[12] C.-T. Hsieh and M. Pedram, "Architectural energy optimization by bus splitting," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 21, no. 4, pp. 408 – 414, April 2002.