Obstacle-Aware Multiple-Source Rectilinear Steiner Tree with Electromigration and IR-Drop Avoidance

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Abstract—**Based on the width determination of any current-driven connection for electromigration and IR-drop avoidance, an area-driven multiple-source routing tree can be firstly constructed to minimize the total wiring area with satisfying the current flow in Kirchhoff's current laws and the electromigration and IR-drop constraints. Furthermore, some Steiner points can be assigned onto feasible locations to reduce the total wiring area under the electromigration and IR-drop constraints. Finally, an obstacle-aware multiple-source rectilinear Steiner tree can be constructed by assigning the obstacle-aware minimum-length physical paths for all the connections. Compared with Lienig's multiple-source Steiner tree[7], the experimental results show that our proposed approach without any IR-drop constraint can reduce 10.5% of the total wiring area. Under 10%V_{dd} and 5%V_{dd} IR-drop constraints, the experimental results show that our proposed approach can satisfy 100% electromigration and IR-drop constraints and reduce 7.5% and 4.9% of the original total wiring area on the average for tested examples, respectively.**

I. INTRODUCTION

In general, electronic interconnections in modern integrated circuits have an intended MTTF(mean time to failure) of at least 10 years. The failure of a single interconnection caused by electromigration can result in the failure of the entire circuit. At the end of the 1960s, the physicist J. R. Black developed an empirical model to estimate the MTTF of any interconnection and to take the electromigration factor into consideration[1] as follows:

$$MTTF = \frac{A}{J^n} \cdot \exp(\frac{E_a}{k \cdot T}),$$

where A is a material constant based on the cross-sectional area of the interconnection, J is the current density, E_a is the activation energy, k is the Boltzmann constant, T is the temperature and n a scaling factor.

The MTTF mainly depends on temperature and current density due to electromigration. Unlike digital circuits, analog circuits must handle a multitude of different current levels, including extremely large currents in some applications. Hence, the interconnection must be designed with the current that will be imposed on it in mind. Interconnect with an insufficient width may be subject to electromigration and eventually might cause the failure of the circuit at any time during its lifetime [1-3]. For analog signal wires, the DC currents where the metal is subject to an electron wind from a constant direction are considered. Because the ongoing reduction of circuit feature sizes has aggravated the electromigration problem, it becomes crucial to address the problems of current densities and electromigration during the routing of the interconnections for analog circuits.

Layout for analog circuits has historically been a manual, time-consuming and trial-and-error task. A primary reason for the lack of automation is the vast amount of expert knowledge typically required to meet constraints such as electrical/thermal symmetry, electromigration, voltage drops, temperature gradients, etc. Recently, many current-driven routing approaches[4-9] are proposed to solve the routing problem for electromigration avoidance in analog circuits. For a multiple-source signal net, the routing problem can be divided into *wire planning* and *wire routing*. Generally speaking, wire planning determines the routing topology by constructing an area-driven routing tree and wire routing assigns the physical path by constructing an area-driven rectilinear Steiner tree. The proposed approaches discuss different current-driven wire planning techniques and wire routing approaches. For advanced process, the wiring resistance of any signal net dominates the IR-drop result. However, the proposed approaches[4-9] may violate the IR-drop constraint in a multiple-source routing tree during wire planning because of ignoring the effect of the wiring resistances. Besides that, Yan's approach[8] does not consider the obstacles in a routing plane and Jiang's approach[9] only considers the wire planning for topology generation.

In this paper, based on the width determination of any current-driven connection for electromigration and IR-drop avoidance, an area-driven multiple-source routing tree can be firstly constructed to minimize the total wiring area with satisfying the current flow in Kirchhoff's current laws and the electromigration and IR-drop constraints. Furthermore, some Steiner points can be assigned onto feasible locations to reduce the total wiring area under the electromigration and IR-drop constraints. Finally, an obstacle-aware multiple-source rectilinear Steiner tree can be constructed by assigning the obstacle-aware minimum-length physical paths for all the connections.

II. PRELIMINARIES AND PROBLEM FORMULATION

In current-driven analog circuits, the determination of the realistic current value of each terminal in a signal net is important. Most approaches[4-8] use the *equivalent current value* to model the current value of any terminal in a signal net.

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By simulating a circuit netlist, a set of the current values is manually attached to the terminals in the schematic netlist. Furthermore, each terminal is labeled with its equivalent root mean square(RMS) current value derived from the set of the simulated values at the terminal.

A. Width Determination for Electromigration and IR-Drop Avoidance

Given a connection, $T_i \rightarrow T_j$, between two terminals, T_i and T_j, based on the maximum tolerant current density, $J_{max}(T_{ref})$, in a given temperature, T_{ref}, the maximum current value, $I_{i,j}^{\max}$, and the minimum process width, w_{min}, the minimum width, $w_{i,j}^{c}$, of the given connection, $T_i \rightarrow T_j$, can be obtained to satisfy the electromigration constraint on the connection, $T_i \rightarrow T_j$, as

$$w_{i,j}^{c} = Max\{\frac{I_{i,j}.s}{d.J_{\max}(T_{ref})}, \frac{|I_{i,j}^{\max}|.s}{d.J_{peak}}, w_{\min}\},$$

where $I_{i,j}$ is the current value on the connection, $T_i \rightarrow T_j$, s is the safety factor, d is the thickness of the routing layer and J_{peak} is the layer-dependent peak current density. If the phenomenon of the peak current density is ignored, it is clear that $w_{i,j}^{c}$ is equal to w_{min} if $I_{i,j} \le \frac{w_{\min} \cdot d \cdot J_{\max}}{s}$ and $w_{i,j}^{c}$ is equal to $\frac{I_{i,j}.s}{d.J_{\max}}$ if $I_{i,j} > \frac{w_{\min} \cdot d \cdot J_{\max}}{s}$. On the other hand, the IR-drop, $V_i - V_j$, between the voltages, V_i and V_j, on the connection, T_i->T_j, must be constrained as IR-drop constraint to maintain the propagation quality of a signal net. It is assumed that $V_{IR}^{\max}$ is the maximum tolerant IR-drop voltage of the connection, $T_i \rightarrow T_j$. If the wiring resistance of the connection, $T_i \rightarrow T_j$, is considered to satisfy IR-drop constraint, the minimum width, $w_{i,j}^{r}$, of the connection, $T_i \rightarrow T_j$, with the current value, $I_{i,j}$, and the connection length, $L_{i,j}$, can be obtained as

$$w_{i,j}^{r} = I_{i,j}\frac{L_{i,j}r_0}{V_{IR}^{\max}},$$

where r_0 is the wiring resistance per unit square.

In order to simultaneously maintain the electromigration and IR-drop constraints on the connection, $T_i \rightarrow T_j$, the width, $w_{i,j}$, of the connection, $T_i \rightarrow T_j$, can be determined as $Max\{ w_{i,j}^{c}, w_{i,j}^{r} \}$. It is clear that $w_{i,j}$ is equal to $w_{i,j}^{c}$ if $L_{i,j} \le \frac{V_{IR}^{\max}.w_{i,j}^{c}}{I_{i,j}r_0}$ and $w_{i,j}$ is equal to $\frac{I_{i,j}L_{i,j}r_0}{V_{IR}^{\max}}$ if $L_{i,j} > \frac{V_{IR}^{\max}.w_{i,j}^{c}}{I_{i,j}r_0}$. Based on the width determination for electromigration constraint, the width, $w_{i,j}$, for electromigration and IR-drop constraints can be determined and divided into four different conditions as follows:

$$w_{i,j} = \begin{cases} w_{\min}, & if \quad I_{i,j} \le \frac{w_{\min} \cdot d \cdot J_{\max}}{s} \quad and \quad L_{i,j} \le \frac{V_{IR}^{\max}.w_{\min}}{I_{i,j}r_0} \\ \frac{I_{i,j}.L_{i,j}.r_0}{V_{IR}^{\max}}, & if \quad I_{i,j} \le \frac{w_{\min} \cdot d \cdot J_{\max}}{s} \quad and \quad L_{i,j} > \frac{V_{IR}^{\max}.w_{\min}}{I_{i,j}r_0} \\ \frac{I_{i,j}.s}{d.J_{\max}}, & if \quad I_{i,j} > \frac{w_{\min} \cdot d \cdot J_{\max}}{s} \quad and \quad L_{i,j} \le \frac{V_{IR}^{\max}s}{d \cdot J_{\max}r_0} \\ \frac{I_{i,j}.L_{i,j}.r_0}{V_{IR}^{\max}}, & if \quad I_{i,j} > \frac{w_{\min} \cdot d \cdot J_{\max}}{s} \quad and \quad L_{i,j} > \frac{V_{IR}^{\max}.s}{d \cdot J_{\max}r_0} \end{cases}.$$

According to the electromigration-constrained current, $\frac{w_{\min} \cdot d \cdot J_{\max}}{s}$, and IR-drop-constrained length, $\frac{V_{IR}^{\max}.w_{\min}}{I_{i,j}.r_0}$ or $\frac{V_{IR}^{\max}.w_{i,j}^{c}}{I_{i,j}.r_0}$ of the connection, $T_i \rightarrow T_j$, the 2D distribution of the determined width of the connection, $T_i \rightarrow T_j$, can be illustrated in Fig. 1.

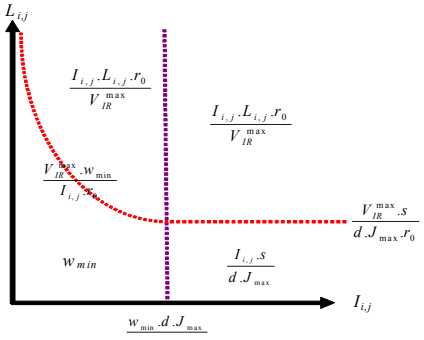

Fig. 1 2D distribution of the determined width for electromigration and IR-drop constraints

B. Problem Formulation

Given a set of n terminals, $\{T_1, T_2, \ldots, T_n\}$ including m current sources which is indicated by the negative RMS current values and *(n-m)* current sinks which is indicated by the positive RMS current values in a signal net, a set of r rectangular obstacles, $\{O_1, O_2, \ldots, O_r\}$, the maximum current density, J_{max}, the maximum IR-drop voltage, $V_{IR}^{\max}$, and the minimum wire width, w_{min}, based on the width determination of any current-driven connection for electro-migration and IR-drop avoidance, the problem is to construct an obstacle-aware multiple-source rectilinear Steiner tree to minimize the total wiring area of the signal net with satisfying the current flow under Kirchhoff's current laws and the electromigration and IR-drop constraints. Given a set of 7 terminals, $\{T_1, T_2, T_3, T_4, T_5, T_6, T_7\}$ including 3 current sources, T_1, T_4 and T_5, and 4 current sinks, T_2, T_3, T_6 and T_7, with a set of their equivalent RMS current values, {-7, +8, +4, -3, -9, +2, +5}, in a signal net, and a set of 3 rectangular obstacles, $\{O_1, O_2, O_3\}$ with the dimensions, 4x3, 3x3 and 3x2, in the locations, (2, 8), (6, 2) and (11, 8) as illustrated in Fig. 2(a). Based on the determined width for electromigration and IR-drop avoidance, an obstacle-aware multiple-source rectilinear Steiner tree is constructed to minimize the total wiring area with satisfying the current flow in Kirchhoff's current laws and the electromigration and IR-drop constraints as illustrated in Fig. 2(b) if it is assumed that the determined width for electromigration and IR-drop avoidance is obtained as

$$w_{i,j} = \begin{cases} 0.2 & if \quad I_{i,j} \le 2 \quad and \quad L_{i,j} \le \frac{20}{I_{i,j}.} \\ \frac{I_{i,j}.L_{i,j}}{100}, & if \quad I_{i,j} \le 2 \quad and \quad L_{i,j} > \frac{20}{I_{i,j}.} \\ \frac{I_{i,j}}{10}, & if \quad I_{i,j} > 2 \quad and \quad L_{i,j} \le 10 \\ \frac{I_{i,j}.L_{i,j}}{100}, & if \quad I_{i,j} > 2 \quad and \quad L_{i,j} > 10 \end{cases}.$$

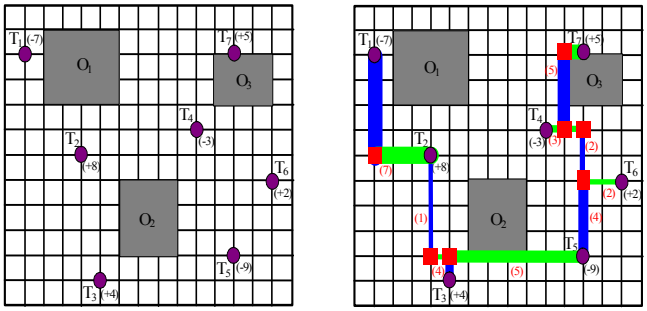

Fig. 2 Obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance

III. Obstacle-Aware Multiple-Source Steiner Tree with Electromigration and IR-Drop Avoidance

For a multiple-source signal in analog circuits, it becomes more important to consider the effect of the electromigration and IR-drop in the construction of a rectilinear Steiner tree. Based on the width determination for electromigration and IR-drop avoidance, an efficient approach is proposed to minimize the total wiring area in the multiple-source rectilinear Steiner tree and the proposed approach is divided into three phases: *Area-driven multiple-source routing tree with electromigration and IR-drop avoidance, Area-driven Steiner-point assignment under electromigration and IR-drop constraints* and *Obstacle-aware physical path assignment*.

A. Area-Driven Multiple-Source Routing Tree with Electromigration and IR-Drop Avoidance

Given a set of n terminals, $\{T_1, T_2, \ldots, T_n\}$, including m current sources which is indicated by the negative RMS current values and $(n\text{-}m)$ current sinks which is indicated by the positive RMS current values in a signal net and a set of r rectangular obstacles, $\{O_1, O_2, \ldots, O_r\}$, a routing tree must be constructed by building a set of two-endpoint connections, $T_i \rightarrow T_j$, from any current source, T_i, to any current sink, T_j, to satisfy the current requirement of all the current sinks in a signal net. Clearly, there are $(n\text{-}m)$ possible connections from any current source to all the current sinks and there are m possible connections from all the current sources to any current sink. For any possible connection, $T_i \rightarrow T_j$, the maximum available current value, $I_{i,j}$, can be obtained as $\text{Min}\{|I_i|, |I_j|\}$according to the providing current on T_i and the required current on T_j. To avoid the given obstacles in a routing plane, the obstacle-aware minimum distance, $L_{i,j}$, of the connection, $T_i \rightarrow T_j$, can be obtained by computing the length of the obstacle-aware shortest path between the terminals, T_i and T_j. Furthermore, the assigned width, $w_{i,j}$, of the connection, $T_i \rightarrow T_j$, can be obtained according to the maximum available current value, $I_{i,j}$, and the obstacle-aware minimum distance, $L_{i,j}$, of the connection, $T_i \rightarrow T_j$, for electromigration and IR-drop constraints.

Based on the obstacle-aware minimum distances and the assigned widths of all the $m(n\text{-}m)$ possible connections, an area-driven multiple-source routing tree with electromigration and IR-drop avoidance can be constructed to minimize the total wiring area by using an iterative selection approach[8] with the assignment of minimum-length zero-current connections. Refer to the routing specification including a set of 4 source terminals and 3 sink terminals, $\{T_1, T_2, T_3, T_4, T_5, T_6, T_7\}$, and a set of 3 obstacles, $\{O_1, O_2, O_3\}$, in Fig. 2(a), the weight value, $(L_{i,j}, w_{i,j})$, and the routing-area penalty, $p_{i,j}$, of any possible connection, $T_i \rightarrow T_j$, can be obtained in the iterative selection approach[8] and assigned on the connection, $T_i \rightarrow T_j$. After completing the selection process for all the 12 possible connections, an area-driven multiple-source routing tree with electromigration and IR-drop avoidance can be obtained and illustrated in Fig. 3. In the area-driven multiple-source routing tree, the pairs, $(L_{i,j}, w_{i,j})$, of the obstacle-aware minimum distance, $L_{i,j}$, and the assigned width, $w_{i,j}$, and the distributed current, $I_{i,j}$, of 6 selected connections are assigned and the final total wiring area is obtained as 15.0.

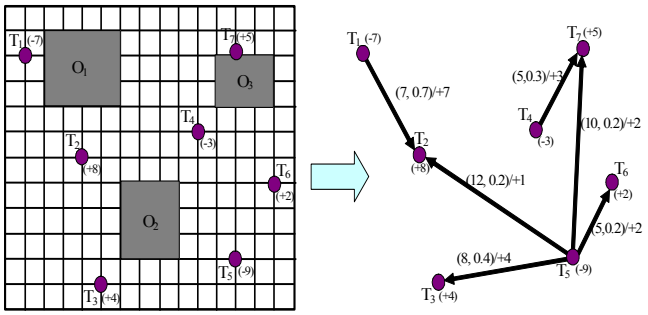

Fig. 3 Area-driven multiple-source routing tree with electromigration and IR-drop avoidance

B. Area-Driven Steiner-Point Assignment under Electromigration and IR-Drop Constraints

According to the geometrical feature for the construction of a Steiner point between two connections from the same source or to the same destination, two adjacent connections inside the same quadrant or in adjacent quadrants can be geometrically merged to form three smaller connections by introducing a necessary Steiner point. In the merging process of two connections from the same source, given two connections, $T_i \rightarrow T_j$ and $T_i \rightarrow T_k$, the Λ-type structure of the two connections in the same quadrant and adjacent quadrants can be transformed into the Y-type structure of three smaller connections, $T_i \rightarrow T_S$, $T_S \rightarrow T_j$ and $T_S \rightarrow T_k$, by introducing a Steiner point, S, as illustrated in Fig. 4(a) and Fig. 4(b), respectively. On the other hand, In the merging process of two connections to the same destination, given two connections, $T_j \rightarrow T_i$ and $T_k \rightarrow T_i$, the Λ-type structure of the two connections in the same quadrant and adjacent quadrants can be also transformed into the Y-type structure of three smaller connections, $T_j \rightarrow T_S$, $T_k \rightarrow T_S$ and $T_S \rightarrow T_i$, by introducing a Steiner point, S, as illustrated in Fig. 4(c) and Fig. 4(d), respectively.

Given a connection, $T_i \rightarrow T_j$, it is assumed that $I_{i,j}$ is the attached current value and $L_{i,j}$ is the Manhattan wirelength of the given connection. As mentioned above, the width, $w_{i,j}$, of the given connection can be assigned as a P-oriented width, w_{min}, a C-oriented width, $\frac{I_{i,j} \cdot s}{d \cdot J_{\max}}$, or a V-oriented width,

$\frac{I_{i,j}.L_{i,j}.r_0}{V_i - V_j}$, according to the attached current value and the Manhattan wirelength of the given connection. Furthermore, a given connection with the assigned P-oriented(C-oriented or V-oriented) width, the connection can be defined as a P-oriented(C-oriented or V-oriented) connection.

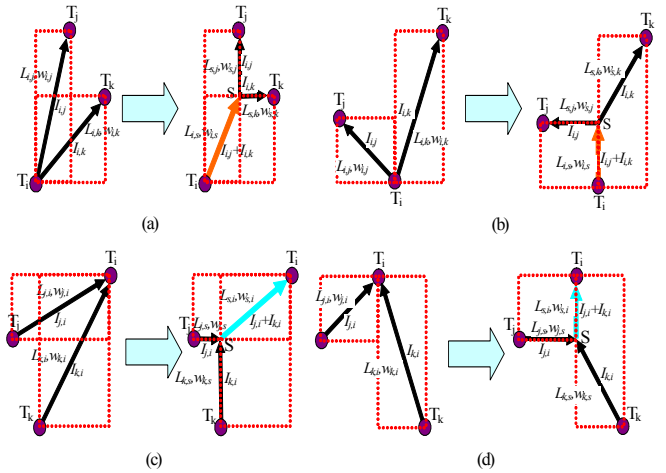

Fig. 4 Merging of two adjacent connections for Steiner-point assignment

Based on the width determination for electromigration and IR-drop avoidance, the C-oriented width is in proportion to the current value of the given connection and the V-oriented width is in proportion to the product of the current value and the wirelength of the given connection. As the current value of the given connection is smaller than the electromigration-constrained current, the resultant P-oriented connection uses more wiring area than the required electromigration-driven area to satisfy the width constraint in the design rules. On the other hand, as the wirelength of the given connection is longer than the IR-drop-constrained length, the resultant V-oriented connection also uses more wiring area than the required process-driven or electromigration-driven area to satisfy the IR-drop constraint. Hence, the merging process of two adjacent connections may reduce the wasted wiring area in any merged P-oriented or V-oriented connection.

For the merging process of two adjacent connections, $T_i \rightarrow T_j$ and $T_i \rightarrow T_k$, in Fig. 4(a) and Fig. 4(b), it is assumed that a Steiner point, S, is introduced, $L_{i,S}$ is the merged Manhattan wirelength from T_i to S, $L_{S,j}$ is the Manhattan wirelength from S to T_j and $L_{S,k}$ is the Manhattan wirelength from S to T_k. Based on the classification of three kinds of connections, P-oriented connections, C-oriented connections and V-oriented connections, the merging process of two adjacent connections can be divided into six different merging processes: P-P merging, P-C merging, C-C merging, P-V merging, C-V merging and V-V merging.

In P-P, P-C and C-C merging processes, it is further assumed that the width, $w_{S,j}$, of the connection, $S \rightarrow T_j$, is equal to the assigned width, $w_{i,j}$ of the connection, $T_i \rightarrow T_j$, and the width, $w_{S,k}$, of the connection, $S \rightarrow T_k$, is equal to the assigned width, $w_{i,k}$ of the connection, $T_i \rightarrow T_k$. Under the IR-drop constraint, the final width, $w_{i,S}$, of the merged connection, $T_i \rightarrow T_S$, in P-P, P-C or C-C merging process can be obtained as

$$w_{i,S} = \begin{cases} Max\{w_{\min}, \dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_{IR}^{\max} - V_S + Min\{V_j, V_k\}}\}, & if \quad (I_{i,j}+I_{i,k}) \le \dfrac{w_{\min}.dJ_{\max}}{s} \\ Max\{\dfrac{(I_{i,j}+I_{i,k})s}{dJ_{\max}}, \dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_{IR}^{\max} - V_S + Min\{V_j, V_k\}}\}, & if \quad (I_{i,j}+I_{i,k}) > \dfrac{w_{\min}.dJ_{\max}}{s} \end{cases}.$$

Furthermore, it is assumed that the connection, $T_i \rightarrow T_k$, in P-V or C-V merging process is a V-oriented connection and the width, $w_{S,j}$, of the connection, $S \rightarrow T_j$, is equal to the assigned width, $w_{i,j}$ of the connection, $T_i \rightarrow T_j$. In P-V or C-V merging process, the voltage, V_s, of the Steiner point, S, can be obtained as

$$V_S = V_j + I_{i,j}.\frac{(L_{i,j} - L_{i,S})r_0}{w_{i,j}}.$$

Based on the voltage, V_s, of the Steiner point, S, the final widths, $w_{i,S}$ and $w_{S,k}$, of the two connections, $T_i \rightarrow T_S$ and $T_S \rightarrow T_k$, in P-V or C-V merging process can be obtained as

$$w_{i,S} = \begin{cases} Max\{w_{\min}, \dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_i - V_j - I_{i,j}.\dfrac{(L_{i,j}-L_{i,S})r_0}{w_{i,j}}}\}, & if \quad (I_{i,j}+I_{i,k}) \le \dfrac{w_{\min}.dJ_{\max}}{s} \\ Max\{\dfrac{(I_{i,j}+I_{i,k})s}{dJ_{\max}}, \dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_i - V_j - I_{i,j}.\dfrac{(L_{i,j}-L_{i,S})r_0}{w_{i,j}}}\}, & if \quad (I_{i,j}+I_{i,k}) > \dfrac{w_{\min}.dJ_{\max}}{s} \end{cases}$$

and

$$w_{S,k} = \begin{cases} Max\{w_{\min}, \dfrac{I_{i,k}(L_{i,k}-L_{i,s})r_0}{V_j - V_i + V_{IR}^{\max} + I_{i,j}.\dfrac{(L_{i,j}-L_{i,S})r_0}{w_{i,j}}}\}, & if \quad I_{i,k} \le \dfrac{w_{\min}.dJ_{\max}}{s} \\ Max\{\dfrac{I_{i,k}.s}{dJ_{\max}}, \dfrac{I_{i,k}(L_{i,k}-L_{i,s})r_0}{V_j - V_i + V_{IR}^{\max} + I_{i,j}.\dfrac{(L_{i,j}-L_{i,S})r_0}{w_{i,j}}}\}, & if \quad I_{i,k} > \dfrac{w_{\min}.dJ_{\max}}{s} \end{cases}.$$

In V-V merging process, it is clear that the voltage of the terminals, T_j and T_k, in two V-oriented connections, $T_i \rightarrow T_j$ and $T_i \rightarrow T_k$, is (V_i- $V_{IR}^{\max}$). To minimize the total wiring area, $L_{i,S}w_{i,S} + (L_{i,j} - L_{i,S})w_{S,j} + (L_{i,k} - L_{i,S})w_{S,k}$, of the three connection, $T_i \rightarrow T_S$, $T_S \rightarrow T_j$ and $T_S \rightarrow T_k$, under the IR-drop constraint, the optimal voltage, V_s, of the Steiner point, S, can be obtained as

$$V_S = V_i - \frac{\sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2 + I_{i,k}(L_{i,k}-L_{i,s})^2} + \sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}.V_{IR}^{\max}.$$

Based on the optimal voltage, V_s, of the Steiner point, S, the final widths, $w_{i,S}$, $w_{S,j}$, and $w_{S,k}$, of the three connections, $T_i \rightarrow T_S$, $T_S \rightarrow T_j$ and $T_S \rightarrow T_k$, in V-V merging process can be obtained as

$$w_{i,S} = \begin{cases} Max\{w_{\min}, \dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2 + I_{i,k}(L_{i,k}-L_{i,s})^2} + \sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}{\sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}.\dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_{IR}^{\max}}\}, \\ \qquad if \quad (I_{i,j}+I_{i,k}) \le \dfrac{w_{\min}.dJ_{\max}}{s} \\ Max\{\dfrac{(I_{i,j}+I_{i,k})s}{dJ_{\max}(T_{ref})}, \dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2 + I_{i,k}(L_{i,k}-L_{i,s})^2} + \sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}{\sqrt{(I_{i,j}+I_{i,k})L_{i,s}^{\ 2}}}.\dfrac{(I_{i,j}+I_{i,k})L_{i,S}.r_0}{V_{IR}^{\max}}\}, \\ \qquad if \quad (I_{i,j}+I_{i,k}) > \dfrac{w_{\min}.dJ_{\max}}{s} \end{cases},$$

$$w_{S,j}=\begin{cases} Max\{w_{\min},\dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}+\sqrt{(I_{i,j}+I_{i,k})L_{i,s}}^2}{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2r_0+I_{i,k}(L_{i,k}-L_{i,s})^2}}\cdot\dfrac{I_{i,j}\cdot(L_{i,j}-L_{i,s})r_0}{V_{IR}^{\max}}\}, \\ \qquad\qquad if \quad I_{i,j}\le\dfrac{w_{\min}.d.J_{\max}}{s} \\ Max\{\dfrac{I_{i,j}.s}{d.J_{\max}(T_{ref})},\dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}+\sqrt{(I_{i,j}+I_{i,k})L_{i,s}}^2}{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2r_0+I_{i,k}(L_{i,k}-L_{i,s})^2}}\cdot\dfrac{I_{i,j}.(L_{i,j}-L_{i,s})r_0}{V_{IR}^{\max}}\}, \\ \qquad\qquad if \quad I_{i,j}>\dfrac{w_{\min}.d.J_{\max}}{s} \end{cases}$$

and

$$w_{S,k}=\begin{cases} Max\{w_{\min},\dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}+\sqrt{(I_{i,j}+I_{i,k})L_{i,s}}^2}{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}}\cdot\dfrac{I_{i,k}(L_{i,k}-L_{i,s})r_0}{V_{IR}^{\max}}\}, \\ \qquad\qquad if \quad I_{i,k}\le\dfrac{w_{\min}.d.J_{\max}}{s} \\ Max\{\dfrac{I_{i,k}.s}{d.J_{\max}(T_{ref})},\dfrac{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}+\sqrt{(I_{i,j}+I_{i,k})L_{i,s}}^2}{\sqrt{I_{i,j}(L_{i,j}-L_{i,s})^2+I_{i,k}(L_{i,k}-L_{i,s})^2}}\cdot\dfrac{I_{i,k}(L_{i,k}-L_{i,s})r_0}{V_{IR}^{\max}}\}, \\ \qquad\qquad if \quad I_{i,k}>\dfrac{w_{\min}.d.J_{\max}}{s} \end{cases}$$

For the merging process of two adjacent connections, $T_i \rightarrow T_j$ and $T_i \rightarrow T_k$, in Fig. 4(c) and Fig. 4(d), the widths of three merged connections in six different merging processes are also obtained according to the similar discussion under electromigration and IR-drop constraints.

Based on the determined widths of three resultant connections in the Y-type structure after completing any merging process, the wasted wiring area of the low-current P-oriented and V-oriented connections may be reduced in P-P, P-C, P-V, C-V or V-V merging process under the electromigration and IR-drop constraint. In order to reduce the total wiring area, the P-oriented connections can be firstly considered to be merged with their adjacent P-oriented or C-oriented connections. If any P-P or P-C merging process reduces the wasted wiring area, the feasible Steiner points will be assigned in the construction of an area-driven multiple-source Steiner tree. As no P-P or P-C merging process reduces the wasted wiring area, the V-oriented connections can be further considered to be merged with their adjacent P-oriented, C-oriented and V-oriented connections. If any P-V, C-V or V-V merging process reduces the total wiring area, the feasible Steiner points will be further assigned in the construction of an area-driven multiple-source Steiner tree. As no P-V, C-V or V-V merging process reduces the wasted wiring area, the C-oriented connections can be further considered to be merged with their adjacent C-oriented connections. Generally speaking, any C-C merging process cannot reduce the total wiring area under the electromigration and IR-drop constraint. However, any C-C merging process can reduce the total wirelength. If any C-C merging process does not increase the total wiring area, the feasible Steiner points will be further assigned in the construction of an area-driven multiple-source Steiner tree.

Refer to the area-driven multiple-source routing tree in Fig. 3, firstly, the P-oriented connection, $T_5 \rightarrow T_2$, can be merged with its adjacent C-oriented connection, $T_5 \rightarrow T_3$, to reduce the wasted wiring area. The Λ-type structure of two connections, $T_5 \rightarrow T_2$ and $T_5 \rightarrow T_3$, can be transformed into the Y-type structure of three connections, $T_5 \rightarrow T_{S1}$, $T_{S1} \rightarrow T_2$ and $T_{S1} \rightarrow T_3$, by introducing a Steiner tree, S_1. Next, the C-oriented connection, $T_5 \rightarrow T_6$, can be merged with its adjacent V-oriented connection, $T_5 \rightarrow T_7$, to reduce the total wirelength. The Λ-type structure of two connections, $T_5 \rightarrow T_6$ and $T_5 \rightarrow T_7$, can be transformed into the Y-type structure of three connections, $T_5 \rightarrow T_{S2}$, $T_{S2} \rightarrow T_6$ and $T_{S2} \rightarrow T_7$, by introducing a Steiner tree, S_2. Finally, the C-oriented connection, $T_4 \rightarrow T_7$, can be merged with the V-oriented connection, $T_{S2} \rightarrow T_7$, to reduce the total wirelength. The Λ-type structure of two connections, $T_4 \rightarrow T_7$ and $T_{S2} \rightarrow T_7$, can be transformed into the Y-type structure of three connections, $T_4 \rightarrow T_{S3}$, $T_{S2} \rightarrow T_{S3}$ and $T_{S3} \rightarrow T_7$, by introducing a Steiner tree, S_3. After completing three merging processes, the total wiring area of the final area-driven Steiner tree in Fig. 5 is obtained as 14.3.

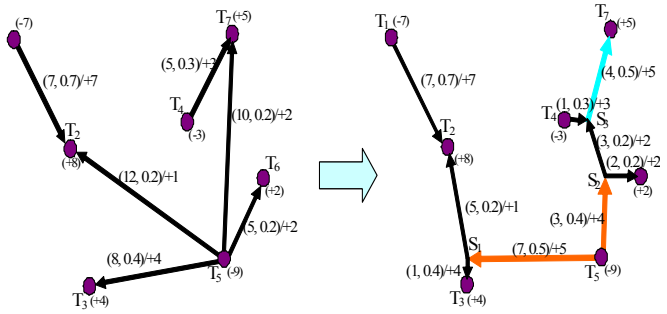

Fig. 5 Steiner-point assignment under electromigration and IR-drop constraint

C. Obstacle-aware Physical Path Assignment

After completing area-driven Steiner-point assignment, a final area-driven multiple-source Steiner tree is constructed by introducing some Steiner points into the initial routing tree. In general, all the connections are independent in a multiple-source Steiner tree. Based on the determined widths of all the connections and the given obstacles in a routing plane, the empty space among obstacles can be partitioned into some rectangular space regions and the physical paths of all the connections in the Steiner tree can be routed one by one by finding the shortest paths among space regions and assigning some I-type, L-type or Z-type routing patterns onto space regions. Furthermore, the widths of all the connections can be assigned onto the corresponding physical paths in obstacle-aware physical path assignment and an obstacle-aware multiple-source rectilinear Steiner tree can be obtained. Refer to the determined widths of all the connections in the Steiner tree in Fig. 5, an obstacle-aware multiple-source rectilinear Steiner tree can be obtained to minimize the total wiring area as illustrated in Fig. 6. As a result, the total wirelength in the final rectilinear Steiner tree is 33, the number of routed vias is 7 in two-layer routing model and the number of used Steiner points is 3.

IV. EXPERIMENTAL RESULTS

For the construction of an obstacle-aware multiple-source rectilinear Steiner tree, Lienig's Steiner-tree-based approach[7] and our proposed approach have been implemented by using standard C++ language and run on a Pentium IV 2.8GHz machine with 2GB memory. The set of useful parameters in

the with determination for electromigration and IR-drop avoidance is based on 0.18μm technology in the SIA'97 roadmap and listed in Table I.

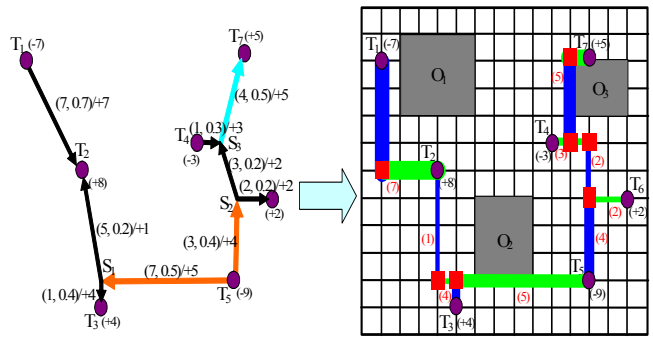

Fig. 6 Physical path assignment for the construction of an obstacle-aware multiple-source rectilinear Steiner tree

TABLE I PARAMETERS ON 0.18UM TECHNOLOGY IN SIA'97

Symbol	Description	Value
r_0	Wiring resistance per unit square	0.068(Ω/□)
V_{dd}	Power voltage	1.8(V)
J_{max}	Maximum tolerant current density	8.2E05(A/cm^2)
d	Thickness on the routing layer	0.55(um)
s	Safety factor	1.1
w_{min}	Minimum process wiring width	0.22(um)

If the IR-drop constraint of any connection is set as $V_{IR}^{\max} = p * V_{dd}/100$, for the given power voltage, V_{dd}, the determined width, $w_{i,j}$, for electromigration and IR-drop avoidance can be obtained as

$$w_{i,j} = \begin{cases} 0.22, & \text{if } I_{i,j} \le 0.902 \text{ and } L_{i,j} \le \dfrac{58.234\,p}{I_{i,j}} \\ \dfrac{I_{i,j}.L_{i,j}}{264.7\,p}, & \text{if } I_{i,j} \le 0.902 \text{ and } L_{i,j} > \dfrac{58.234\,p}{I_{i,j}} \\ \dfrac{I_{i,j}}{4.1}, & \text{if } I_{i,j} > 0.902 \text{ and } L_{i,j} \le 64.5624\,p \\ \dfrac{I_{i,j}.L_{i,j}}{264.7\,p}, & \text{if } I_{i,j} > 0.902 \text{ and } L_{i,j} > 64.5624\,p \end{cases}.$$

In the following experiment, six tested signal nets, c01, c02, c03, c04, c05 and c06, are randomly generated in a 1000x1000 um^2 area and the attached currents on the terminals are set as the values generated from 1.5mA to 7.5mA. For the construction of an obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance, the experimental results in Lienig's Steiner-tree-based approach[7] and our proposed approach with 5%V_{dd} or 10%V_{dd} as IR-drop constraint are obtained and listed in Table II. Compared with Lienig's multiple-source Steiner tree[7], the experimental results show that our proposed approach without any IR-drop constraint can reduce 10.5% of the total wiring area for the tested examples in reasonable CPU time. Under 10%V_{dd} and 5%V_{dd} IR-drop constraints, the experimental results show that our proposed approach can satisfy 100% electromigration and IR-drop constraints and reduce 7.5% and 4.9% of the original total wiring area on the average for the tested examples in reasonable CPU time, respectively.

V. CONCLUSIONS

Based on the width determination of any current-driven connection for electromigration and IR-drop avoidance and a set of given obstacles in a routing plane, an obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance can be constructed to minimize the total wiring area.

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TABLE II EXPERIMENTAL RESULTS FOR OBSTACLE –AWARE RECTILINEAR STEINER TREE WITH ELECTROMIGRATION AND IR-DROP AVOIDANCE

Nets	*#Terminals*		*#Obstacles*	*Lienig's Rectilinear Steiner Tree[7] (No IR-drop constraint)*				*Our Proposed Steiner Tree*						
								No IR-drop constraint		*5%V_{dd} IR-drop constraint*			*10%V_{dd} IR-drop constraint*	
	#Sources	*#Sinks*		*Total Wiring Area(um^2)*	*#(Satisfied sinks) for p=5*	*#(Satisfied sinks) for p=10*	*CPU Time(s)*	*Total Wiring Area(um^2)*	*CPU Time(s)*	*Total Wiring Area(um^2)*	*#(Satisfied sinks) for p=5*	*CPU Time(s)*	*Total Wiring Area(um^2)*	*#(Satisfied sinks) for p=10*	*CPU Time(s)*
c01	*5*	*6*	*3*	*324.27(100%)*	*4(66.7%)*	*5(83.3%)*	*0.14*	*287.14(88.5%)*	*0.11*	*302.18(93.2%)*	*6(100%)*	*0.14*	*294.33(90.8%)*	*6(100%)*	*0.14*
c02	*10*	*8*	*4*	*383.56(100%)*	*6(75.0%)*	*7(87.5%)*	*0.26*	*342.32(89.2%)*	*0.21*	*362.31(94.5%)*	*8(100%)*	*0.26*	*354.76(92.5%)*	*8(100%)*	*0.26*
c03	*15*	*7*	*5*	*412.39(100%)*	*6(85.7%)*	*6(85.7%)*	*0.49*	*379.53(92.0%)*	*0.43*	*404.58(98.1%)*	*7(100%)*	*0.51*	*399.27(96.8%)*	*7(100%)*	*0.51*
c04	*20*	*11*	*6*	*529.07(100%)*	*8(72.7%)*	*9(81.8%)*	*0.83*	*461.36(87.2%)*	*0.78*	*497.47(94.0%)*	*11(100%)*	*0.93*	*483.69(91.4%)*	*11(100%)*	*0.93*
c05	*25*	*10*	*6*	*598.92(100%)*	*8(80.0%)*	*9(90.0%)*	*1.15*	*536.78(89.6%)*	*1.02*	*568.46(94.9%)*	*10(100%)*	*1.21*	*549.13(91.7%)*	*10(100%)*	*1.21*
c06	*30*	*12*	*7*	*684.27(100%)*	*9(75.0%)*	*10(83.3%)*	*1.42*	*617.39(90.2%)*	*1.29*	*652.92(95.4%)*	*12(100%)*	*1.52*	*631.63(92.3%)*	*12(100%)*	*1.52*
Total				*2932.48(100%)*	*41(75.9%)*	*46(85.2%)*	*4.29*	*2624.52(89.5%)*	*3.84*	*2787.92(95.1%)*	*54(100%)*	*4.57*	*2712.81(92.5%)*	*54(100%)*	*4.57*