An All-Digital Built-In Self-Test Technique for Transfer Function Characterization of RF PLLs

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***Abstract* — This paper presents an all-digital built-in self-test (BIST) technique for characterizing the error transfer function of RF PLLs. This BIST scheme, with on-chip stimulus synthesis and response analysis completely done in the digital domain, achieves high-accuracy characterization and is applicable to a wide range of PLL architectures. For the popular sigma-delta fractional-*N* RF PLLs, the added circuitry required for this BIST solution is all digital except a bang-bang phase-frequency detector (BB-PFD), which incurs an area of only 0.0001mm^2 for our implementation in a 65nm CMOS technology. The silicon characterization results at 3.6GHz reported by this BIST solution and by explicit measurement have a root-mean-square difference of 0.375dB only.**

***Index Terms* — BIST, PLL, frequency synthesizer, frequency modulator.**

I. Introduction

Phase-locked loops (PLL) are an essential element for frequency synthesis and modulation. A PLL's loop dynamics, which are best characterized by its closed-loop transfer function, affect the accuracy of the RF systems. In particular, the output spectrum of an RF transmitter is dependent upon its frequency synthesizer's phase noise, which is sensitive to the PLL's transfer function [1]. In addition, good matching between the pre-emphasis filter and the PLL's transfer function is necessary for assuring a low modulation phase error in low-cost direct frequency modulators [2]. As a result, detailed characterization of the PLL's transfer function is a crucial task for assuring the quality of an RF system.

Testing of an RF PLL is a challenging and costly task due to the PLL's mixed-signal and tight feedback nature, as well as the requirement for high-frequency, high-precision test equipments. Moreover, for low-cost transceivers, because the modulator is reused as the receiver-side synthesizer, direct loopback testing is not feasible without the aid of external test elements such as a delay line on the load board [3]. Conversely, built-in self-test (BIST) provides a low-cost solution for pre-shipment screening and manufacturing testing. In addition, the test circuitry can be reused for multiple post-silicon quality assurance tasks including characterization, validation, in-field testing, and post-deployment performance tuning [4].

The requirements of a practical BIST design for PLLs include: 1) a high test coverage for the BIST circuitry itself so that test accuracy can be guaranteed, 2) a low sensitivity to variations/noises/interferences and greater robustness than the PLL-under-test, and 3) all-digital test signal synthesis and analysis to facilitate on-chip computing and performance tuning. To meet these requirements, most of the BIST circuitry, if not all, should be digital, and thus synthesizable, more variation-tolerant, and digital-scan testable. Any analog test circuitry, if any, must be simple, small and has a high natural yield. It should be noted that the BIST technique for all-digital PLLs [5] cannot be used for charge-pump-based PLLs due to its need for high-resolution time-to-digital converters (TDCs). The on-chip jitter transfer function measurement technique proposed in [6] demands a test clock that is several times greater than the VCO's output frequency so it is not applicable to high-frequency RF PLLs. The effectiveness of the frequency characterization system described in [7] depends heavily upon the natural yield and the accuracy of the analog test circuitry that cannot be easily guaranteed.

This paper presents an all-digital BIST technique for characterizing the error transfer function of an RF PLL that incorporates a Type-I loop filter [8]. The BIST scheme, characterizing the device with respect to a generic linear model of the PLL, is applicable to a broad range of PLL architectures. For the popular sigma-delta fractional-*N* PLLs, the only full-custom unit added for supporting this BIST solution is a bang-bang phase-frequency detector (BB-PFD), which occupies an area of only 0.0001mm^2 in a 65nm technology and thus should have a high natural yield. All other BIST circuitry is digital, synthesizable from HDLs following a standard digital design methodology, and, thus, self-testable.

The rest of the paper is organized as follows. Section II presents the necessary background for the proposed BIST technique. The theoretical background and the application of our BIST scheme to a sigma-delta fraction-*N* PLL is presented in Section III. Section IV discusses the SNR enhancement techniques. The simulation and measurement results are presented in Section V and VI, respectively. Section VII concludes the paper.

II. Background

Figure 1 shows an s-domain linear model of a PLL, in which the error transfer function, $E(s)$, is defined as:

$$E(s)\big|_{s=j\omega} = \frac{\theta_e(s)}{\theta_i(s)} = \frac{sN}{sN + K_d F(s) K_{vco}} \qquad (1)$$

A PLL can be classified as either Type I or II according to the number of integrators in the loop. A Type-I PLL has one integrator, which is from the VCO, in the loop. A Type-II PLL has an additional integrator implemented in the loop filter. A Type-I PLL is often faster and has a larger phase

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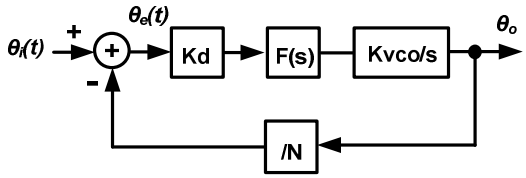

Figure 1: The s-domain linear model of a PLL.

margin than a Type-II PLL. In addition, due to requiring fewer capacitors, a Type-I PLL has a smaller silicon footprint than its Type-II counterpart. However, due to the lack of frequency tracking capability, a Type-I PLL introduces static phase error in response to a frequency difference between the reference and feedback signals that could result in undesirable idle tones at the PLL output. The response to a frequency step of a PLL is analyzed as follows.

Assume a frequency step $\Delta\omega t$ is applied at $\theta_i(t)$ which is equivalent to $\Delta\omega/s^2$ in the s-domain representation. According to Eq. (1), we can represent the corresponding phase error θ_e as:

$$\theta_e(s) = \frac{N\Delta\omega}{s(sN + K_d F(s) K_{vco})} \qquad (2)$$

The static phase error is the steady-state value of the phase error that can be evaluated using the final value theorem of the Laplace transform: [9]

$$\theta_{static} = \lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0} \frac{N\Delta\omega}{sN + K_d F(s) K_{vco}} = \frac{N\Delta\omega}{K_d F(0) K_{vco}} \qquad (3)$$

For a typical Type-II loop filter, $F(s)$ contains a pole in the denominator so it becomes infinite when s approaches zero. Therefore, for a Type-II loop filter, a frequency step will not result in any static phase error. For a Type-I loop filter, $F(0)$ is a constant. Since N, K_d, and K_{vco} are all constant values, the magnitude of the static phase error is proportional to the frequency step $\Delta\omega$.

Both Type-I and -II PLLs could be found in modern synthesizers [8] and modulators. It is possible to switch from Type II to Type I by disconnecting or disabling the integration capacitor [2, 4].

III. The Proposed BIST Scheme

A. Using DC Signal to Test AC Performances

Most RF circuit performances are specified in the power and frequency domains [11]. For example, the transfer function characterization of an RF circuit involves the application of a sinusoidal stimulus at different frequencies and measure its output response that often demands for high frequency signal analyzers or on-chip sensors. To facilitate a low-cost BIST, in the following, we propose a technique that utilizes a DC signal to test an AC signal's amplitude.

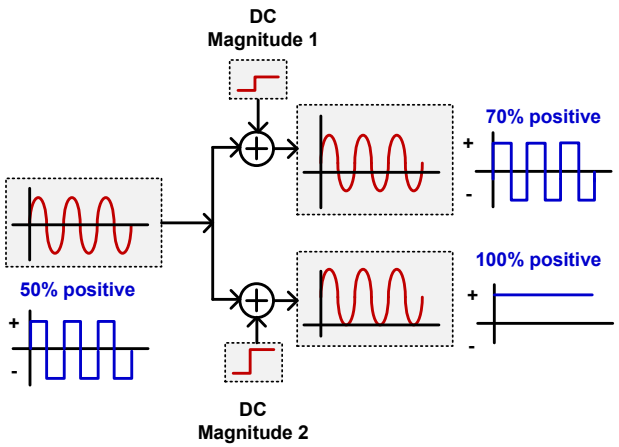

Figure 2: Adjusting the polarity of an AC signal with a DC level.

The AC signal's power can be further derived from the obtained amplitude information.

A single-tone AC signal centered at 0V has a 50% duty cycle, as shown in Figure 2. By adding a DC level to shift the mean of this AC signal, we could alter the periods of its positive and negative polarities. To test the amplitude of an AC signal, we can adjust the magnitude of the added DC level (i.e. shifting a different amount to the AC signal's mean) and simultaneously monitor the polarity of the AC signal. The amount of DC level added to result in a 100% positive polarity would be equal to the amplitude of the AC signal.

To successfully apply this test technique, we need (i) a digitally controllable mechanism to shift the mean of the AC signal, and (ii) a method to monitor the polarity of the AC signal. The accuracy of the test result depends on the granularity of the DC signal, the sampling frequency of the polarity monitor, and the purity of the AC signal.

To test the error transfer function of a Type-I PLL, requirement (i) can be fulfilled by introducing a frequency step to a loop that leads to a static phase error. Furthermore, requirement (ii) can be implemented with a negligible overhead. In Section III-B, we describe the operating principle of this BIST scheme for generic Type-I PLLs. In Section III-C, we present a specific implementation and design considerations for a sigma-delta factional-N PLL.

B. Operating Principle

$E(s)$ can be tested by applying an input signal $\theta_i(t)$ with a known amplitude and at a frequency ω_i to the PLL and measuring the corresponding magnitude of the phase error signal $\theta_e(t)$. This test process is repeated for multiple frequencies ω_i's, in the range of interest, for $\theta_i(t)$.

The time-varying phase error signal $\theta_e(t)$ is the phase difference between the input and the feedback signal. If $\theta_i(t)$ is a DC signal, $\theta_e(t)$ would be zero. If $\theta_i(t)$ is a sinusoidal signal, $\theta_e(t)$ fluctuates between positive and negative

polarities with an equal probability and with a magnitude $|\theta_e(t)|$, which can be measured by shifting the mean of $\theta_e(t)$ and monitoring the polarity of the shifted $\theta_e(t)$. By adding a static phase error, θ_{static}, to $\theta_e(t)$, $\theta_e(t)$'s mean will be shifted by θ_{static}, thereby altering the probability for the occurrence of $\theta_e(t)$'s positive and negative polarities. The minimum θ_{static} that results in a shifted $\theta_e(t)$ with a positive polarity only (or negative polarity only) would be the magnitude of the original $\theta_e(t)$.

As a Type-I PLL has only one integrator in the loop and, therefore, a finite DC gain, θ_{static} can be added by introducing an extra frequency step $\Delta\omega$ to the PLL. According to Eq. (3), the added static phase error can be calculated from the frequency step $\Delta\omega$ and the PLL's DC gain K_{DC}:

$$\theta_{static} = \frac{N\Delta\omega}{K_d F(0) K_{vco}} = \frac{\Delta\omega}{K_{DC}} \qquad (4)$$

Hence, the magnitude of the phase error $\theta_e(t)$ induced by $\theta_i(t)$ can be identified by finding the minimum amount of $\Delta\omega$ introduced such that the shifted $\theta_e(t)$ has a positive-only (or negative-only) polarity.

To summarize, the BIST scheme relies on three sub-tasks: 1) applying a known-amplitude $\theta_i(t)$ of different frequencies to the PLL, 2) introducing a $\Delta\omega$ to the PLL to shift the mean of $\theta_e(t)$, and 3) monitoring the polarity of the shifted $\theta_e(t)$.

In practice, $\theta_i(t)$ can be introduced to the PLL by digitally modulating the PLL from the divider through a sigma-delta modulator (SDM). Therefore, this BIST scheme does not require a high-precision, high-frequency external test clock. However, the SDM introduces high frequency quantization noise to $\theta_e(t)$. To mitigate this noise from the measurement of $\theta_e(t)$'s mean value, a low pass filter and a comparator, both of which are digital, are integrated to enhance the signal-to-noise ratio (SNR). In Section IV, we provide detailed analysis on the SNR enhancement techniques.

C. Implementation detail for sigma-delta fractional-N PLLs

Figure 3 illustrates the implementation of this BIST technique to a sigma-delta fractional-*N* PLL. First, a sine-wave signal, synthesized by a direct digital frequency synthesis (DDS) unit followed by a sigma-delta modulator (SDM), is applied to the PLL as $\theta_i(t)$. The frequency of $\theta_i(t)$ can be varied and swept by adjusting the frequency control word (FCW) applied to the DDS. The amplitude of $\theta_i(t)$ is set to its maximum allowable value to maximize the SNR.

The frequency step $\Delta\omega$ used for shifting $\theta_e(t)$ is introduced by adding a constant, through an up-down counter, to the SDM's fractional code. The added fractional code Δm introduces a frequency step $\Delta\omega$ based on the following relationship:

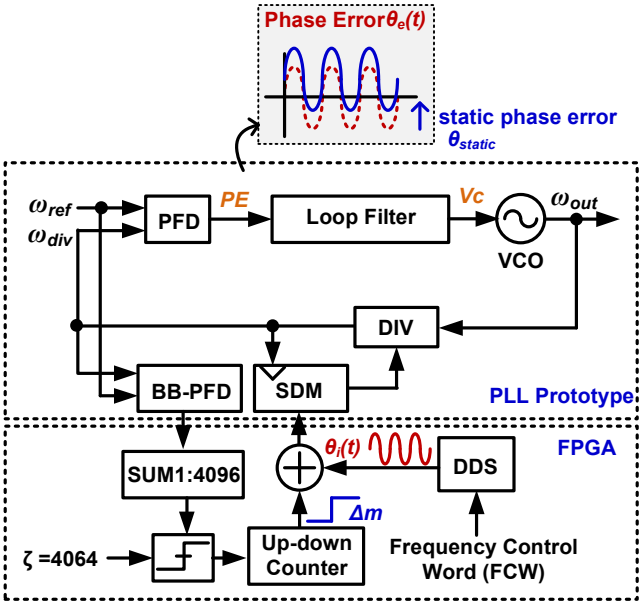

Figure 3: Architecture of the proposed BIST technique for a sigma-delta fractional-*N* PLL.

$$\Delta\omega = \frac{\omega_{ref}}{M} \times \Delta m\ , \qquad (5)$$

where M is the maximum fractional code. Combining Eqs (4) and (5), the amount of θ_{static} introduced to the loop is equal to the added fractional code Δm multiplied by a constant β:

$$\theta_{static} = \frac{\omega_{ref}}{K_{DC} M} \times \Delta m = \beta \times \Delta m \qquad (6)$$

Note that, to identify the magnitude of $\theta_e(t)$, it is not really necessary to derive β of the PLL-under-test. Based on the fact that $E(s)$ approaches 1 as the input frequency approaches infinity, $\theta_e(t)$'s magnitude at each input frequency f can actually be found by simply normalizing the fractional code obtained at f with respect to that obtained at a sufficiently high frequency.

As a result, the error transfer function of the PLL-under-test can be expressed in terms of Δm at each θ_i:

$$E(f) = \frac{\theta_e(f)}{\theta_i(f)} \approx \frac{\theta_{static}(f)}{\theta_i(f)} \propto \frac{\Delta m(f)}{\theta_i(f)} \qquad (7)$$

A BB-PFD, depicted in Figure 4, can be used to monitor the polarity of the shifted $\theta_e(t)$. Consisting of two cross-coupled latches, its symmetric topology minimizes the mismatch between the reference and the feedback path. The BB-PFD reports a phase lead or lag of the reference with respect to the feedback signal, which corresponds to a positive or negative phase error, respectively.

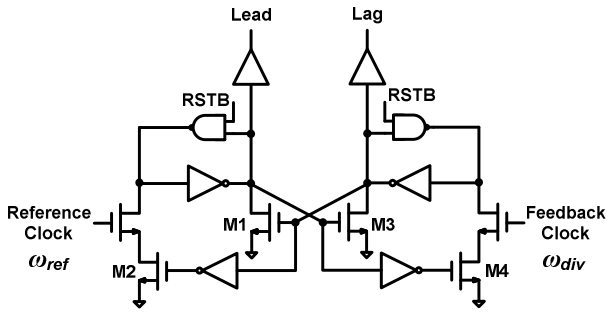

Figure 4: Schematic of a bang-bang phase frequency detector (BB-PFD).

As shown in Figure 3, the BB-PFD's output is connected to a summer (SUM1:4096), which is a running-sum low-pass filter (LPF) that helps mitigate the effect of the SDM's quantization noise. The summer's output is compared with a threshold ζ to detect if the accumulated phase lead exceeds a constant. The threshold ζ is set to 4064 in our implementation, instead of 4096, to tolerate some high-frequency transitions at the BB-PFD output due to the quantization noise. The output of the comparator drives the up-down counter that updates the fractional code.

IV. SNR Enhancement Techniques

Implemented in the digital domain, the SDM used in a fraction-N PLL is often constructed in a MASH structure for its simplicity. The transfer function of a α-order MASH SDM with input $x[k]$, output $y[k]$, and quantization noise $n[k]$ can be expressed as:

$$y(z) = x(z) - (1 - z^{-1})^{\alpha} n(z) \qquad (7)$$

Ideally, n[k] is white and has a flat spectrum with a magnitude of 1/12 [10]. According to Eq. (7), the noise transfer function (NTF) of the SDM has a high pass characteristic. As a result, the SDM passes the input signal and shapes the quantization noise to higher frequencies depending on the order α. The shaped noise can be attenuated by the loop filter to enhance the fidelity of the PLL output, but the noise would directly pass on, without filtering, to the PFD output and degrade the SNR. In a conventional PFD, the phase error is proportional to the input phase difference. In the case of a BB-PFD, the phase error is either 1 or 0 which corresponds to a phase lead or lag, regardless of the amount of the input phase difference.

The BB-PFD is used as a polarity monitor, the output of which is 1 and 0 for positive and negative polarities respectively. As illustrated in Figure 2, the mean of a sufficient number of samples would be 0.7, 0.5, and 1 respectively for the cases of 70%, 50%, and 100% positive polarities. Therefore, we can simply monitor the mean of the BB-PFD output for a sufficient number of samples to determine if the polarity of the phase error has been shifted to become 100% positive (or 100% negative).

A running-sum filter (RSF), which is one of the simplest finite-impulse-response (FIR) LPFs, is used to accurately retrieve the DC component (i.e., mean) of the BB-PFD output. In the frequency domain, an r-point RSF has the following two properties:

1) The DC gain is r.
2) The nulls occurs at $f = \pm(k/r) \times f_s$, where k is an integer and f_s is the sampling frequency in Hz.

An r-point RSF is equivalent to taking the sum of the BB-PFD output for r samples. Therefore, the RSF output correlates well with the mean of the phase error. In addition, the low-pass characteristics of an RSF help attenuate the high-frequency noise from the SDM. The attenuated high-frequency noise can be further reduced by setting a proper threshold ζ to the comparator following the RSF.

In the time domain, an r-point RSF, input $x[k]$, and output $y[k]$ has the following property.

$$y[n] = \sum_{m=0}^{r-1} x[n-m]$$
$$= x[n] + x[n-1] + \cdots + x[n-r+1]$$

When the output of the BB-PFD has an equal opportunity of a phase lead and lag, the RSF output is close to $r/2$ because there are 50% of 1s and 0s in every r samples. Similarly, when the BB-PFD output is mostly 100% 1s (0s), the RSF output would be close to r (0).The introduction of a static phase error through the increment of Δm shifts the mean of the phase error and, in turn, changes the 1/0 distribution of the BB-PFD output and the DC level of the RSF output.

Due to high-frequency noise, the BB-PFD output could still fluctuate between 1 and 0 even when the polarity of the phase error should ideally be all positive (or all negative). Since the high-frequency noise has been attenuated, the noise should have a small magnitude. Therefore, the RSF output is compared to a threshold ζ, instead of r, using a comparator which could more accurately determine if the shifted phase error signal is 100% positive (or negative).

A larger r usually results in a greater SNR but would incur a greater hardware complexity. The ζ is another implementation parameter. In our implementation, both r and ζ are determined based on simulation results that will be presented in Section V-B.

V. Simulation Results And Analysis

A. Time Domain Simulation Results

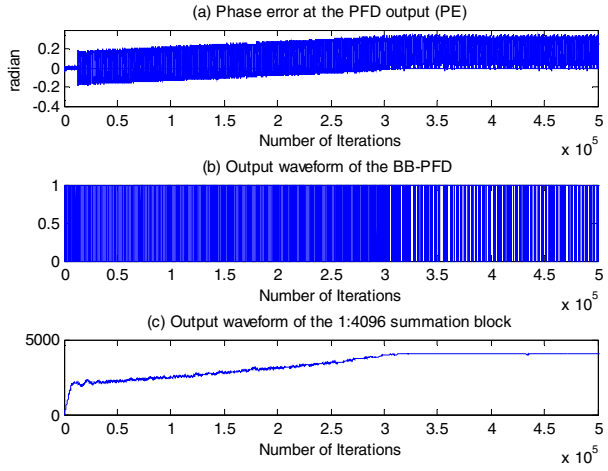

Figure 5: Numerical simulation results for the BIST scheme.

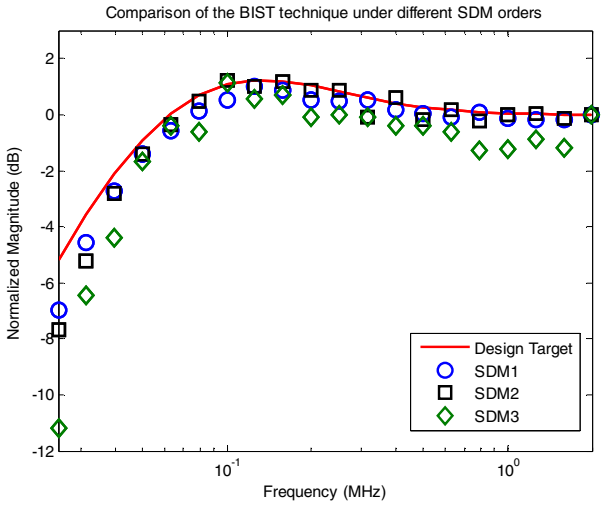

Figure 6: Simulated transfer function characterization results for the first-, second- and third-order SDMs.

Figure 5 shows some simulation results illustrating the output waveforms of key building blocks. Figure 5(a) shows the phase error at the PFD output induced by a sinusoidal input signal θ_i(t). Through the addition of the fractional code from the up-down counter, θ_{static} introduced to the loop increases, which, in turn, shifts the mean of the sinusoidal $\theta_e(t)$. Figure 5(b) shows that the BB-PFD output fluctuates between a phase lead (1) and a lag (0), that correspond to the phase error's polarity. Note that due to the SDM's quantization noise, the BB-PFD output continues to fluctuate between phase lead and lag even after $\theta_e(t)$'s polarity becomes mostly positive. As shown in Figure 5(c), the summer filters out high-frequency transitions and generates an output that reflects the mean of the phase error.

B. Choosing SDM order and ζ

The accuracy of the BIST result depends on the order of the SDM, the running length of the summer block, and the threshold ζ.

Figure 6 shows the simulation results of the BIST scheme using first-, second-, and third-order SDMs. The root-mean-square (rms) errors, compared to the design target, at 20 equally-spaced frequencies from 0.025MHz to 2MHz, are 0.57dB, 0.74dB, and 1.77dB respectively. The frequency range where the transfer function has a magnitude greater than 0dB – from 0.06MHz to 0.6MHz in Figure 6 – amplifies phase noise and, thus, should be the primary focus. For this frequency range only, the rms errors are 0.40dB, 0.30dB, and 0.79dB respectively. Although the rms errors of first and second-order SDMs are similar, the amount of spurious tones introduced by a second-order SDM is much less than that introduced by a first-order SDM. Therefore, a second-order SDM is chosen for implementation in our silicon prototype. The choice of SDM order does not affect the transfer function of the PLL-under-test.

Figure 7(a)(b) depicts the simulation results for the BIST scheme using different numbers of taps for the summer block and different thresholds for the 0.02-20MHz and 0.06-0.6MHz frequency ranges, respectively. The x-axis represents the threshold value, defined as the difference between the tap count and ζ. The y-axis illustrates the rms errors, and each curve represents the result for a specific tap count for the summer block. The results indicate that those tap counts greater than 2^{11} yield a smaller rms error for both frequency ranges. Among them, a tap count of 2^{12}, or 4096, is a preferred choice for implementation due to its lower

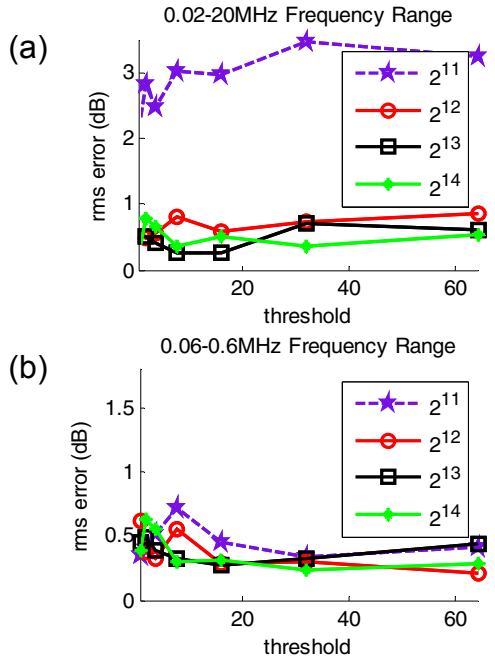

Figure 7: Simulation results under various tap counts and threshold values.

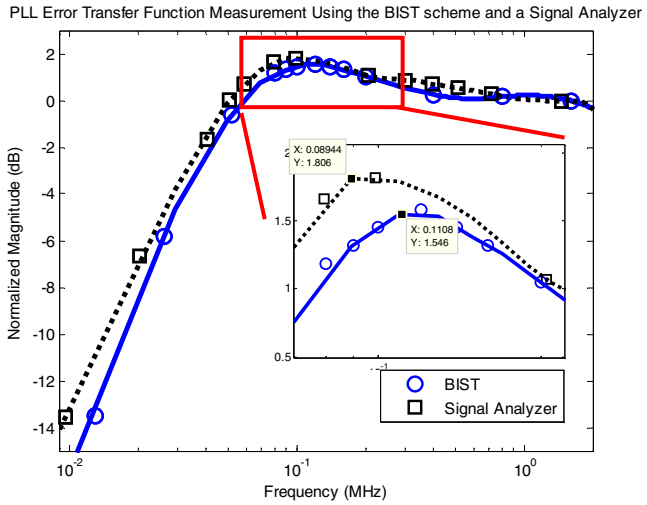

Figure 8: Measurement results obtained from the BIST scheme and from a signal analyzer.

hardware requirement. We chose a threshold of 32 in our implementation, which achieves a small rms error for both frequency ranges, resulting in the choice of 4064 for ζ.

C. Test time Analysis

The larger the amplitude of $\theta_i(t)$ and the smaller the step size for each Δm increment, the longer the time required for reaching convergence. When the step size is set to 1, all the test cases converged within 40,000 iterations, which corresponds to a convergence time of 1.54 msec given a 26MHz reference frequency. Increasing the step size reduces the test time but also reduces SNR. Conversely, a gear shifting algorithm similar to that described in [4] can be incorporated for reducing the test time while maintaining a fine test resolution.

VI. Measurement Result

The BIST scheme in Figure 3 was further evaluated with a silicon prototype fabricated in a 65nm CMOS technology, along with the digital test circuitry implemented in an FPGA. Figure 8 depicts the PLL transfer function measured at 3.6 GHz output frequency by the BIST scheme and by a signal analyzer, the curve fitting of which was based on a piecewise cubic spline interpolation function in MATLAB. Comparing the BIST results and the measurement results captured by a signal analyzer, their rms difference at 20 equally-spaced frequencies between 0.025MHz and 2MHz is 0.353dB, and that between 0.06MHz and 0.6MHz is 0.375dB only. The offsets of the peak frequency and the maximum magnitude of the transfer function between these two measurements are 21KHz and 0.26dB respectively. Figure 9 shows the die micrograph.

VII. Conclusion

This paper presents a BIST technique for characterizing the error transfer function of Type-I PLLs. The proposed BIST technique enables testing the AC performance using DC signals only. The measurement results validate that the proposed BIST technique offers a robust, accurate, and practical solution to characterizing the error transfer function of an RF PLL.

Acknowledgments

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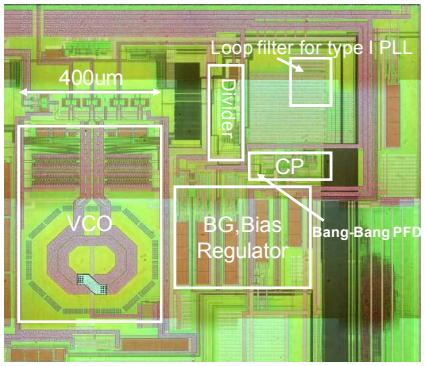

Figure 9: Die micrograph of the test chip that follows the BIST architecture in Figure 3, excluding the digital BIST circuitry which is implemented in an FPGA.