Beyond UPF & CPF: Low-Power Design and Verification

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Abstract—**Two formats for specifying power intent are currently in wide use in the industry today and as designers continue to strive for more power efficient designs new issues arise that need new solutions to improve on today's standards. This panel will discuss areas for improving today's power formats and the direction that these formats need to move, in order to provide the most efficient flows for design and verification and especially with regards to low-power. The scope of the formats and their suitability from early ESL design exploration to back-end sign-off checking will also be discussed.**

Keywords-component; Unified Power Format; UPF; Common Power Format; CPF; Low-Power; Power-Aware; Power-Efficient; Design; Verification

BIOGRAPHIES:

John Biggs has been involved with ARM developments since 1986 and co-founded ARM Ltd. in 1990. After a number of years working as a VLSI design engineer he went on to form ARM's Design Methodology Group in 1995. Biggs currently works as a Consultant Engineer in ARM's research group focusing on the development of advanced methodologies for the low-power deployment of synthesizable ARM IP. John represents ARM in the IEEE 1801 working group for the UPF standard.

Christophe Clavel joined ST 11 years ago, as a System Level design engineer using CoWare. After 3 years, Christophe moved to System Level Verification, and until now, has participated in the verification of several Nomadik family chips, starting from the early days prototype, the 8800, then the 8810, 8815 (as an object leader), 8820 & 8500 (as the verification platform object leader). He is now in charge of the central verification methodology team for STEricsson, dealing with both the IPs & the SOC level. He's also focusing on the LP verification, using an internal test chip that features all of the 32 nm LP constructs that will be part of the next generation SOCs. This test chip is being used as a test vehicle for the introduction of UPF2.0 primitives & tools evaluations.

Olivier Domerego received the M.S. degree in digital signal processing and electronics and the M.S degree in digital communication from Nice Sophia Antipolis University in 2001 and 2002, respectively. He has worked at Texas Instruments for the last 8 years in Wireless EDA/Methodology. He is an expert in verification, especially on power management verification. His interests include power management techniques, design automation, and low power designs.

Knut Just received his PhD in electrical engineering from the Technical University of Munich, Germany, before he joined Siemens Semiconductors (now Infineon Technologies) in 1987. He was with the CAD department until 1995, being responsible for FE-Tools for logic synthesis und test. Then, he joined the "Wireless Solutions" Business Group as project manager for development of chips for GSM baseband, GPS, and Wireless-LAN. From 2001 until 2003 he was project manager for the Infineon "Low Power/Low Voltage" project for the 90nm technology node where the team developed low power features in the fields of: technology, cell libraries, memories, and design architectures. Since 2002 he's been in the Digital Design Methodology and Implementation Group, responsible for low power methodologies development and implementation in the RTL2GDS design flow. Since 2009 he is the Infineon representative in the IEEE 1801 working group for UPF 2.0 definition.

Barry Pangrle is a Solutions Architect in the Engineered Solutions Group at Mentor Graphics Corporation focusing on energy efficient design and verification. He received a B.S. in Computer Engineering and a Ph.D. in Computer Science, both from the University of Illinois at Urbana-Champaign. Barry has previously worked at Synopsys as an R&D Director for power optimization and analysis tools. He was also the Director of design methodology for a fabless semiconductor company, Clearwater Networks, and has focused on design automation for low power/energy designs. He has published over 25 reviewed works in high level design automation and low power design and served as a Technical Program Co-chair for the 2008 and a General Co-Chair for the 2010 ACM/IEEE International Symposium on Low Power Electronics Design (ISLPED).

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