Logic Synthesis and Physical Design: Quo Vadis?

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Virtually all current integrated circuits and systems would not exist without the use of logic synthesis and physical design tools. These design technologies were developed in the last fifty years and it is hard to say if they have come to full maturity. Physical design evolved from methods used for *printed-circuit boards*, where the classic problems of *placement and routing* surfaced for the first time [1]. Logic synthesis evolved in a different trajectory, starting from the classic works on switching theory [2], but took a sharp turn in the eighties when multi-level logic synthesis, coupled to semicustom technologies, provided designers with a means to map models in *hardware description languages* into netlists ready for physical design [3],[4]. The clear separation between logic and physical design tasks enabled the development of effective design tool flows, where signoff could be done at the netlist level. Nevertheless, the relentless downscaling of semiconductor technologies forced this separation to disappear, once circuit delays became interconnect-dominated. Since the nineties, design flows combined logic and physical design tools to address the so-called *timing closure* problem, i.e., to reduce the designer effort to synthesize a design that satisfies all timing constraints. Despite many efforts in various directions, most notably with the use of the *fixed timing* methodology, this problem is not completely solved yet. The complexity of integrated logic and physical tool flows, as well as the decrease in *design starts* of large ASICs, limits the development of these flows to a few EDA companies.

Open questions relate to how tools will address future technologies, where the downscaling beyond the 32nm node may lead to non-planar devices and to strong restrictions on layout geometries [5]. Indeed manufacturing considerations influence strongly physical design, thus making the overall tool chains even more complex. We expect a few foundries to provide manufacturing for deeply-scaled CMOS, essentially with 3-dimensional devices and a full range of new materials to provide insulation and interconnect. We also expect to use new technologies, such as *silicon nanowires* (SiNW), *carbon nanotubes* (CNTs), *molecular electronics* (ME) and *phase-change* storage materials. We also expect *3-dimensional* (3D) integration to appear quite soon in a variety of products. These emerging technologies will force a departure from standard design flows for two reasons: variability of nano-devices and the need to control wiring-length tightly. For example, CNT transistors suffer from variability in the directionality of the tubes themselves [6] and thus new design rules and styles have to cope with the elimination of possible sneak paths. SiNW and CNT devices may be designed to show ambipolarity, i.e., electrically-controlled polarity of the logic switches. This feature enables the design of new libraries and new mapping rules that take advantage of the intrinsic binateness of the logic gates [7]. Moreover, the corresponding physical layout of these ambipolar gates supports a regular design fabric, with a corresponding better control on the spread of wiring lengths. Circuit crossbars with SiNW and ME technologies have been realized for both computation and storage. These rectangular macro-cells, reminiscent of *programmable logic arrays* (PLAs), are highly structured, inherently more resilient to wiring delay spreads, and supporting fault tolerance schemes. Module generators for this design style combine logic and physical design tools.

3D integration technologies require solving new physical design problems, such as 3-D partitioning, placement and routing, as well as buffer insertion and *through silicon via* (TSV) positioning. Native 3D integration technologies, such as those that support vertical transistor stacking, require a full new set of physical design tools. Indeed logic cells are designed on two layers [8], increasing the device density and decreasing the local interconnect length. For multi-core *systems on chips* (SoCs), *network on chip* (NoCs) technology provides the ultimate evolution of combined logic and physical design [9]. NoCs will be especially instrumental in realizing 3D systems, and supporting modular, flexible and reprogrammable interconnection schemes.

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