Towards a Chip Level Reliability Simulator for Copper/Low-k Backend Processes

Muhammad Bashir and Linda Milor
School of Electrical and Computer Engineering, Georgia Institute of Technology

Abstract

A framework is proposed to analyze circuit layout geometries to predict chip lifetime due to low-k time-dependent dielectric breakdown (TDDB). The methodology uses as inputs data from test structures, which have been designed and fabricated to detect the impact of area and metal linewidth on low-k TDDB.

I. Introduction

Copper/Low-k interconnects have proven to be the solution of choice to overcome issues raised by wire delays and dynamic power consumption in the deep submicron and nanometer regime. However, Cu/low-k interconnect systems are vulnerable to breakdown because of the nature of the materials and the complexity of the manufacturing process.

Some of the factors affecting breakdown are the lower breakdown field strengths of porous low-k materials, the susceptibility of low-k materials to mechanical damage by chemical mechanical polishing (CMP), and the high susceptibility of low-k materials to Cu drift. Consequently, time-dependent dielectric breakdown (TDDB) of damascene structures has to be assessed as a system of a dielectric, diffusion barrier, cap layer (SiC, for example), and Cu interconnect. This system is shown in Figure 1.

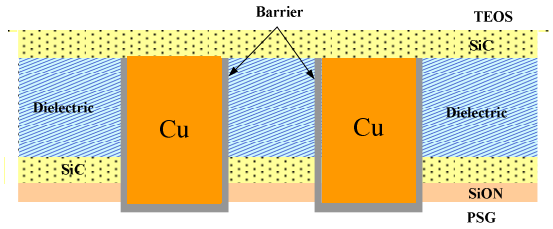

Fig. 1. Cross-section of a Cu/low-k interconnect system, including the barrier and capping layers.

This paper aims to account for low-k dielectric breakdown, measured in test structures, to predict full chip lifetime.

This paper is organized as follows. In the next section, we discuss low-k dielectric breakdown physics and chip scale reliability simulators. In the following section, we formulate the problem and propose the methodology that will be used. Section 4 describes our test structures. Section 5 summarizes the data obtained from our test structures and the breakdown models for target layout features. Section 6 demonstrates how to use existing models and data to predict chip lifetimes. Section 7 discusses issues with our approach and conclusions.

II. Full Chip Reliability Analysis

A. Low-k Breakdown Mechanisms

Several competing theories have been around for some time and appear to model TDDB equally well. The dominant models are the "E Model", based on dipolar interactions [1], and the "$\sqrt{E}$ Model," based on Cu diffusion [2]. These models are concerned with linking lifetimes at high temperatures and voltages to lifetimes at operating conditions. Similarly, the effect of different conductor geometries on low-k TDDB has been the subject of various studies, such as [3],[4].

The physics behind existing models cannot be easily extended to circuits. This is because lifetime is assumed to depend on only one circuit parameter. For instance, according to the E model,

$$TF = A_0 \exp\left((\Delta H_0 - \rho_{eff} E)/k_B T\right). \quad (1)$$

where TF is the time-to-breakdown, A_0 is a material constant, ΔH_0 is zero-field activation energy and depends on the properties of the dielectric, k_B is Boltzmann's constant, and ρ_{eff} is the effective dipole moment and depends on the chemical composition of the dielectric. In (1), only temperature, T, and electric field, E, affect lifetime. If we assume that electric field and temperature distributions are unrelated, then these models would require the electric field intensity at the chip level. Such an analysis would require the finite element method to simulate the behavior of electric field in a chip, the computation of its average, together with a temperature profile simulator to compute the average temperature.

Other models fare no better. In general, all models are of the form,

$$TF = k_1 \exp\left(\gamma E^m\right) \quad (2)$$

where k_1 is a constant that depends on the material properties of the low-k dielectric, γ is a field acceleration factor that incorporates an inverse dependence on temperature, $m=1$ for the E model, and $m=1/2$ for the $\sqrt{E}$ model.

B. Chip Scale Reliability Simulators

There are both industrial (FAMMOS by Synopsys) and academic [5]-[7] simulators to assess reliability. However, most do not deal with the backend of the process. Moreover, those that deal with the backend of the process are limited to wearout caused by electromigration and do not take into account the effect of the dielectric on reliability [5]. Hence, there are no tools to predict the impact of low-k TDDB on lifetimes, even though low-k

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TDDB has emerged a major concern as Cu metallization has become mainstream.

III. Problem Formulation and Methodology

Given models for low-k TDDB, is there a way to predict chip lifetime because of low-k TDDB for different physical geometries and layout features, without directly using physics-based models?

To address this question, we first identify critical geometry features affecting *TF*. Specifically, although a number of factors can affect the *TF* of Cu/Low-k interconnects, in this work, as a starting point, we focus on the impact of area and metal linewidth on *TF*.

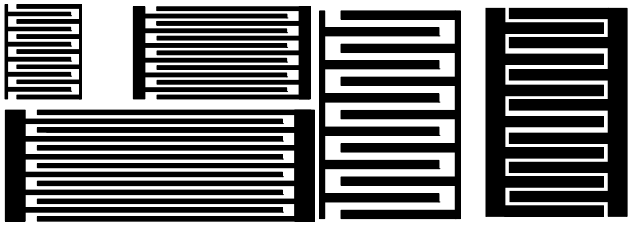
Next, we build models to extrapolate *TF* from one feature size to another. And, we use models to combine failure rates from different features to extract a full chip failure rate.

IV. Test Structure Design

Comb structures are used to measure TDDB characteristics of low-k dielectrics. Stress, an electric field, is created in the dielectric by applying a voltage difference between combs. We have designed a test chip for an industrial 45nm process to enable us to model lifetimes. Wafers have been fabricated that include these test structures.

A. Test Structures to Study the Effect of Area

To isolate the impact of area, we have designed structures with area multiples of a *1X* area test structure. Figure 2(a) shows test structures that vary the area of the dielectric while keeping the number of tips constant. Other features, like metal linewidth and metal line space, remain constant in these test structures.



(a) (b)

Fig. 2. Test structures to study the effect of (a) area and (b) metal linewidth.

B. Test Structures to Study the Effect of Metal Linewidth

Figure 2(b) shows test structures designed for isolating the impact of linewidth on low-k TDDB. The test structure on the left in Figure 2(b) has unit metal linewidth. The test structure on the right has wider lines. All test structures have a constant line space and dielectric area. As a result, only the area of metal changes.

V. Test Results

The data collected from the tests is fit by a Weibull distribution. To do this, the data are arranged from the smallest *TF(i)* to largest, and probability points, P_i, are assigned accordingly. We plot:

$$\ln(-\ln(1-P_i)) = \beta(\ln(TF(i)) - \ln\eta). \quad (3)$$

The intercept of the x-axis is the characteristic lifetime, η, and the slope is the shape parameter, β. The characteristic lifetime, η, corresponds to $P_i = 0.625$.

A. Effect of Area

The measurement data related to area, with a fixed number of tips, is shown in Figure 3. The results indicate a strong impact of area. In [8],[9], we have proposed a methodology to determine η and β from this data, while eliminating any impact of failure due to electric field enhancement at comb tips.

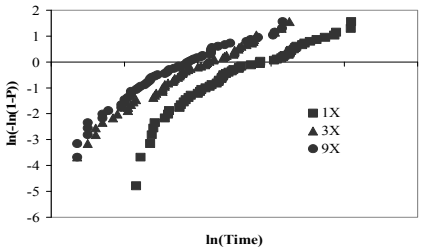


Fig. 3. Test results for structures used to isolate the impact of area.

B. Effect of Metal Linewidth

Figure 4 shows the Weibull plots for data from our test structures which vary linewidth. The results show that linewidth has a strong impact on low-k TDDB, despite the fact that the area of the dielectric under stress remains the same. This is not in line with any of the existing theories, i.e. (2), where *TF* is only a function of electric field, *E=V/S, V* is the voltage stressing the dielectric, and *S* is the line spacing between the metal lines. However, in fabricated chips, line spacing can be a function of density [10],[11] and the aspect ratio of the trench [11].

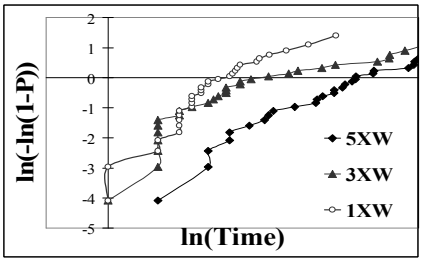


Fig. 4. Test results for structures used to isolate the impact of linewidth.

Our data was found to display a dependence on the aspect ratio of the trench, which explains the better lifetimes for wide lines. Specifically,

$$S_{ACTUAL} = S_{DRAWN} - \Delta W \quad (4)$$

where S_{ACTUAL} is the true line spacing, S_{DRAWN} is the drawn line spacing in the layout, and ΔW is the shift between the two due to the manufacturing process. We have used SEM measurement data to extract a function for ΔW. The data are shown in Figure 5.

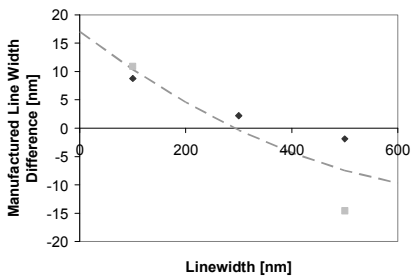


Fig. 5. The manufactured shift in line width as a function of linewidth.

Any dielectric area is bordered by two lines. To find S_{ACTUAL} for a dielectric area, we first find the width of the lines on each side using the layout. We then use the data in Figure 5 to find the shift in width, ΔW, for each line. These shifts are added, and S_{ACTUAL} is computed with (4).

VI. Lifetime Extraction From the Chip Layout

We now turn to predicting chip lifetimes based on data on the breakdown statistics of Cu/low-k interconnect systems. We assume a random distribution of electric fields due to signaling. In other words, the average voltage difference between any two lines is assumed to be equal. In addition, we make the most pessimistic assumption that the electric field is under constant stress.

A. Determination of Vulnerable Sites for a Single Layer

The feature that is extracted from layouts is the vulnerable length between two lines, L_i, associated with a distance between the lines, S_i, which is a function of the widths of the two adjacent lines, W_1, W_2, $W_1 \geq W_2$. The corresponding vulnerable area is $A_i = S_i L_i$, where S_i is the actual line space, in accordance with (4). Suppose we are interested in conductors separated by space, S_i, Figure 6 shows the corresponding length of interest.

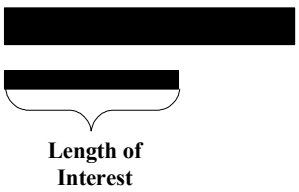


Fig. 6. For two parallel lines, the length we are interested in is the length for which the two lines run side by side.

We analyze the layout by determining a set of pairs $(S_i(W_1,W_2),L_i)$ for each layer, for all line spacings, $S_i(W_1,W_2)$, surrounded by widths W_1, W_2.

B. TF for a Single Layer

We assume a Poisson model for the probability of failure and a Weibull distribution, i.e.

$$P = 1-\exp(-\lambda(t)A_f) = 1-\exp\left(-(TF/\eta)^{\beta}\right) \qquad (5)$$

where $d_f = \lambda(t)A_f$ is the number of defects at failure for the f^{th} feature, $\lambda(t)$ is the defect density at failure, and A_f is the vulnerable area. Let $A_{test} = L_{test}S_{test}$ be the vulnerable area of the test structure, whose actual line spacing is S_{test}, which corresponds a vulnerable length, L_{test}. Then, we use the test data to find $\lambda(t)$ corresponding to S_{test}.

Suppose that the vulnerable length corresponding to actual spacing S_f is L_f. Then the corresponding number of defects for a spacing S_f is $d_f = \lambda(t)S_f L_f$. Since the characteristic lifetime corresponds to $P = 0.625$, the corresponding characteristic lifetime of the chip is related to the lifetime of the test structure as follows:

$$\eta_f = \eta_{test}\left(\frac{L_{test}}{L_f}\right)^{\frac{1}{\beta}}. \qquad (6)$$

Note that the layout contains more than one spacing between the lines. Therefore, we must consider how to determine a lifetime when the line spacing is different than the test structure. To do this, we rely on (2), rewritten in terms of S_{test}:

$$\eta_{test} = k_1 \exp\left(\frac{-\gamma W^m}{S_{test}^m}\right). \qquad (7)$$

Next, suppose that the chip contains line spacing, S_f. Then, the corresponding characteristic lifetime of a chip with lines spacing S_f and vulnerable length L_f is

$$\eta = \eta_{test}\exp\left(-\gamma W^m\left(S_f^{-m} - S_{test}^{-m}\right)\right)\left(\frac{L_{test}}{L_f}\right)^{\frac{1}{\beta}}. \qquad (8)$$

Clearly, layouts contain many different line spacings, S_f. Hence, it is necessary to combine the failures for all lines spacings. We do this by computing an overall defect count at failure. For a single spacing, the defect count as a function of time is

$$d_f = \frac{L_f}{L_{test}}\left(\frac{TF}{\eta_{test}}\right)^{\beta}\exp\left(\gamma W^m\beta\left(S_f^{-m} - S_{test}^{-m}\right)\right) \qquad (9)$$

The total defect count at failure is the sum, $d = \sum_f d_f$. Then, finding the characteristic lifetime, we choose the probability point $P_i = 0.625$ to get

$$\eta = \eta_{test}\left(L_{test}\Big/\sum_f L_f \exp\left(\gamma W^m\beta\left(S_f^{-m} - S_{test}^{-m}\right)\right)\right)^{\frac{1}{\beta}}. \qquad (10)$$

Figure 7 shows the characteristic lifetime for each layer for an example JPEG encoder/decoder chip. The lifetime of Layer 3 is shortest because it is the densest, with more than 70% of the lines belonging to one linespace group.

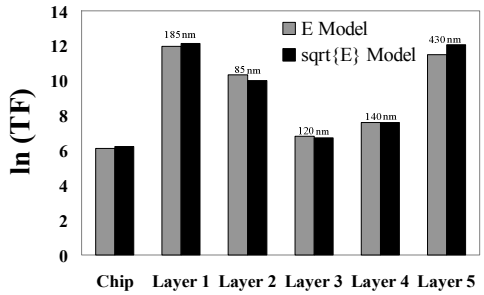


Fig. 7. Characteristic lifetime for individual layers and the complete chip for an example circuit, a JPEG decoder/encoder. The figure also shows the critical line spacing for each layer.

C. TF of the Full Chip

Let d_l be the defect density for each layer, where

$$d_l = \sum_f d_f \tag{11}$$

and d_f is computed with (9). Overall, for the chip,

$$d_{chip} = \sum_l d_l \ . \tag{12}$$

Unlike for a single layer, multiple layers of a chip may have different process details. Therefore, data would need to be collected from test structures for each layer separately, i.e., $L_{test(l)}$, $\eta_{test(l)}$, and $\beta(l)$ are unique to each layer.

If β were common to all layers, then it is possible to solve for the characteristic lifetime of the chip, η_{chip} ,

$$\eta_{chip} = \left(\sum_l \frac{\sum_{f(l)} L_{f(l)} \exp\left(\mathcal{W}^m \beta \left(S_{f(l)}^{-m} - S_{test(l)}^{-m}\right)\right)}{L_{test(l)} \left(\eta_{test(l)}\right)^{\beta}} \right)^{-\frac{1}{\beta}} . \tag{13}$$

Otherwise, η_{chip} is implicitly defined:

$$\sum_l d_l = 1 \tag{14}$$

where

$$d_l = \sum_{f(l)} \frac{L_{f(l)}}{L_{test(l)}} \left(\frac{\eta_{chip}}{\eta_{test(l)}} \right)^{\beta(l)} \exp\left(\mathcal{W}^m \beta(l) \left(S_{f(l)}^{-m} - S_{test(l)}^{-m}\right)\right). \tag{15}$$

The characteristic lifetime for the JPEG encoder/decoder chip is shown in Figure 7. It can be seen that the characteristic lifetime of the full chip is close to that of Layer 3, the most dense layer.

VII. Discussion and Conclusions

In this work, a methodology has been proposed to extend models of low-k TDDB to circuits. The analysis methodology estimates the impact on lifetime of low-k dielectric breakdown, accounting for differences in vulnerable area between the chip and test structures and variation due to metal linewidth and line space.

The current methodology has some limitations. We currently do not handle all geometric features in a layout, such as any impact due to vias, pattern density, and field enhancement at tips, corners, bends, and other unconventional geometries. Instead, we have focused on only two major sources of variation, line space and linewidth, and we have accounted for differences in area.

We have not scaled our results to use conditions. This should be done for full chip reliability prediction since the chip operates at very different temperatures and voltages than the test conditions. Moreover, different areas of the layout may experience different stress conditions due to variation in operation (signaling) and temperature profiles. It is likely that areas that experience higher stress may also experience higher temperature. This needs to be taken into account in future work.

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References

[1] J.W. McPherson and D.A. Baglee, "Acceleration factors for thin gate oxide stressing," *Proc. Int. Reliability Physics Symp.,* 1985. pp. 1-5.

[2] J.R. Lloyd, E. Liniger, and T.M. Shaw, "Simple model for time-dependent dielectric breakdown in inter- and intralevel low-k dielectrics," *J. Applied Physics,* vol. 98, pp. 1-6, 2005.

[3] F. Chen, *et al.,* "The effect of metal area and lime spacing on TDDB characteristics of 45nm low-k SiCOH dielectrics," *Proc. Int. Reliability Physics Symp.* 2007, pp. 382-389.

[4] C. Hong, L. Milor, and M.Z. Lin, "Analysis of the layout impact on electric fields in interconnect structures using finite element method," *Microelectronics Reliability,* vol. 44, pp. 1867-1871, Sept.-Nov. 2004.

[5] S. Alam, *et al.,* "Relaibility computer-aided design tool for full-chip electromigration analysis and comparison with different interconnect metallizations," *Microelectronics Journal,* vol. 38, no. 4-5, pp. 463-473, 2007.

[6] C. Hu, "IC reliability simulation," *IEEE J. Solid-State Circuits,* vol. 27, no. 3, pp. 241-246, 1992.

[7] X. Li, *et al.,* "A new SPICE reliability simulation method for deep submicrometer CMOS VLSI circuits," *IEEE Trans. Device Materials Reliability,* vol. 6, no. 2, pp. 247-257, 2006.

[8] M. Bashir and L. Milor, "A methodology to extract failure rates of low-k dielectric breakdown with multiple geometries and in the presence of die-to-die linewidth variation," *Microelectronics Reliability,* vol. 49, no. 9-11, pp. 1096-1102, 2009.

[9] M. Bashir and L. Milor, "Modeling low-k dielectric breakdown to determine lifetime requirements," *IEEE Design & Test Computers,* vol. 26, no. 6, pp. 18-26, Nov./Dec. 2009.

[10] L. Milor and C. Hong, "Backend dielectric breakdown dependence on linewidth and pattern density," *Microelectronics Reliability,* vol. 47, pp. 1473-1477, 2007.

[11] K.O. Abrokwah, P.R. Chidambaram, and D.S. Boning, "Pattern based prediction for plasma etch," *IEEE Trans. Semiconductor Manufacturing,* vol. 20, pp. 77-86, 2007.