TSV Redundancy: Architecture and Design Issues in 3D IC

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***Abstract*—3D technology provides many benefits including high density, high band-with, low-power, and small form-factor. Through Silicon Via (TSV), which provides communication links for dies in vertical direction, is a critical design issue in 3D integration. Just like other components, the fabrication and bonding of TSVs can fail. A failed TSV may cause a number of known-good-dies that are stacked together to be discarded. This can severely increase the cost and decrease the yield as the number of dies to be stacked increases. A redundant TSV architecture with reasonable cost for ASICs is proposed in this paper. Design issues including recovery rate and timing problem are addressed. Based on probabilistic models, some interesting findings are reported. First, the probability that three or more TSVs are failed in a tier is less than 0.002%. Assumption of that there are at most two failed TSVs in a tier is sufficient to cover 99.998% of all possible faulty free and faulty cases. Next, with one redundant TSV allocated to one TSV block, limiting the number of TSVs in each TSV block to be no greater than 50 and 25 leads to 90% and 95% recovery rates when 2 failed TSVs are assumed. Finally, analysis on overall yield shows that the proposed design can successfully recover most of the failed chips and increase the yield of TSV bonding to 99.99%. This can effectively reduce the cost of manufacturing 3D ICs.**

I. Introduction

3D integration techniques are proposed as solutions to overcome the scaling limit [1]. 3D technology provides many benefits including high density, high band-with, low-power, and small form-factor [2]. Through-Silicon Via (TSV) [3], which provides communication links for dies in vertical direction, is a critical design issue in 3D integration. In current manufacturing process for 3D designs, each die to be integrated is manufactured individually. When TSV technology is applied, TSVs and bond pads are fabricated inside each die [4][5]. Then, bonding technology is used for die stacking. Just like other components, the fabrication and bonding of TSVs can fail. A failed TSV may cause a number of known-good-dies that are stacked together to be discarded. This can severely increase the cost and decrease the yield as the number of dies to be stacked increases.

To improve the yield, some recovery mechanism is needed. A simple but effective solution is to add redundant TSVs which can be used to replace failed TSVs. This idea has been realized in 3D DRAM designs [6]. In the proposed scheme, for every 4 signals, 6 TSVs are allocated as a group. A switching box is required for each group to select which 4 TSVs are actually used to transfer signals. The advantage of this structure is that the delays of all signals are almost identical. This is an attractive property for DRAM designs. Although this structure is suitable to the dedicated layout style of memory designs, the cost is too expensive for ASICs. Another fault tolerance scheme that utilizes redundant TSVs targets on 3D network-on-chip (3DNoC) links [7]. Though significant yield improvement is achieved, the analysis and design flow are based on the dedicated network structure of 3DNoC. For ASICs, the analysis and design flow may not be suitable. In this paper, a redundant TSV architecture and related design issues are discussed. The proposed redundant TSV design can successfully recover most of the failed chips and increase the yield to 99.99% based on probabilistic models.

The rest of this paper is organized as follows. First, in Section II, the yield of TSV bonding is discussed. In Section III, the proposed architecture for TSV redundancy is introduced. Next, in Section IV, the recovery rate and the number of redundant TSVs required for the proposed architecture is analyzed. Probabilistic model is used for evaluation. The design issues for timing and required design flow are explained in Section V. Finally the conclusion of this work is given in Section VI.

II. Failure Rate Analysis for TSV

The fabrication of TSV-based 3D ICs can be partitioned into following stages. First, dies of each tier are fabricated individually. The fabrication of TSVs in each tier takes place in this stage. Depending on the technology (TSV first/last), either reactive-ion etching (RIE) or laser drilling is performed before TSV metallization process. According to the diameter and aspect ratio of TSV, proper material (Cu or W [5]) is selected for metallization. In general, the size of a TSV is much larger than other on-chip devices. This leads to certain unique defect features for TSV forming [8]. For example, void may be formed in TSV and causae a TSV to fail [10]. After the fabrication of TSVs, wafer thinning is performed. Presently, most 3D IC processes require each tier to be less than 100 microns [5]. The surface roughness is an important factor to the yield of later bonding stage. When the dies of consecutive tiers are stacked, the TSVs of the die in upped tier need to be bonded to the bond pads of the die on lower tier, as shown in Figure 1. Due to the alignment problem, a bond pad is required

This work was supported in parts by National Science Council of Taiwan, Republic of China, under grant NSC 98-2220-E-007-024, NSC 98A052

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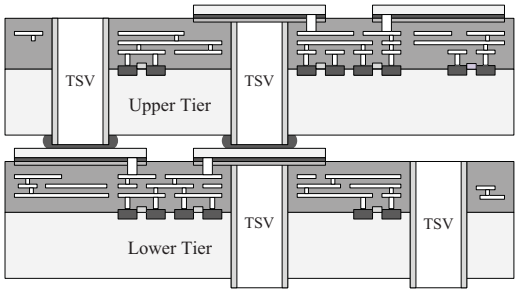

Fig. 1. Bonding between TSVs and Bond Pads

for each TSV [9][10]. In addition to misalignments, TSVs can also fail in the soldering process [11]. For example, short circuits between two distinct TSVs or open circuits between a TSV and its corresponding bonding pad may be formed. Other failure mechanisms such as dislocation, process variations or mechanical stress also decrease the fabrication yield of TSVs.

Above all, misalignment and failures on bonding are primary failure mechanisms for TSVs [11]. Both of the technologies used for alignment and bonding are very similar to the packaging methods used in current IC industry [5]. Although the exact failure rate of TSVs is still not clear, it is possible to use the failure rates of alignment and bonding to perform a failure rate analysis for TSV. Considering the TSV diameter and the size of bond pads, the failure rate of a single TSV may ranges between 10^{-4} and 10^{-5} based on current packaging technology. This assumption roughly meets the yields of TSVs from the process technologies of HRI, IMEC and IBM [12][13][14].

According to the applications and network styles, the number of TSVs in each tier can be quite different. For many-core processors or NoC-based designs, thousands of TSVs may be required in each tier. On the contrary, hundreds of TSVs may be sufficient for smaller IP-based designs. In this work, we focus on IP-based designs where TSVs are mainly used for connections between modules on different tiers. Considering the area of bond pads and floorplan problems, we assume that the number of TSVs to be placed in a tier ranges from 300 to 500.

An analysis between failure rate and yield is given in Figure 2. Assume that all dies to be stacked are known-good-dies. Thus, only the failure rate of TSV bonding needs to be considered. Let f stands for the failure rate of bonding one TSV and *#tier* stands for the number of tiers to be stacked. Note that the actual number of tiers that contain TSVs to be bonded is equal to *#tier* - 1. For example, when *#tier* = 2, only the top tier contains TSVs to be bonded. The x-axis represents the number of TSVs to be placed in each tier (*#TSV*). Since a good chip stack requires all TSVs to be successfully bonded, the binding yield can be computed as $(1-f)^{\#TSV\times(\#tier-1)}$.

The analysis results for f = $\{0.0001, 0.00002\}$ and $\#tier$ = $\{2\ ,\ 5\}$ are shown in Figure 2. Without any redundant TSVs, the average yield is 94.35%. And when $\#TSV$ = 500 and $\#tier$ = 5, the yield degrades to 81.8%. Note that dies to be stacked are all known-good-dies. Therefore, the cost of discarding chip stacks that are failed due to TSV bonding is very expensive. In fact, in most failed chip stacks, only a very

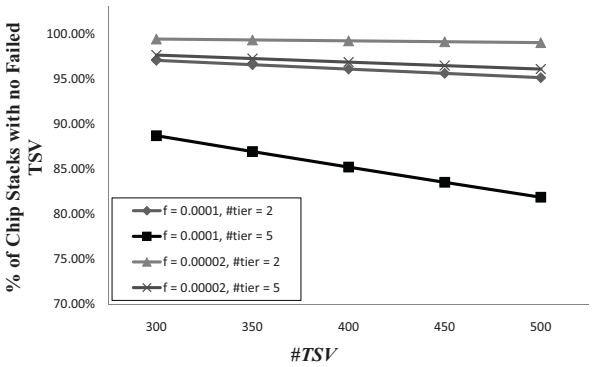

Fig. 2. Yield Analysis

small portion of TSVs are failed. If these failed TSVs can be recovered with circuits of reasonable cost, the yield can be largely improved. The redundant TSV design to be proposed in this paper provides a solution to this problem.

III. Redundant TSV Architecture

In this section, the architecture of our proposed redundant TSV design is introduced in Section III-A. Next, a brief introduction to the floorplan of 3D IC and its relation to our proposed architecture are given in Section III-B.

A. Architecture Design

The proposed architecture for redundant TSV is depicted in Figure 3. For each TSV, 2 MUXs are added to shift the signal to neighboring TSV when one TSV is failed. To reduce the timing effect caused by the loading capacitance of the additional wires used for signal shifting, a pair of buffers are added to each TSV. The TSVs are connected as a chain where the redundant TSV is placed at the last position of the chain. When no TSV is failed, all signals are transferred by original TSVs as shown in Figure 4(a). When a TSV is failed, the signal of the failed TSV needs to be shifted. This in term causes all signals between the failed TSV and the redundant TSV to be shifted. For example, let *TSV_1* be failed. The signal paths after shifting are shown in Figure 4(b). When a signal is shifted, larger delay is introduced due to larger wire length and buffers. For signals that are timing critical, this may become a problem. We will discuss it in Section V-A. In this architecture, only one failed TSV can be recovered in each chain. If two or more TSVs are failed in a chain, only one of them can be recovered. Therefore, how to determine the number of TSVs in a chain so that an acceptable recovery rate can be achieved is an important design issue. This issue will be discussed in Section IV. For simplicity, the term *TSV-chain* is used to refer to the structure of the proposed redundant TSV architecture.

The MUXs in the proposed architecture are connected to an e-fuse array which can be programmed by a scan-chain. By default, all signals connect to MUXs are set to 0. When the testing for TSV connectivity is done, signals are scanned in to program the e-fuses so that each MUX receives an appropriate control signal.

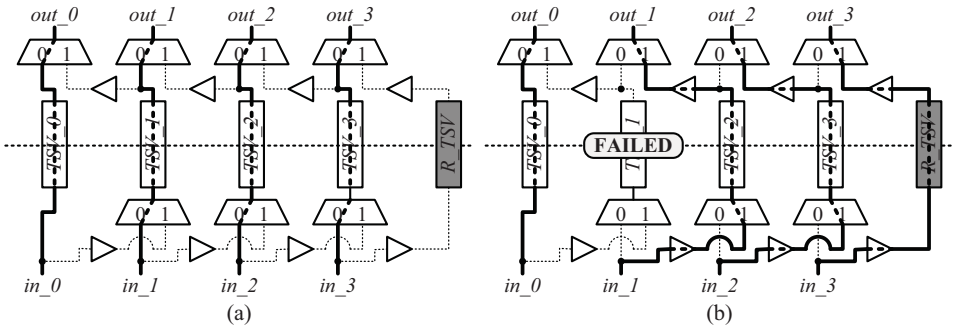

Fig. 4. TSV Recovery Mechanism: (a) Normal operations of TSVs; (b) TSV_1 is failed and TSV_1, TSV_2, and TSV_3 are shifted right one position

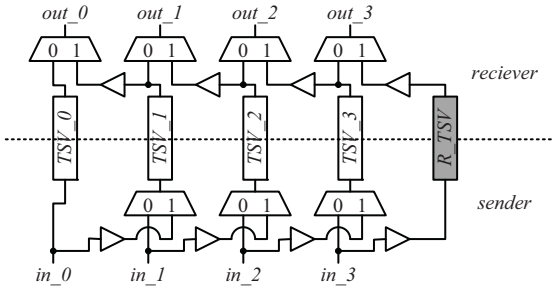

Fig. 3. Architecture for Redundancy TSV

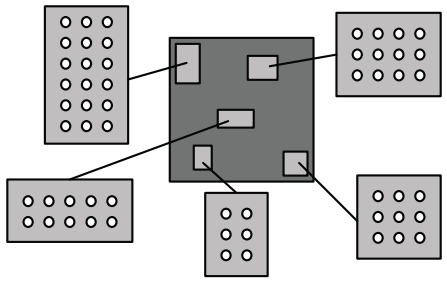

Fig. 5. TSV Blocks

B. TSV Block and TSV-Chain

Due to manufacturing and physical design issues, TSVs are not recommended to be placed arbitrarily on a plane. From the aspect of manufacturing, a regular placement of TSVs improves the exposure quality of the lithographic process and therefore improves the yield. In real designs, TSVs are suggested to be placed regularly in *TSV blocks* which are determined in floorplan stage. Inside each TSV block, TSVs are arranged in a grid-based structure to satisfy the pitch constraint of bond pads. Examples of TSV blocks are shown in Figure 5. Obviously, it is undesirable for a *TSV-chain* to contain TSVs of different TSV blocks due to long wires for signal shifting. Therefore, **a *TSV-chain* in our design is suggested to contains TSVs in the same TSV block**. Moreover, we let each TSV block contain only one redundant TSV. This means, for each TSV block, only one *TSV-chain* is defined. Nevertheless, in terms of recovery rate, the number of TSVs in a *TSV-chain* needs to be limited. In case the number of TSVs in a TSV block is too large for one *TSV-chain*, the TSV block needs to partitioned to a number of smaller TSV blocks.

The design issues for our the proposed *TSV-chain* are listed as follows:

- Determine the number of TSVs in each TSV block
- Determine the path to link the TSVs in a TSV block as a chain

The first problem is related to the recovery of a 3D design. In Section IV, an analysis based on probabilistic model is performed to answer this question. The second problem is related to the timing behavior of shifted signals. Discussions on timing issues and guidelines for *TSV-chain* design are presented in Section V.

IV. Recovery Rate Analysis

In this section, the relation between the number of TSVs in each TSV block and recovery rate is analyzed based on probabilistic models. First, based on the failure rate of a single TSV, the expected number of TSVs that may fail in a tier is discussed in Section IV-A. The result of Section IV-A determines the maximum number of failed TSVs that are expected to be recovered by our proposed *TSV-chains*. Next, for an expected number of failed TSVs in each tier, the required number of *TSV-chains* as well as the size limit of each TSV block are discussed in Section IV-B.

A. Analysis on the Expected Number of TSVs to be Recovered

Let F stand for the failure rate of a single TSV and N stand for the number of TSVs in a tier. The probability that exact n TSVs are failed in a tier can be expressed as

$$P_{f\_tsv=n} = C_n^N \times (F^n \cdot (1-F)^{N-n})$$

where C_n^N represents the number of combinations of N TSVs with n of them failed and $F^n \cdot (1-F)^{N-n}$ represents the probability of n chosen TSVs are failed while other $N-n$ TSVs are not. Next, the term C_Ratio_n is defined as the probability that the number of failed TSVs is no greater than n, including the faulty free condition (that is, n = 0). This can be computed by accumulating $P_{f\_tsv=i}$ for $0 \leq i \leq n$ and can be expressed as

$$C\_Ratio_n = \sum_{i=0}^{n} P_{f\_tsv=i}.$$

The values of $P_{f\_tsv=n}$ and C_Ratio_n for $F = 0.0001$ and N = {300, 400, 500} are listed in Table I.

TABLE I
$P_{f\_tsv=n}$ AND C_Ratio_n WHEN F = 0.0001

N	n	$P_{f\_tsv=n}$	C_Ratio_n
300	0	97.0444%	97.0444%
	1	2.9116%	99.9560%
	2	0.0435%	99.9996%
400	0	96.0788%	96.0788%
	1	3.8435%	99.9223%
	2	0.0767%	99.9990%
500	0	95.1227%	95.1227%
	1	4.7566%	99.8793%
	2	0.1187%	99.9980%

Table I shows that, when n = 2, the values of C_Ratio_n for N = {300, 400, 500} are all greater than 99.998%. A smaller F will result in a larger C_Ratio_n. This means, **as long as the failure rate F is no greater than 0.0001, the probability that three or more TSVs are failed is less than 0.002%.** Therefore, when designing *TSV-chains*, we can assume that **the maximum number of failed TSVs in a tier is 2.** This assumption covers 99.998% of all possible faulty free and faulty situations.

B. Analysis on Recovery Rate

As mentioned in Section III, each *TSV-chain* is capable of recovering at most one failed TSV in a TSV block. As the number of TSVs in a TSV block increases, the probability that all failed TSVs can be recovered decreases. To achieve an expected recovery rate, the number of TSVs in each TSV block must be limited. To simplify the analysis, we assume that the number of TSVs in all TSV blocks are identical. Let $\#B\_TSV$ stand for the number of TSVs in each TSV block and n stand for the number of failed TSVs. For a given value of n, we want to analyze the relation between $\#B\_TSV$ and recovery rate. The discussion in Section IV-A indicates that assuming $n \leq 2$ is sufficient to covers 99.998% of all possible faulty free and faulty situations. Therefore, we will perform the analysis for $n = 1$ and $n = 2$ only.

Let N stand for the number of TSVs in a tier. The number of combinations of N TSVs with n failed TSVs can be computed as C_n^N. The number of combinations that all failed TSVs can be recovered by *TSV-chains* is referred as $\#Recoverable\_Combinations$. The recovery rate discussed in this section is defined as

$$\frac{\#Recoverable\_Combinations}{C_n^N}.$$

When $n = 1$, only one failed TSV needs to be recovered. Since one TSV block contains one redundant TSV, regardless of the number of TSVs in each TSV block, one failed TSV can always be recovered. Therefore, the recovery rate for $n = 1$ is 100%.

The recovery rate analysis for $n = 2$ is more complicated. Let the term $\#Block$ represent the number of TSV blocks in a tier. Under our assumptions, $\#Block$ can be computed as $\frac{N}{\#B\_TSV}$. To successfully recover all failed TSVs, each failed TSVs must be located in different TSV blocks. That is, n TSV blocks are selected from $\#Block$ TSV blocks. Each selected TSV block contains exactly one failed TSV. The number of combinations that satisfies this requirement can be computed as

$$C_n^{\#Block}.$$

Inside each TSV block that contains one failed TSV, the failed TSV can be located at $\#B\_TSV$ possible positions. Therefore, the $\#Recoverable\_Combinaions$ for $n = 2$ can be computed as

$$C_2^{\#Block} \cdot (\#B\_TSV)^2.$$

The relation between $\#B\_TSV$ and recovery rate for N = 500 and n = 2 is shown in Figure 6. For different values of $\#B\_TSV$ that result in the same $\#Block$, only the smallest $\#B\_TSV$ is shown in the figure since the recovery rates of them are the same.[1]

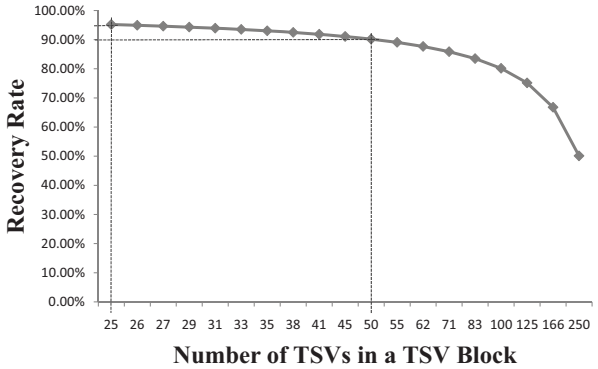

Fig. 6. Recovery Rate when N = 500, n = 2

According to Figure 6, to achieve 90% recovery rate, $\#B\_TSV$ needs to be no greater than 50. By limiting the number of TSVs in each TSV block to be less than or equal to 50, the recovery rate is greater than 90%. To achieve a higher recovery rate, the figure shows that with 95% recovery rate, the number of TSVs in each TSV block cannot be greater than 25. In realistic ASIC designs, the number of TSVs in a TSV block is usually less than 50. Therefore, in most cases, TSV block partitioning is not required.

A further analysis is to compute the overall yield. In Table I, when N = 500, $P_{f\_tsv=0}$, $P_{f\_tsv=1}$, and $P_{f\_tsv=2}$ are 95.1227%, 4.7566%, and 0.1187%, respectively. The discussion above indicates that the recovery rate for $n = 1$ is always 100% based on our proposed architecture. Thus, let the recovery rate for n = 2 be set to 90%. The overall yield can be computed as

$$P_{f\_tsv=0} + P_{f\_tsv=1} \times 100\% + P_{f\_tsv=2} \times 90\% = 99.98613\%.$$

This value is high enough for most applications.

V. Design Flow and *TSV-Chain* Design

The discussion in Section IV focuses on the recovery of failed TSVs in terms of connectivity. Timing issues are not concerned. As mentioned in Section III-A, when a signal is shifted in a *TSV-chain*, extra delay will be incurred. For signals that are timing critical, the delay caused by signal shifting may

[1]The actual computation of $\#RecoverableCombinaions$ is a little more complicated since sizes of TSV blocks may differ by one due to the division operation to compute $\#Block$

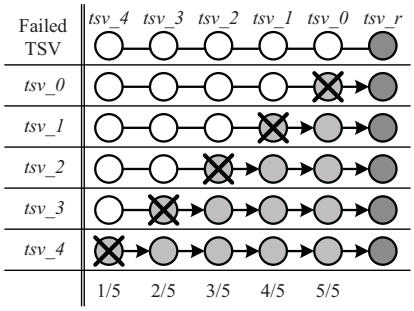

Fig. 7. All Possible Shifting Situations for a *TSV-chain* of Size 6 when 1 TSV is Failed

not be acceptable. In this section, timing issues for *TSV-chain* design are discussed in Section V-A. The discussion leads to the guidelines to link TSVs in a TSV block as a chain. Candidate *TSV-chain* structures are proposed in Section V-B. In Section V-C, design issues in each stage of 3D design flow are discussed.

A. Design Issues for Timing

As explained in Section III-A, when a TSV is failed, according to the position of the failed TSV in a *TSV-chain*, one or more signals need to be shifted. Due to the chaining structure, even under the assumption that each TSV has identical failure rate, the probability for each TSV in a *TSV-chain* to be shifted varies. Figure 7 shows this situation.

Assume that 1 TSV is failed in a *TSV-chain* of size 6, all possible shifting situations are enumerated in Figure 7. When no TSV is failed and no shifting is required, the *TSV-chain* is shown in the right column of the first row where the redundant TSV is denoted as *tsv_r*. For each row below, the left column indicates the failed TSV and the right column shows the shifting situation. The last row lists the shifting probabilities of the TSVs in the *TSV-chain* when 1 TSV is failed. For *tsv_0*, no matter which TSV in the *TSV-chain* is failed, it is always shifted because it is on the position next to the redundant TSV. On the contrary, *tsv_4*, which is at the head position of the *TSV-chain*, need not to be shifted unless itself is failed. In terms of extra delays introduced by signal shifting, this property of *TSV-chain* indicates that the probability that the delay of a signal linked by a TSV is increased depends on the position of the TSV in the *TSV-chain*. This means, for signals that are timing critical, it is preferable to assign these signals at the head parts of *TSV-chains*.

An evaluation for an extreme case where only one signal is timing critical is shown in Figure 8. The x-axis stands for the number of TSVs in a *TSV-chain* and the y-axis stands for the probability that the timing critical signal is shifted. The line denoted as "Unaware" represents that the timing critical signal has equal probability to be located at any position of a *TSV-chain*. And the line denoted as "Timing Aware" represents that the timing ctitical signal is always located at the beginning of a *TSV-chain*. Assume that the failure rate of each TSV is identical and there is only one failed TSV. The result in Figure 8 shows that, in "Unaware" cases, the probabilities for the timing critical signal to be shifted are greater than 50% in all cases. On the contrary, by assigning the timing critical

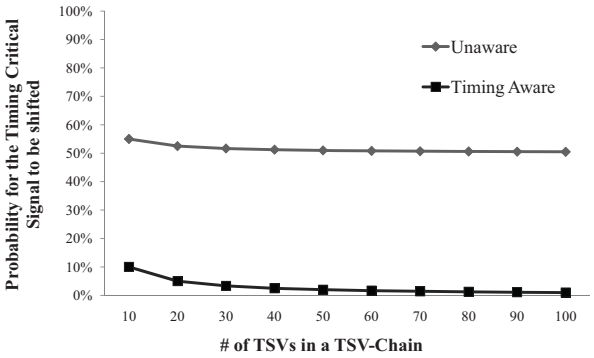

Fig. 8. Evaluation on the Possibility for the Timing Sensitive Signal to Be Shifted

signal to the head of a *TSV-chain*, the probability is reduced to 2.93% in average. Based on the evaluation, **timing sensitive signals should always be routed through the TSVs located at the head of *TSV-chains***. This is one of the guideline that should be followed when designing *TSV-chains*.

The next issue is to minimize the delay caused by signal shifting. This can be done by minimizing the distance between the connected TSVs in a *TSV-chain*. As mentioned in Section III-B, TSVs in each block are placed in a grid-based structure. Therefore, by requiring the connected TSVs in a *TSV-chain* to be neighbors in the grid-based structure, minimal and fixed shifting delay can be guaranteed. This also makes the shifting delay predictable in early design stages. Thus, the second guideline for *TSV-chain* design is that **any two connected TSVs in a *TSV-chain* must be next to each other in the grid-based structure**.

B. TSV-chain *Design Problem*

For each TSV block in a plane, the structure of the *TSV-chain* needs to be considered. The analysis in Section V-A indicates that timing critical signals should always be routed through the TSVs located at the head parts of *TSV-chains*. In current design flow, signals that are assigned to each TSV block are roughly determined in floorplan stage. However, the exact assignment of signals to TSVs is not necessarily to be done in this stage. From the perspective of physical design, leaving the assignment of signals to TSVs to be done in routing stage is beneficial to minimize wire length. Therefore, in addition to the guidelines obtained in Section V-A, the design of *TSV-chain* should also consider routing issues.

Based on the concept of bounding box, discussion on wire length is given first. For two pins on two different tiers to be connected, the relation between the bounding box of these two pins and a TSV block can be listed as follows. First, the bounding box and the TSV block can be non-overlapped. In this situation, only going through a TSV on the boundary of the TSV block can result in minimum wire length. Next, the TSV block can be either partially or completely overlapped by the bounding box. In this situation, any TSV that is overlapped by the bounding box can result in minimum wire length. Unless the bounding box is completely contained in the TSV block, a TSV on the boundary of the TSV block can always be found for minimum wire length. The discussion shows that, TSVs on the boundary of a TSV block have higher

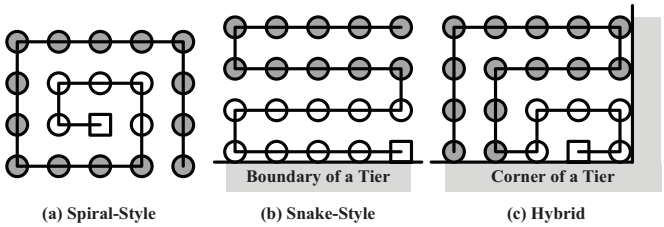

Fig. 9. *Chaining Styles*

probabilities to be routed through for minimum wire length. These TSVs should be assigned as head parts of *TSV-chains*.

A spiral-style chaining policy is proposed for *TSV-chain* design. In a TSV block, by picking a TSV in the central position to be the starting point, spiral-style chaining results in a routing path where all TSVs on the boundary are at one end. The starting TSV is assigned as redundant TSV while the other end becomes the head of a *TSV-chain*. An example for a 4×5 TSV block is shown in Figure 9(a) where TSVs in grey are head and good for timing critical signals. In routing stage, routers can choose to assign timing-critical signals to TSVs that are on the boundary of a TSV block. This can reduce the probability for a timing critical signal to be shifted.

The spiral-style chaining policy is appropriate for a TSV block that is not on the boundary or the corner of a tier. For a TSV block located on the boundary of a tier, most signals assigned to that TSV block are connected from the opposite side of the tier boundary. In this case, a snake-style chaining policy satisfies the requirement. The result is shown in Figure 9(b). For a TSV block located on the corner, most signals assigned to that TSV block are connected from the counter direction of the tier corner. In this case, a hybrid chaining policy as shown in Figure 9(c) becomes the best candidate. Based on the position of each TSV block, one of these three chaining policies can be applied to determine the structure of a *TSV-chain*.

C. Physical Design Flow Considering TSV-Chain

In current design flow for 3D ICs , 3D partitioning first takes place to determine which tier each design blocks to be placed. The number of required TSVs for signals between two consecutive tiers is determined in this stage. Next, in floorplan stage, blocks with fix area but unknown dimensions are placed in each tier. To provide communication links between blocks in different tiers, TSV blocks are placed. The number of signals to be assigned to each TSV block as well as the position of each TSV block are roughly determined in this stage. Based on the discussion in Section IV, the number of TSVs in each TSV block should be limited. Partitioning may be required for large TSV blocks. Based on the position of each TSV block, the structure of each *TSV-chain* is determined. In place and route stage, routers should be aware of the *TSV-chain* structure in each TSV block. Based on design constraints and requirements, router needs to decide whether to assign timing critical signals to TSVs that are located at the head of *TSV-chains*. The overall design flow for *TSV-chain* is shown in Figure 10.

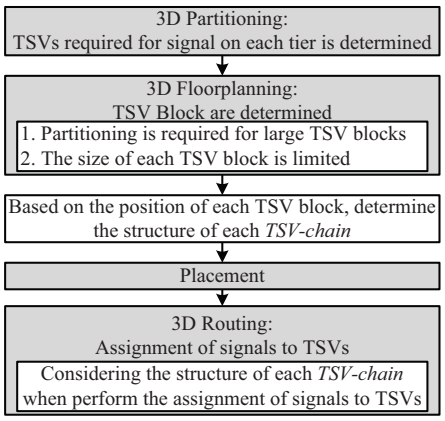

Fig. 10. Proposed Design Flow for *TSV-Chain*

VI. Conclusion

In this paper, a new redundant TSV architecture with reasonable cost for ASICs has been proposed. Design issues including recovery rate and timing problem have been investigated. Required modifications on the design flow has been explained. Based on probabilistic models, the new design can successfully recover most of the failed chips and increase the yield of TSV bonding to 99.99%. This can effectively reduce the cost of manufacturing 3D designs.

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