Reliability Aware Through Silicon Via Planning for 3D Stacked ICs

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***Abstract*—This work proposes reliability aware through silicon via (TSV) planning for the 3D stacked silicon integrated circuits (ICs). The 3D power distribution network is modeled and extracted in frequency domain which includes the impact of skin effect. The worst case power noise of the 3D power delivery networks (PDN) with local TSV failures resulting from fabrication process or circuit operation is identified in both frequency and time domain. From the experimental results, it is observed that a single TSV failure could increase the maximum voltage variation up to 70% which should be considered in nanoscale ICs. The parameters of the 3D PDN are designed such that the power distribution is reliable under local TSV failures. The spatial distribution of the power noise, reliability and block out area is analyzed to enhance the reliability of the 3D PDN under local TSV failure[1].**

I. Introduction

3D Integration technology is one of the fastest growing IC design directions that offer flexible and low cost integration and packaging solutions. The 3D PDN features bring in new challenges in addition to conventional power distributions. First, the reliability of the network due to the yield of through silicon vias is critical and need to be analyzed. Second, the signal integrity for multiple power supplies requires more stringent noise margin [1]. The TSV technology is aimed for nanoscale technology, where the noise margins are tight and power integrity needs accurate estimation.

On the other hand the increase in the power density and the distance of the stacked dice from heat sink will increase the temperature profile. As a result the power distribution network in 3D systems needs to be accurately modeled and designed in order to satisfy the noise margins and power and reliability.

In this work, a framework for the analysis of the reliability of 3D PDN under local TSV failures is proposed. The worse case power noise under local TSV failures resulting from fabrication process or circuit operations is analyzed. The 3D PDN is extracted and modeled in frequency domain considering skin effect and frequency dependent *RL* parasitics of the TSV.

The package for the 3D PDN analysis is developed which utilizes parallel computing. The model is first solved in frequency domain to identify the behavior of the system. Then the time domain voltage noise under worse case transistor switching currents is obtained with our enhanced vector fitting algorithm.

The reliability of the 3D PDN is analyzed with and without the local TSV failures. The spatial distribution of the power network metrics such as voltage noise, block out area and reliability is derived for the entire 3D (PDN). The parameters of the 3D PDN, such as TSV dimensions, densities and the tier mesh width and pitch and the decoupling capacitors are designed to mitigate the power noise due to the TSV failures. The objective of the optimization is to increase the reliability of the 3D structure and reduce the voltage noise while minimizing the block out area from TSV design rules.

The rest of the paper is organized as follows: The problem statement and reliability of the through silicon via is discussed in section 2. The 3D PDN and TSV model and extractions is described in section 3. In section 4, we will go over the flow for analysis of the reliability of the 3D PDN. Section 5 depicts the experiments result and analysis for a reliable 3D PDN design. Conclusions are drawn in section 6.

II. Reliability of Through Silicon Vias

Reliability is one first and foremost issue when we embrace the 3D IC technology via through silicon vias. When the via fails to make proper connection, unwanted loss in yield and performance may occur. A complete via open failure leads to a complete broken net, while a partial failure increases the resistance of the interconnect. As the technology shrinks, vias become more and more sensitive to variations such as cut misalignment, and electron migration and thermal stress induced voids. In this study, we explore efficient via placement to reduce the IR drop and SSN such that the PDN is fault tolerant under the local failures.

A. Thermo-mechanical reliability of TSV

Important reliability aspects of TSV in stacked devices are mechanical stresses and strains, thermally induced by the mismatch in coefficient of thermal expansion(CTE) of the individual materials. Test results also show that the solder bump portions are as critical as the TSV itself for the reliability [2]. Most of the TSVs are built with copper or siliconpoly and tungsten as an alternative. The CTE of copper ($17.5 \times 10^{-6}/^{\circ}\mathrm{C}$) is few times higher than that of silicon

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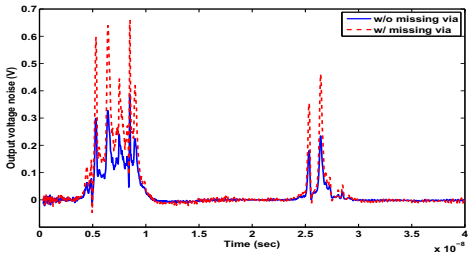
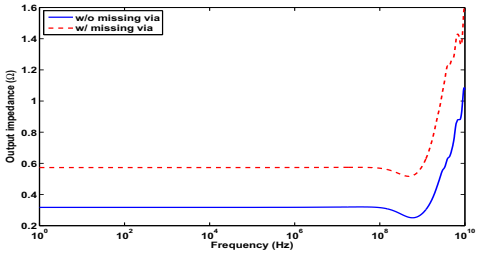
$(2.5 \times 10^{-6}/^{\circ}\mathrm{C})$ [3]. As a result the copper filled TSV is subject to temperature loading. These stress/strains between copper, silicon and dielectric can be high enough to introduce delamination between the interfaces [4].

The failure rate for TSV is defined as λ_f with the mean time to failure as: $MTTF = 1/\lambda_f$ [5]. The reliability factor is introduced as $R(t) = e^{-\lambda_f t}$ where t is the operation cycles of the TSV.



(a) TSV voltage drop



(b) TSV impedance profile

Fig. 1. Through silicon via noise under local TSV failures.

Fig. 1(a) is the result from failure analysis of the 3D power distribution. The maximum voltage droop noise increased by 70% from $0.39V$ to $0.66V$ after failure. The impedance profile in the frequency domain (Fig. 1) also is increased significantly due to the local via failure.

B. Reliability analysis problem statement

In this TSV reliability analysis, three major metrics are used: maximum power noise voltage drop (ΔV), Reliability factor (R) and the block out area ($A_{block\,out}$). Block out area is the region surrounding the TSV in the contact of the TSV and each mesh. Based on the design rules, this region is blocked and no signal or wire could be routed and no hard macro could be placed. Introducing more TSV reduces the ΔV and increases the reliability. On the other hand, increasing the density will reduce the limited routable area. The objective is to increase the reliability factor while reducing the block out region. TSV $Failure_i$ is:

$$Failure_i = (1 - R_i(TSV_{density}, TSV_{size})) \tag{1}$$

Here, we define the cost function as:

$$\Delta V \times (1 - R_i(TSV_{density}, TSV_{size})) \tag{2}$$

The constraint is the $A_{keepout}$. Therefore, the problem statement is described as:

$$\begin{aligned} min \quad & \Delta V \times (1 - R_i(TSV_{density}, TSV_{size})) \\ s.t. \quad & \sum_i A_{TSV\,keepout} \leq A_{max} \end{aligned} \tag{3}$$

where A_{max} is the maximum block out area that is available while routability is preserved.

III. TSV and 3D Power Distribution Model

The 3D power delivery model that we use in the experiments is a stacked $10 \times 10 mm^2$ active die modeled with 3D RLC mesh. We use $Q3D$ from Ansoft [6] to extract the parasitics of the 3D mesh. In the TSV extractions, the skin effect and the frequency dependenct $RL(f)$ model of the TSV is included to represent high frequency non-uniform current flow through TSV cross section. Our extracted TSV models demonstrate significant impedance increase for the TSV in the GHz range which need to be considered in the analysis (Fig. 2).

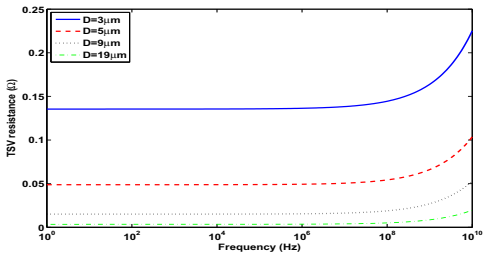


Fig. 2. Skin effect in TSV structure.

IV. 3D PDN Analysis Flow

In this section, we will describe the flow we developed in [7] for the analysis of the TSV and 3D power networks to identify the resonance peak as well as the maximum voltage drops. Because of the large scale number of mesh in the 3D PDN most of the conventional simulator fails to simulate the system in a reasonable time. The developed package is an efficient parallel processing analysis flow for the full power distribution network which enables iteration between both frequency and time domain.

In order to convert the frequency domain results into time domain we use vector fitting method [7]. However, as the clock frequency of the 3D stacked ICs is reaching GHz range and the transistor current stimuli includes many high frequency components, conventional vector fitting method [7] cannot fits high frequency component properly and the time domain recovered result has a large error ($\Delta \bar{V}_{VF}$):

$$\Delta \bar{V}_{VF} = \bar{V}(f) - \bar{V}_{VF}(f) \tag{4}$$

where $\Delta \bar{V}_{VF}$ is the deviation of the fitted frequency domain approximation and the original signal. We enhanced the vector fitting process and use the remainder of the vector fitting $\Delta \bar{V}_{VF}$ as the next iteration input and perform the vector fitting

process iteratively until $\Delta\bar{V}_{VF}$ reaches the acceptable error boundary (in our test case $\sim \Delta\bar{V}_{VF} \leq 10^{-15}$).

In order to identify the worse case voltage drop, we identify the frequency of resonant peak from the first run of the 3D PDN analysis. We stimulate the PDN with the current pulse with the period of the PDN resonance to identify the worse case drop of the 3D PDN under local TSV failures.

V. Results and Analysis for Robust TSV Design

In this section, we optimize the design parameters of the 3D PDN such that the system remains robust under local via defects. In our experiments, we model a $10 \times 10 mm^2$ die with stacked dies from 4 to 10 layers. We first analyze the original model without any TSV failures. We excluded the TSV under the hard macro of interest and demonstrated the increase in the power noise (Fig. 1(a)). From Fig. 1(a), we observe that the maximum voltage drop is increased by 70% which can not be ignored in nanoscale technology.

A. TSV dimension and density scaling

In this section, we increase the density of the TSV placement in the stacked ICs such that the power noise is reduced below an acceptable voltage drop tolerance. Increasing the density of TSV reduces the voltage drop caused by the TSV failure. Figure 3, demonstrates iterations among the dimensions of the TSV and the changes of the aspect ratio (height to cross section) of the TSV. Increasing the TSV cross section area will reduce the impedance of the PDN structures and as a result mitigate the power noise (Fig. 3).

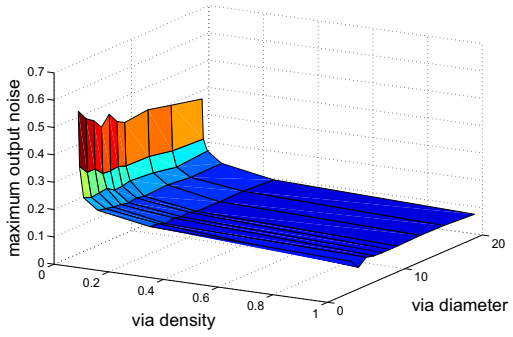


Fig. 3. Fault tolerant TSV design with TSV pitch and width scaling.

However, increase in the dimension and density will reduce the routable area of the stacked dies. According to the Design Rule Check, there is a keep out area surrounding the TSV in the contact of the TSV and tier power grids where no signal or power could be routed and no hard macro could be placed. In order to satisfy our minimum routability area we need to simultaneously analyze the noise and block area. Fig. 4 demonstrates that as the power noise decreases from the TSV dimension and density increase, the block out area is increased.

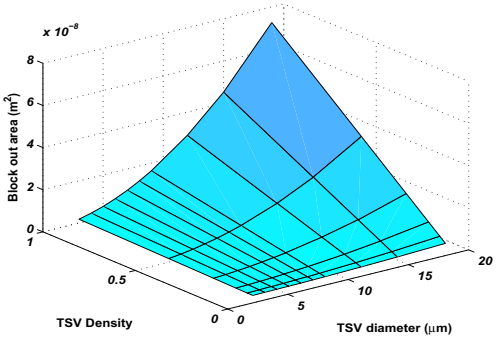


Fig. 4. Block out area versus the TSV diameter and density.

B. Power grid mesh scaling in each tier

In this part, the impact of different power mesh width for the metal layers in the tiers is analyzed. We observe that as the width in the tiers increases the power noise decreases. We increase the width such that we still preserve our maximum routable area in the dies. Next, for the same metal layers, the metal pitch is scaled down (Fig. 5).

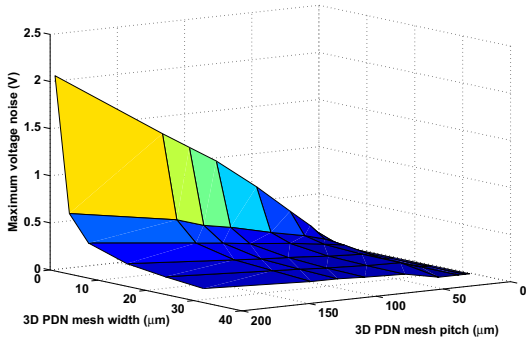


Fig. 5. Power noise profile versus the metal pitch and width scaling in the metal layers with TSV failure.

C. Number of stacking layers

Fig. 6 is the maximum voltage drop for different number of stacking layers which is normalized over the non-missing TSV voltage drop. It is observed the relative voltage drop increases as the number of stacking and impedance is increased. In some number of stacked layers, the increase in the relative voltage drop is not significant which is due to the anti-resonance of the stacking PDN and the frequency profile of the current.

D. Reliability of the TSV

Selvanayagam *et al.* [3] performed comprehensive study on thermo-mechanical reliability of the TSV for different TSV dimensions. Their study shows the relation between the thermal strain and diameter of the TSV is derived. The increase in the TSV diameter will increase the thermo-mechanical strains and as a result the reliability is reduced. The thermal resistance of the stacked 3D PDN reduces with the increase in the TSV densities.

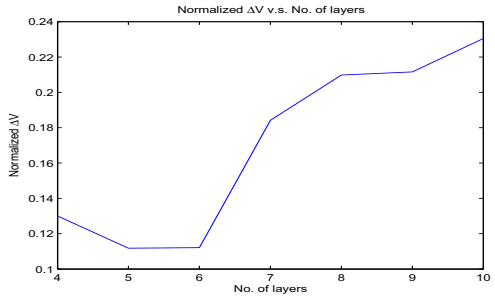


Fig. 6. Normailized ΔV vs. No. of layers.

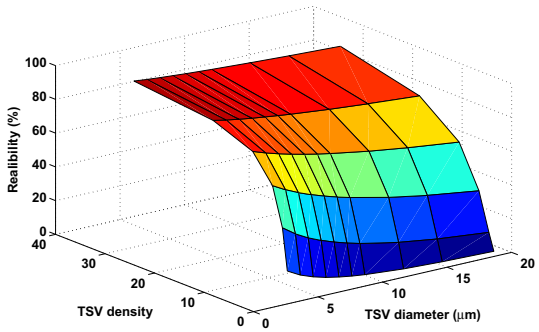


Fig. 7. Normalized TSV reliability factor.

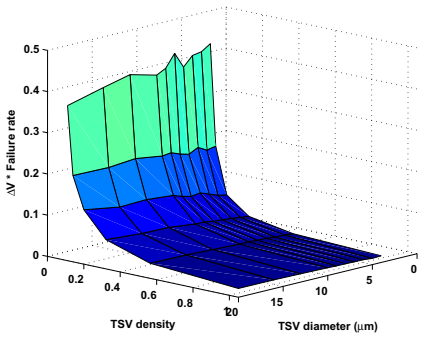


Fig. 8. Maximum ΔV × Failure rate vs. TSV pitch and size.

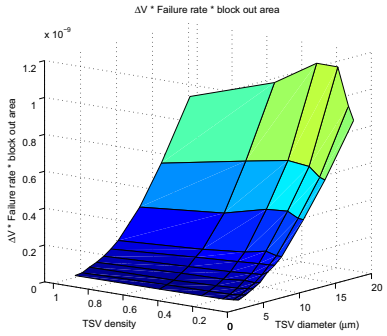


Fig. 9. Max ΔV × Failure rate × Block out area.

We used [3] and approximate and extrapolate the the stress. The reliability factor is defined as $R(t) = e^{-\lambda_f t}$ [5] . The relative normalized TSV reliability factor for fixed number of operation cycles is derived in Fig. 7. Fig. 7 shows that as the TSV diameter increases, the relative reliability factor is reduced. The 3D PDN reliability is also increased with the increase in the density of the TSV in the stacking. In addition, from Fig. 3 it is observed that we have the minimum power noise for the largest TSV diameters and highest density.

These conclude our observation in Fig. 8 which represents the cost function: failure rate times maximum voltage drop from equation (3). There is a trade off between the reliability and the power noise reduction as the TSV diameters increases. Increases in the diameter will reduce the voltage noise but decrease the reliability factor which is demonstrated in Fig. 8.

Fig. 9 concludes our TSV analysis framework. To obtain the minimum cost function (Failure rate × max voltage drop) with the minimum feasible TSV block out area, we minimize the failure rate × maximum voltage drop × block out area . The minimum , in Fig. 9, is the configuration where the 3D PDN has the least cost function (failure×noise) under local TSV failures and the block out region is minimized.

VI. Conclusion

In this work, a reliability aware through silicon via analysis framework is proposed. From the experimental results, it is observed that the ac noise could be increased up to 70% with single local TSV failure from fabrication or during the thermal cycling operation of the stacked IC which could not be ignored. We introduced the reliability metric cost function which is the relative failure rate of the TSV times the maximum voltage drop under local failure. The TSV block out area is the constraint that should not exceed the maximum routable area. The design parameters of the TSV and the 3D PDN are analyzed to mitigate the increase in the power noise caused by the TSV local failure.

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