A Loopback-Based INL Test Method for D/A and A/D Converters Employing a Stimulus Identification Technique

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***Abstract*—We propose a new method for the integral nonlinearity (INL) and differential nonlinearity (DNL) testing of D/A - A/D converter pairs employing the recently developed stimulus identification method. This allows both converters to be measured independently but simultaneously without significant fault masking problems. Simulations show that the INL and DNL estimation errors for 12-b A/D and D/A converters are less than 0.5 least significant bit (LSB) units, and experimental tests give similar results.**

I. Introduction

There is great pressure towards low-cost test solutions for A/D and D/A converters (ADCs and DACs) [1]. Static linearity measurement is one of the most time-consuming tests, especially if high resolution converters are to be tested, so that a fully digital test setup would give significant savings, because the time spent in an expensive tester can be reduced. If both converter types are present on the same chip, it would be beneficial to use the DAC to generate the test signal for the ADC, but this "loopback" configuration will usually result in fault masking problems and low test yields [2]. Without fault masking problems this test setup would be optimal for low-cost testing of both converter types, because it would allow an all-digital test configuration, the test stimuli and response both being digital.

Several low-cost test techniques have been proposed for both ADCs and DACs, but only a few of them use both converters in a loopback configuration to minimize the amount of additional test circuitry. Loopback test techniques that concentrate on testing dynamic parameters such as the signal-to-noise ratio, total harmonic distortion or spurious-free dynamic range have been proposed in [2]–[5], and a few loopback techniques have also been proposed for static linearity testing. In [6] the authors used the statistical behaviour of noise to resolve the linearity of an ADC and then used this to measure the linearity of a DAC, while the authors of [7] proposed that it may also be possible to first measure the integral nonlinearity (INL) of a DAC using the statistical behaviour of noise and then to linearize it and generate a uniformly distributed input signal for an ADC to test this by the standard histogram method.

It is proposed in [8] that the linearity of an ADC can be measured without a linear or a priori known test stimulus if two related test signals are used, and we have demonstrated in [9], [10] how a very simple calculation algorithm can be used to solve the probability density function (PDF) of the test signal and how this information can be used to calculate the stimulus-independent INL of an ADC.

We will show in this paper that it is possible to use a loopback configuration with this stimulus identification method to determine the linearity of both converters simultaneously without significant fault masking problems. We will describe the basics of the stimulus identification method in the next section and suggest in section III how the INL of a DAC (or any test stimulus) can be calculated using stimulus identification. Section IV will describe our simulations and section V show some experimental results. Other applications of the stimulus identification method will be discussed in section VI, and this will be followed by our conclusions.

II. The Stimulus Identification Method

The code density test method (or histogram method) is based on the fact that the number of hits per ADC code depends on the code width (cw) and the slope of the test stimulus (x') at this point

$$h(i) = cw(i) \cdot \frac{f_s}{x'(t_i)}, \tag{1}$$

where t_i is the time instant when the ADC output code is i, f_s is the sampling frequency and $cw(i)$ is the normalized width of code i.

If we define h_{ideal} to be the code density histogram of an ADC which has constant code widths and code centres that are equal to those of the ADC under test, we can represent the measured code density histogram of a particular stimulus by

$$h(i) = cw(i) \cdot h_{\mathrm{ideal}}(i), \tag{2}$$

and if h_{ideal} is known, we can solve the code widths from (2) as:

$$cw(i) = \frac{h(i)}{h_{\mathrm{ideal}}(i)}. \tag{3}$$

Even if the stimulus (and thus h_{ideal}) is unknown, we can reconstruct h_{ideal} and extract the non-linearity of the test

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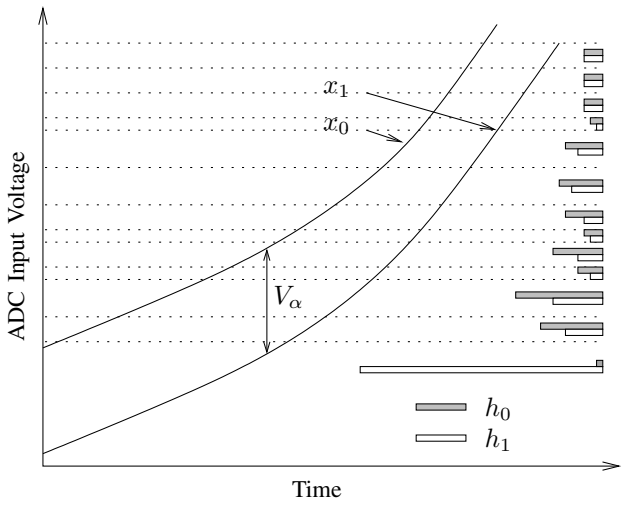


Fig. 1. Related stimuli x_0 and x_1.

stimulus from the measured histogram data if we use two (or more) related test stimuli. Let the stimuli be

$$x_0(t) = x(t), \quad (4)$$
$$x_1(t) = x(t) - V_\alpha, \quad (5)$$

where $x(t)$ is the original repeatable stimulus and V_α is the constant difference between x_0 and x_1. Possible x_0, x_1 and corresponding histogram bins are shown in Fig. 1. Using (2) we can express measured histograms for both stimuli as:

$$h_0(i) = cw(i) \cdot h_{\text{ideal}}(i), \quad (6)$$
$$h_1(i) = cw(i) \cdot h_{\text{ideal}}(i + \alpha), \quad (7)$$

where α is V_α in LSB units.

As was shown in [9], it is possible to use numerical differentiation and the measured histograms h_0 and h_1 to approximate the derivative of h_{ideal}

$$\begin{aligned} \hat{h}'_{\text{ideal}}(i) \cdot cw(i) &= \frac{h_{\text{ideal}}(i+\alpha) - h_{\text{ideal}}(i)}{\alpha} \cdot cw(i) \\ &= \frac{h_1(i) - h_0(i)}{\alpha}, \end{aligned} \quad (8)$$

and after integrating $\hat{h}'_{\text{ideal}}$ we obtain the estimate of the code density histogram $\hat{h}_{\text{ideal}}$, which corresponds to the histogram of an ideal ADC for that stimulus. The integration can be implemented using the trapezoidal integration rule

$$\begin{aligned} \hat{h}_{\text{ideal}}(i) &= \sum_{j=0}^{i-1} \hat{h}'_{\text{ideal}}(j) \cdot cw(j) + \frac{\hat{h}'_{\text{ideal}}(i) \cdot cw(i)}{2} \\ &= \sum_{j=0}^{i} \frac{h_1(j) - h_0(j)}{\alpha} + \frac{h_1(i) - h_0(i)}{2\alpha}, \end{aligned} \quad (9)$$

where the $cw(i)$s are part of the integration process, because we want to determine how the stimulus affects the measured ADC given that the codes are not equally spaced, so that the correct integration steps are $cw(i)$s instead of a constant value.

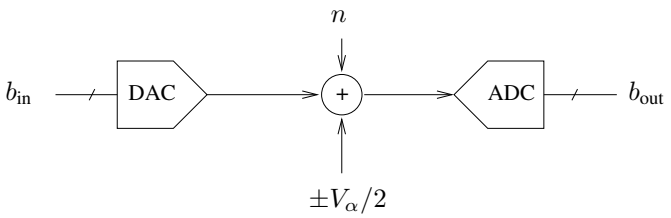


Fig. 2. The stimulus identification-enabled loopback test configuration.

Using (3) and (9) it is possible to determine the code widths and calculate the differential nonlinearity (DNL) and INL of the ADC. If we use the average of $h_0(i)$ and $h_1(i)$ as $h(i)$, equations (3) and (9) and the fact that the end-point INL should be zero at the end-points, we can solve α as in [9]:

$$\alpha = \frac{2 \cdot (2^N - 2)}{\sum_{i=1}^{2^N-2} \left[\frac{h_1(i) + h_0(i)}{\sum_{j=0}^{i-1} [h_1(j) - h_0(j)] + \frac{h_1(i) - h_0(i)}{2}} \right]}, \quad (10)$$

where N is the number of ADC bits.

The algorithm proposed in [9], as briefly described above, is simple and works well if the magnitudes of the higher derivatives in the test stimulus are low enough. Higher derivatives (sharp edges) will cause problems because the simple differentiation method as used above detects only the lowest derivatives correctly. In [10] we proposed a means for using the central-difference method to increase the differentiation accuracy and this should be used instead of the forward and backward differentiation suggested above. In order to concentrate on the main idea, we do not use the central-difference method when describing the test method, but it is used in the simulations and experimental tests in order to demonstrate the attainable estimation accuracy.

III. A Linearity Test Method for DAC-ADC Pairs

In the previous section we described how the INL of an ADC can be measured with an unknown test stimulus and argued that the INL of an ADC can be resolved because the effect of the test stimulus on the measured histograms can be estimated and this code density histogram h_{ideal} is similar to the PDF of the input signal. If we use a DAC to generate the test stimulus, we have the test configuration shown in Fig. 2 and the stimulus identification gives the PDF of the DAC output. To measure the INL of the DAC we simply add $V_\alpha/2$ and $-V_\alpha/2$ in turn to the DAC output and go through all the codes several times. If the DAC input is uniformly distributed over all the codes, the DAC output should also be uniformly distributed and h_{ideal} should be flat. Therefore, the end-point INL estimate for the DAC can be calculated from $\hat{h}_{\text{ideal}}$ using an inverted version of the linear histogram method:

$$\bar{h}_{\text{ideal}} = \frac{1}{2^N - 2} \sum_{j=1}^{2^N-2} \hat{h}_{\text{ideal}}(j) \quad (11)$$

$$INL_{DA}(i) = \sum_{j=1}^{i} \left(1 - \frac{\hat{h}_{\text{ideal}}(i)}{\bar{h}_{\text{ideal}}} \right). \quad (12)$$

The reason for using the inverted histogram method is that a high $h_{\mathrm{ideal}}(i)$ value represents a small difference between adjacent DAC output voltages, but in normal histogram testing for ADCs a high number of code occurrences means that the difference between adjacent transition voltages is large.

It should be noted that, because histograms are measured using an ADC, we get the INL of the DAC in LSB units of the ADC. For example, $INL_{DA}(i)$ is the INL estimate of a DAC at ADC code i in LSB units of the ADC, so that it is not possible to compare the estimated and actual INL curves of a DAC code by code.

The PDF of a DAC output can have very high derivatives, which are not all detected by the stimulus identification algorithm, because the numerical differentiation method and the minimum value for α are limited. If we use smaller and smaller values for α the truncation error will in theory decrease, but a smaller α make the differentiation process more noise-sensitive, an effect which limits the minimum practicable value for α. This limitation is not major problem for INL estimation, but it should be taken into account in DNL estimation. In order to estimate h'_{ideal}, and to see how much the DAC output PDF is altered when the ADC input voltage is adjusted by α LSB units, we divided the difference between the histograms by α, as in (8). Since the change detected in the PDF can occur equally as well when the DAC output is changed by one code instead of α codes, it is necessary to take this possibility into account when estimating the DNL of a DAC. We therefore use the factor α to obtain the DNL estimate:

$$DNL_{DA}(i) \quad = \quad \alpha \cdot \left(1 - \frac{\hat{h}_{\mathrm{ideal}}(i)}{\bar{h}_{\mathrm{ideal}}} \right). \qquad (13)$$

This is not the exact DNL curve of the DAC, although it can be used to estimate the maximum DNL.

The whole calculation procedure from histograms to DNL and INL estimates is shown in Table I.

IV. Simulations

The block scheme of the simulated configuration was the same as in Fig. 2. Both converters were modelled using very simple DC models. The ADCs were modelled in MATLAB using the $\mathrm{histc}(x, T_{ADC})$ function, which gives the number of input signal (x) occurrences between transition levels defined in T_{ADC}. This model gives the histograms directly as:

$$h_0 = \mathrm{histc}(x_0, T_{ADC}), \qquad (14)$$

$$h_1 = \mathrm{histc}(x_1, T_{ADC}), \qquad (15)$$

where x_0 and x_1 are the two test stimuli. The DACs were modelled using the equation

$$v_{DAC}(t) = V_{DAC}(b_{in}(t)), \qquad (16)$$

where V_{DAC} includes all DAC output voltages and $b_{in}(t)$ is the DAC input code at the time instant t. A small constant voltage was added or subtracted to generate two related versions of the test stimulus

$$x_0(t) \quad = \quad v_{DAC}(t) + V_\alpha/2 + n_1(t), \qquad (17)$$

$$x_1(t) \quad = \quad v_{DAC}(t) - V_\alpha/2 + n_2(t), \qquad (18)$$

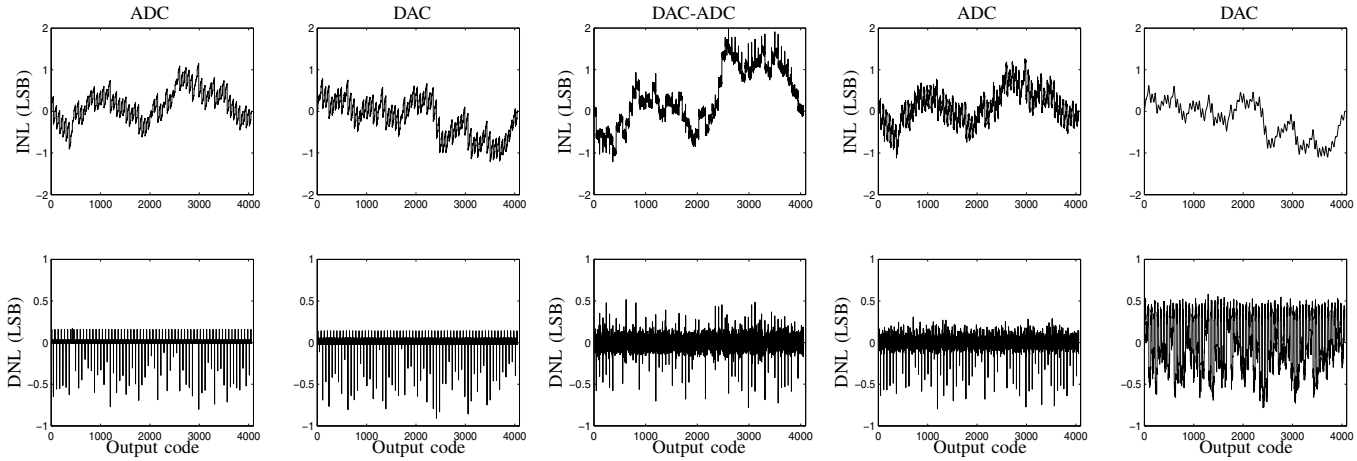
TABLE I
The Calculation Procedure, from Histograms to DNL and INL Estimates

$$\begin{aligned}
\alpha &= \frac{2\cdot(2^N-2)}{\sum_{i=1}^{2^N-2} \frac{h_1(i)+h_0(i)}{\sum_{j=0}^{i-1}(h_1(j)-h_0(j)) + \frac{h_1(i)-h_0(i)}{2}}} \\
\hat{h}_{\mathrm{ideal}}(i) &= \sum_{j=0}^{i} \frac{h_1(j)-h_0(j)}{\alpha} + \frac{h_1(i)-h_0(i)}{2\alpha} \\
\bar{h}_{\mathrm{ideal}} &= \frac{1}{2^N-2} \sum_{j=1}^{2^N-2} \hat{h}_{\mathrm{ideal}}(j) \\
CW(i) &= \frac{h_0(i)+h_1(i)}{2\cdot\hat{h}_{\mathrm{ideal}}(i)} \\
DNL_{AD}(i) &= CW(i) - 1 \\
INL_{AD}(i) &= \sum_{j=1}^{i} DNL_{AD}(j) \\
DNL_{DA}(i) &= \alpha \cdot \left(1 - \frac{\hat{h}_{\mathrm{ideal}}(i)}{\bar{h}_{\mathrm{ideal}}} \right) \\
INL_{DA}(i) &= \sum_{j=1}^{i} \left(1 - \frac{\hat{h}_{\mathrm{ideal}}(j)}{\bar{h}_{\mathrm{ideal}}} \right)
\end{aligned}$$

where $n_1(t)$ and $n_2(t)$ are the Gaussian white noise added between the converters. The simulated converters had a resolution of 12-b, and T_{ADC} and V_{DAC} included randomly generated linearity errors. (Six least significant bits were binary weighted and six most significant bits were segmented.)

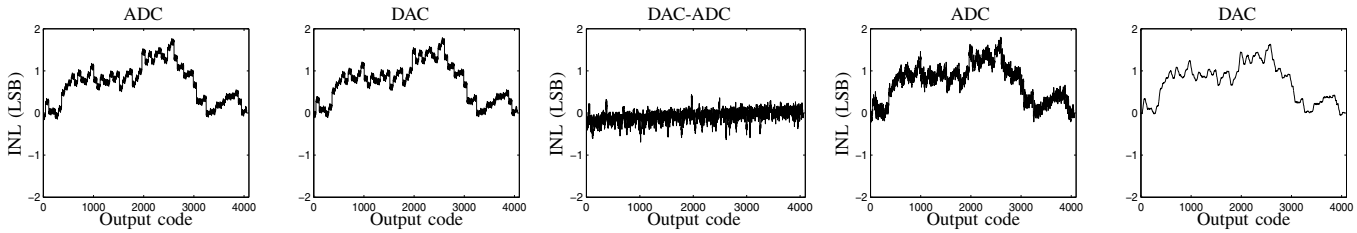
It may be seen from Fig. 3 and Fig. 4 how unreliable direct INL measurement of the DAC-ADC loop is. The actual INL of both converters in Fig. 3a is about 1 LSB, but the direct loopback measurement (Fig. 3b) indicates an INL of almost 2 LSB, whereas in Fig. 4a the actual INL of the DAC and ADC are over 1 LSB but the direct loopback measurement indicates nearly zero INL (Fig. 4b). Fig. 4 is a special case where both converters have identical transfer functions, and therefore the INL of the DAC is totally masked by the INL of the ADC. The INL of a DAC-ADC loop could be smaller or greater than that of the ADC or DAC, so that it is useless as an indicator of the INL of either converter.

We then tested how the stimulus identification algorithm performs under similar conditions. Every input code was repeated 128 times in the simulations, 64 times with $V_\alpha/2$ added to the DAC output and 64 times with $V_\alpha/2$ subtracted from the DAC output. The rms value of the noise was 0.7 LSB units and α was 40 LSBs in every simulation. Estimated INLs and DNLs for the ADC and DAC with stimulus identification algorithm are shown in Fig. 3c and 4c. The estimated INL curves are very close to the actual ones, but the INL estimate for the DAC is smoother than the actual because of limited differentiation accuracy. The DNL estimate for the ADC is quite close to the actual DNL, and that of the DAC is estimated well with respect to the peak values. The linearity of about 40 of the outermost codes is not defined, because the stimuli do not cover the whole ADC input range due to the small voltage



(a) Actual (b) Direct DAC-ADC loop (c) Stimulus identification

Fig. 3. Simulated INL and DNL measurements.



(a) Actual (b) Direct DAC-ADC loop (c) Stimulus identification

Fig. 4. Simulated INL measurement ($INL_{AD} = INL_{DA}$).

shifts.

In production testing the maximum INL and DNL values are usually measured instead of full INL or DNL curves. To simulate this scenario we used 500 randomly generated converter pairs and set α to 40 LSBs and the noise rms level to 0.7 LSB units. The actual maximum INL and DNL values for 500 converter pairs are shown in Fig. 5, together with their corresponding estimation errors. The maximum error in INL estimation is 0.44 for ADCs and -0.44 LSB units for DACs, while the corresponding DNL estimation errors are -0.15 and -0.40 LSBs. We can see from Fig. 5b that the ADC INL is slightly overestimated, whereas the DAC equivalent is underestimated to a corresponding extent. This may be attributed to the limited differentiation accuracy, as not all the details of the DAC INL are detected and they are interpreted as ADC errors.

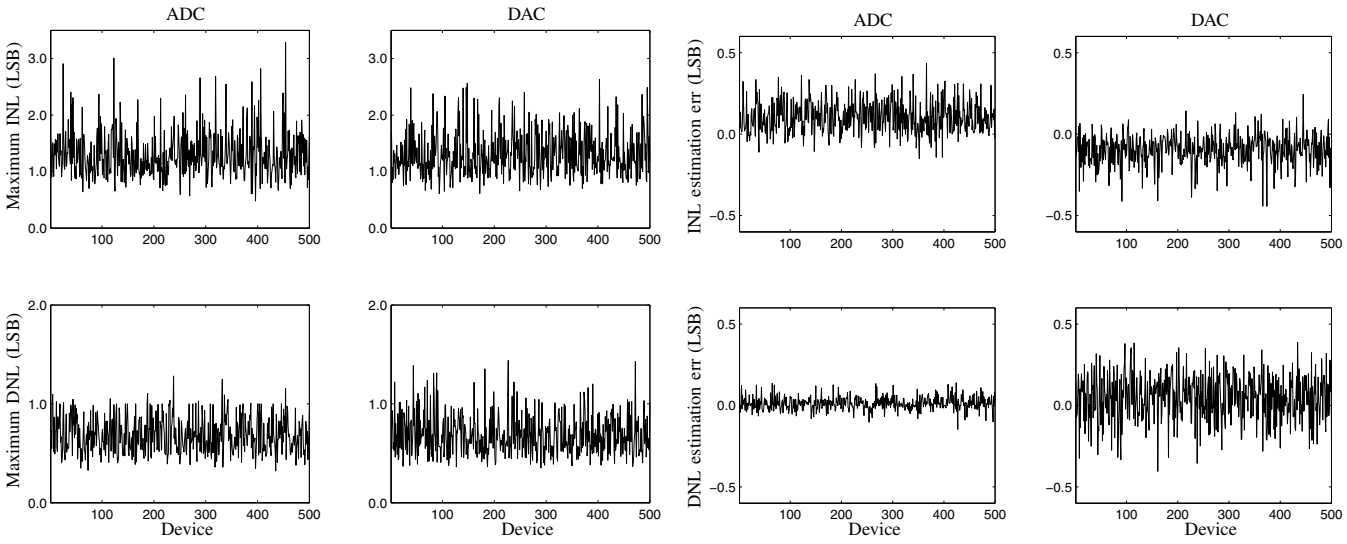
This simulation was repeated under three sets of noise conditions. The numbers of cases in which the error in maximum INL and DNL estimation was lower than the value in the leftmost column are shown in Table II. If the noise level is very low (0.1 LSB), the PDF of the DAC output will be noncontinuous and will include sharp edges, causing significant problems for the stimulus identification algorithm. When the rms level of the noise is 0.7 LSB, the PDF is more continuous and the stimulus can be detected correctly. We can see that in 99.2% of the test cases the estimation error of the INL and DNL was less than 0.4 LSB units, and the ADC DNL measurement was even more reliable. If the rms noise is 1.6 LSB units the estimation reliability will decrease slightly.

TABLE II
INL AND DNL ESTIMATION STATISTICS FOR 500 DAC-ADC PAIRS

Noise rms (LSB)	Estimation error (LSB)	Number of cases			
		ADC		DAC	
		INL	DNL	INL	DNL
0.1	< 0.1	53	114	114	58
	< 0.2	116	222	228	138
	< 0.4	233	462	358	316
	< 0.6	333	500	426	492
0.7	< 0.1	241	480	261	228
	< 0.2	415	500	441	409
	< 0.4	499	500	496	499
	< 0.6	500	500	500	500
1.6	< 0.1	154	470	221	166
	< 0.2	298	499	379	318
	< 0.4	463	500	490	494
	< 0.6	496	500	500	500

V. EXPERIMENTAL RESULTS

Our test setup is shown in Fig. 6. The ADC and DAC were both 12-b ones, and a small constant voltage was generated



(a) Actual maximum INL and DNL

(b) Estimation error of maximum INL and DNL

Fig. 5. Maximum values and estimation errors of maximum values for INL and DNL of 500 ADC-DAC pairs.

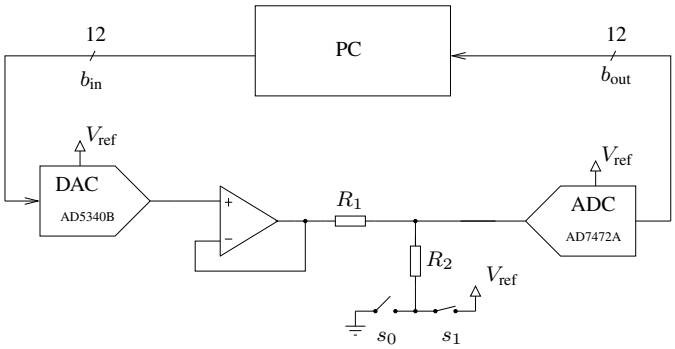


Fig. 6. Test setup.

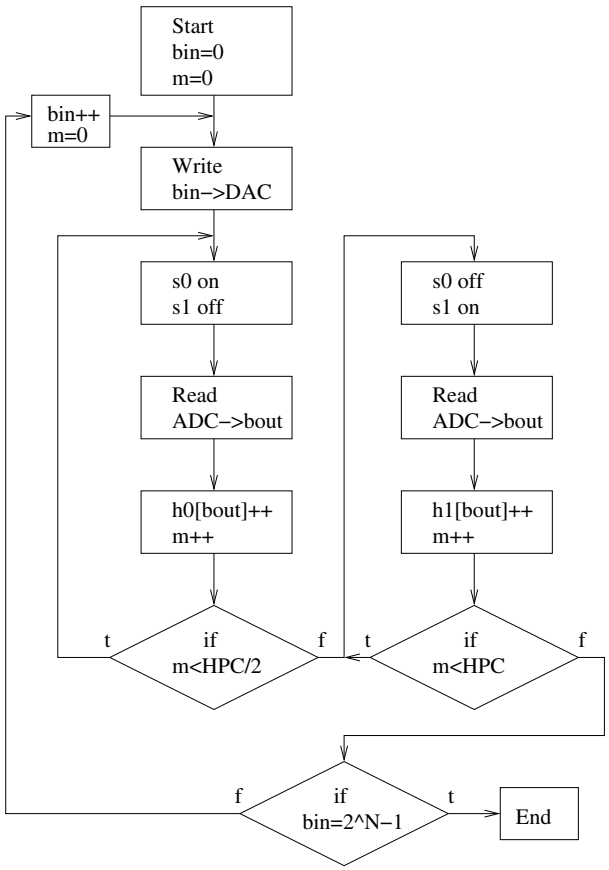


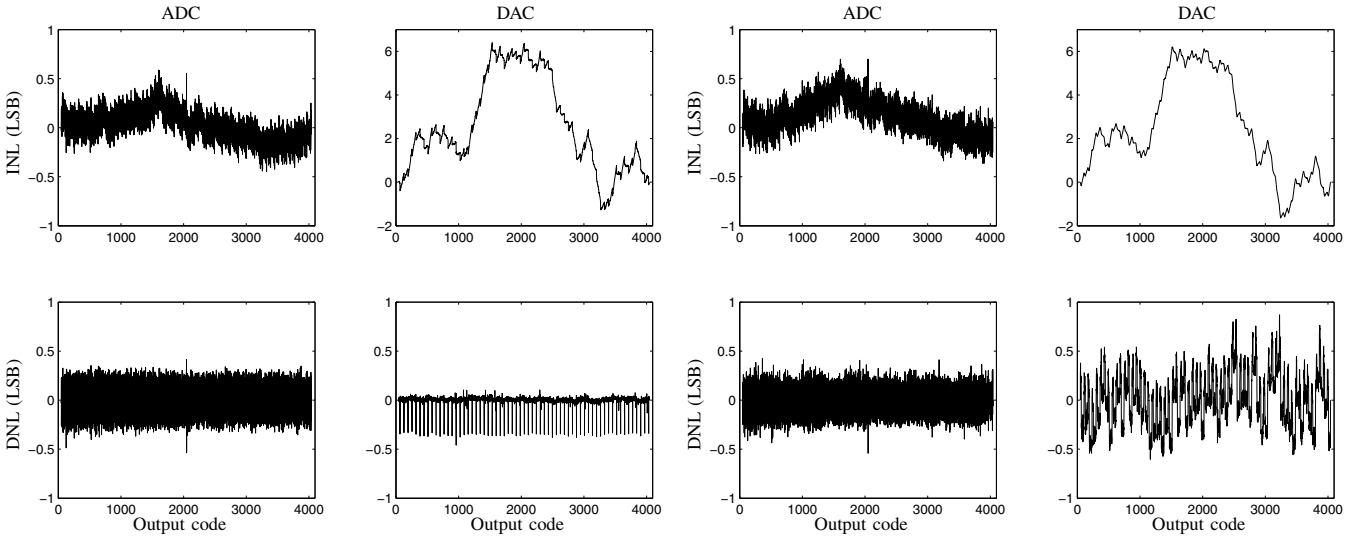
Fig. 7. Test flow.

using two CMOS switches, two resistors and a reference voltage [11]. The reference voltage was common to the ADC, DAC and voltage shifter. The operational amplifier (TL072) was used to buffer the DAC output signal. The implementation of the test process, using a personal computer and data acquisition card, is shown in Fig. 7. We can derive the test time from this flow chart as:

$$t_{\text{test}} = 2^N \left(t_{\text{s}}^{DA} + 2 \cdot (t_{\text{s}}^{RS} + \frac{HPC}{2} \cdot t_{\text{conv}}^{AD}) \right) + t_{\text{comp}}, \quad (19)$$

where N is the number of DAC bits, t_{s}^{DA} is the setup time for DAC output, t_{s}^{RS} is the setup time of resistive shifter, HPC is the number of hits per DAC code, t_{conv}^{AD} is the ADC conversion time and t_{comp} is the time required to compute the results. The minimum test time for 1 MHz 12-b converters with 256 hits per code would be about one second.

The rms value of noise measured from ADC input was 0.7 LSB units, and every DAC input code was repeated 300 times during the measurement. The actual INL and DNL for the ADC (AD7472) and DAC (AD5340) are shown in Fig. 8, together with the estimated results. The INL estimates for both converters are close to the actual ones, and so is the DNL estimation of the ADC. The DNL estimate for the DAC is not perfect, but this was predictable because it was meant to represent only the peak values. This experiment supports our



(a) Actual (b) Stimulus identification

Fig. 8. INL and DNL measured using stimulus identification algorithm.

simulations, and we can say that the maximum INL and DNL of DAC-ADC pairs can be estimated without significant fault masking problems using our stimulus identification algorithm.

VI. Discussion

It is also possible to measure the INL of other analogue blocks between a DAC and ADC using the same principle as described above. If we can add a small dc voltage shift on both the input and output side of each component to be tested, we can measure the linearity of the DAC, the linearity of the ADC and the linearity of the DAC to device under test (DUT) loop or DUT to ADC loop. It is then a straightforward process to extract the DUT linearity from these data.

VII. Conclusions

A new test method is proposed here for low-cost static linearity testing of DACs and ADCs using a loopback configuration and a stimulus identification method. This method is significantly less prone to the fault masking problems which usually affect a loopback test configuration. A single measurement gives reliable estimates for the maximum INL and DNL of both converters.

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