

QC-Fill: An X-Fill Method for Quick-and-Cool Scan Test

Chao-Wen Tzeng Shi-Yu Huang

EE Dept., National Tsing-Hua University, Taiwan

cwtzeng@larc.ee.nthu.edu.tw syhuang@ee.nthu.edu.tw

Abstract — In this paper, we present an *X-Fill (QC-Fill)* method for not only slashing the test time but also reducing the test power (including both capture power and shifting power). *QC-Fill*, built upon the existing multicasting scan architecture, can coexist with most low-capture-power (LCP) X-fill methods through a *multicasting-driven X-fill* method incorporating a *clique-stripping scheme*. *QC-Fill* is independent of the ATPG patterns and does not require any area-overhead since it can directly operate on an existing scan architecture incorporating test compression.

Index Terms—Scan Test, Multicasting, Test Compression, Low-Power Scan, Low-capture-power X-fill

I. INTRODUCTION

The power consumed by a chip during the scan testing has been reportedly much higher than that during the functional operation, and this phenomenon could cause power-induced test yield loss or even chip damage. Therefore, low-power testing has received great attention recently [10]. The scan test power is often divided into either *shifting power* (i.e., the power consumed during the scan shifting operations) or *capture power* (i.e., the power consumed during the response capture cycle).

The shifting power in a chip with multiple scan chains can be reduced by several schemes, e.g., by scan chain reordering [10], by augmenting the scan cells with output gating capability to keep the transition from rippling through the core logic during scan shifting [11]. *Adjacent-Fill* (or called minimum-transition fill) assigns the most recent care-bit value repeatedly to a string of X-bits so as to keep the transition small during the scan shifting [3][18][20]. When appropriate, one can freeze the clock signals for those inactive scan chains to cut down unnecessary power [2][19][21]. In general, these approaches jointly could reduce the shifting power to a satisfactory level.

Similarly, numerous schemes have also been proposed to address the Low Capture Power (LCP) problem, for both the average power and the peak power. [20] proposed an LCP-conscious test pattern modification process that can eliminate those test vectors that cause violation of a predefined peak power limit. [12] added some delay elements so that response capturing of the FF's could spread out and thereby reducing the peak power. [13] introduced a concept called *multiple capture order* that successfully reduces the capture power substantially by dividing the capture process in stages. [17] utilized sophisticated clocking scheme to conduct response capturing to the scan cells in multiple phases, under

the support of so-called *hold registers* to break the data dependency between scan cells. More recently, [7] proposed a *RISC cell* (i.e., Response Inversion Scan Cell) to perform selective inversion to suppress the transition amounts at the outputs of the scan cell during the capture cycles. Since the excessive peak power often has an even more profound adverse effect during an at-speed scan test by causing severe IR drops, several works have been aimed at producing low capture power test patterns by specific rules indicating what values should be assigned to certain don't-care bits (X-bits) so that the number of transitions at the outputs of scan cells in the capture mode is minimized [16][25][26].

To cope with the scan test power issues in the test compression environment, the three main test compression categories [24]: (1) *coding-based schemes*, (2) *linear decompression-based schemes* and (3) *broadcast-based schemes* have developed their own solutions.

The low power coding-based schemes [4][5] used Golomb or alternating run-length codes with careful mapping of the don't-care bits in test sets to 1's and 0's leads to significant savings in peak and average shifting power.

For the low power linear-decompression-based schemes, [8][15] employ the feature of LFSR or add additional control signal and shadow registers to keep the state of LFSR unchanged to minimize the shift-in data transition counts.

The low power scan test integrated with the broadcast-based schemes is proposed in [6]. With modest combinational area-overhead and modification on the scan architecture, the average switching activities induced by shift-in data can be reduced significantly. [14] used multilayer mux-arrays to reuse the last shift-in data to achieve test compression and low shifting power. The extension of broadcast-based scheme is called as *multicasting scan* [22]. [1] proposed *Segmented Addressable Scan* (SAS) architecture to provide dynamic configurations by incorporating some address control data. The architecture not only reduces test data volume and test time but also reduces the average shifting power consumption during test application by selectively activating the scan chains that need to be loaded while disabling the clocking to the other scan chains. [23] proposed *Universal Multicasting Scan* (UMC-Scan) to improve the test compression ratio by providing the maximal freedom in multicasting. However, the multicasting scan architectures like [1][23] may result in higher peak shifting power when the broadcasting mode is operated (i.e., when a test pattern is broadcast to all scan chains). These approaches can reduce the scan shifting power, but not the capture power. Therefore, good low-capture-power scan methodology that can coexist with the popular test

compression schemes are still in need.

In this paper, we propose a new X-fill method called *Quick-and-Cool X-fill* (QC-Fill) aiming at reducing the test time and the test power either in shifting mode or in capture mode. We make contribution in leveraging the existing *low capture power X-fill* (LCP-Fill) methods into the multicasting scan architecture. Since low-power and test compression are often achieved by exploiting the flexibility provided by the X bits in the test patterns, we need a balanced treatment to compromise the two requirements. In our *multicasting-driven X-fill* method, the *clique stripping* scheme provide such a compromise. In summary, our method has the following features: (1) it is built upon the multicasting scan architectures, (2) it can reduce shifting power and capture power with the modest loss on test compression ratio, (3) it is independent of the ATPG patterns, and (4) it does not require any modification to the scan architecture.

The rest of this paper is organized as follows. Section 2 depicts the underlying scan architecture and introduces the basic power metrics in use. Section 3 introduces the overall QC-Fill methodology. Section 4 presents the experimental results, and Section 5 concludes.

II. BASIC ARCHITECTURE AND POWER METRICS

A. Multicasting Scan Architecture

Fig. 1 shows the multicasting scan architecture called *UMC-Scan* [23]. The data input of the single test channel is connected to an Universal Multicasting controller which directs an incoming test sub-patterns to a specific group of compatible scan chains under the support of a column of *clock-gating logic* as shown.

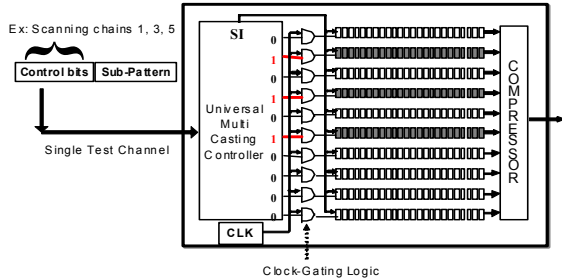


Fig. 1: Universal Multi-Casting (UMC) scan architecture.

To avoid confusion, we refer to a *test pattern* as the value combination of all flip-flops in all scan chains, while a *sub-pattern* as the value combination of the scan cells in a *compatible group of scan chains*, or *compatible group* for short. In other words, to flush a test pattern into the multiple scan chains in a chip, we will partition it into several test sub-patterns; each of which is cast to its designated set of scan chains. Note that a test sub-pattern is now augmented with some pilot *control bits* to define the scan chains that should receive that specific test sub-pattern. These control bits are to be inserted by our methodology after compatibility analysis and encoding.

The multicasting scan architectures such as SAS [1] or UMC-Scan [23] can provide effective average shifting power reduction because the nature of their scan operation - *selectively activating the scan chains that need to be loaded*

while disabling the clocking to the other scan chains. However, they still result in high peak shifting power since from time to time when the broadcasting mode is operated all scan chains are active at the same time. Such a phenomenon was also observed in [6]. In light of this, our QC-Fill method will incorporate a clique stripping scheme to cope with the peak shifting power issue later.

B. Basic Power Metrics

To evaluate the power dissipation effectively, several metrics have been proposed. For shifting power evaluation, the switching activity can be estimated by so-called *weighted transition metric* (WTM) [18] that not only counts the number of induced transitions in successive scan cells, but also takes into account their relative positions. Let l be the length of a scan chain, and $T = b_1b_{l-1} \dots b_2b_1$ represents a test sub-pattern with bit b_i scanned in before b_{i+1} . The power metric in the shifting mode is defined as follows:

$$PM_{shift} = \sum_{i=1}^{l-1} ((l-i)(b_i \oplus b_{i+1})) \quad (1)$$

Where the multiplicative factor $(l-i)$ is the weight associated with i -bit position in a scan chain with the index, ordering from the scan output towards the scan input. Then let n be the total number of test patterns:

$$\text{Avg. Shifting Power Metric} = \frac{\sum_{j=1}^n PM_{shift,j}}{n}$$

$$\text{Peak Shifting Power Metric} = \text{MAX}\{PM_{shift,1}, PM_{shift,2}, \dots, PM_{shift,n}\}$$

The capture power is more related to the total number of differences between a test pattern and its responses pattern. Let s be the total number of scan cells in a scan chain, $T = b_1b_{l-1} \dots b_2b_1$ represents a test sub-pattern and $R = b_1b_{l-1} \dots b_2b_1$ represents a test response sub-pattern. The metric for the capture power is defined as follows:

$$PM_{capture} = \sum_{i=1}^l (b_{T,i} \oplus b_{R,i}) \quad (2)$$

III. QC-FILL METHODOLOGY

The overall QC-Fill flow is shown in Fig. 2. To aim at reducing test time and test power simultaneously, a set of techniques are in need: (1) *low power driven maximal-clique partition*, (2) *multicasting-driven X-fill* and (3) *clique stripping for low capture power (LCP) and low shifting power (LSP)*.

A. Low Power Driven Maximal-Clique Partitioning

The compatibility analysis for a test pattern with X bits can be modeled as a graph, in which a vertex represents a scan chain, and an edge connecting two vertices represents a compatible relation – denoting that the test sub-patterns of these two scan chains are bit-by-bit compatible. Next, we conduct *maximal-clique partitioning* to partition the graph into a minimum number of cliques, where a *clique* is a fully compatible set of vertices in which every two vertices has an edge in between. However, the priority of vertex selection for traditional *maximal-clique partitioning* algorithm is based on the degree level of each scan chain, which presents the

compatible number of a scan chain. For low-power consideration, we modify the selection criterion by using *Potential Weighted Transition Metric* (PWTM) as defined in Eq. 3. The difference between WTM and PWTM is that PWTM introduces an additional parameter to handle the X bits in the original scan data. For each bit, we use an additional parameter α to present the *potential transition parameter*, which sits in a range between 0.5 and 1. When α is 1, it means that its corresponding bit has been deterministically decided as either '0' or '1'. On the other hand, when α is 0.5, it means that its corresponding bit is still a don't-care.

$$PWTM = \sum_{i=1}^{l-1} ((l-i)(b_i \oplus b_{i+1})(\alpha_i \times \alpha_{i+1})) \quad (3)$$

$$\alpha_i = \begin{cases} 1.0 & b_i = 0 \text{ or } 1 \\ 0.5 & b_i = X \end{cases}$$

Table 1 shows the PWTM associated with an original test pattern for a design with four scan chains. It is notable that when two consecutive bits are both don't-care, it is assumed that there is no transition between them. In this test pattern, the PWTM for the four scan chains are (9.5, 0, 0, 5), respectively. During the maximal-clique partitioning process, a scan chain with a higher PWTM is assigned to have a higher resistance of being included in a clique. Such a heuristic is useful in maintaining a power-balanced partitioning in which no power-hungry clique will be formed.

Table 1: Illustration of potential weighted transition metric

	Scan Data								Potential-WTM
	FF ₈	FF ₇	FF ₆	FF ₅	FF ₄	FF ₃	FF ₂	FF ₁	
Chain ₁	X	X	1	0	X	X	X	1	$7 \times 0.5 + 4 \times 0.5 + 3 + 2 \times 0.5 = 9.5$
Chain ₂	X	X	X	X	X	X	X	X	0
Chain ₃	X	X	X	X	X	X	X	X	0
Chain ₄	X	X	X	X	1	1	X	X	$6 \times 0.5 + 4 \times 0.5 = 5$

B. Multicasting-Driven X-Filling

In general, the LCP-Fill methods assign each X-bit using certain specific power metric and signal probability as the guideline, and each X-bit is decided independently. In this work, we combine the multicasting scan architecture and the data filled by the general LCP-Fill methods by considering the dependency among *cousin X-bits* (i.e., those X-bits with the same bit position in compatible scan chains belonging to a clique).

There are three main steps in this multicasting-driven X-filling scheme:

(Step1): (LCP step) Fill all X-bits of an original test pattern using a basis LCP-Fill method. We call the result of the completely filled pattern as *LCP data*. Note that this data will be used as the guidance in step 3 later.

(Step2): (Test compression step) On the original test pattern again, fill the X-bits for enabling multicasting using the above discussed maximal-clique-partitioning in order to achieve reasonably good test compression. The result of this partially filled test pattern is called *compressed data*.

(Step3): (Mixing step) Fill the remaining X bits in the compressed data using the LCP data as the guideline. As we

mentioned previously, it is important in our X-filling process that we consider all cousin X bits simultaneously.

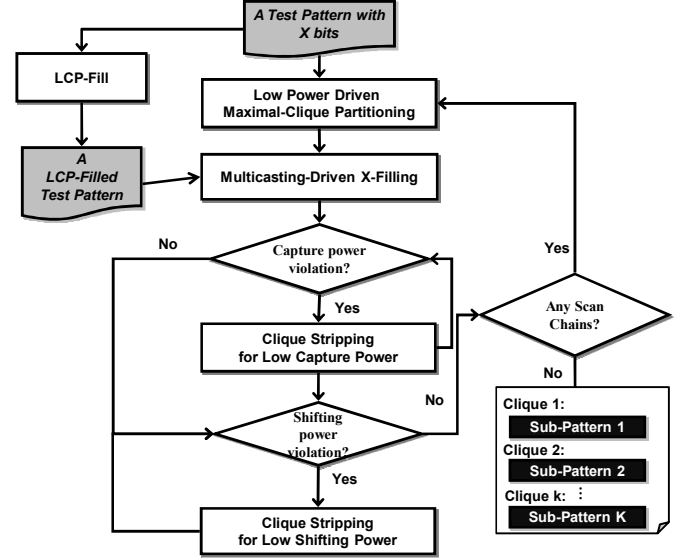


Fig.2: Overall QC-Fill flow.

Let us consider the X-filling of a clique with k scan chains. We use a guiding metric called *Capture Violation Impact* (CVI), as defined below to decide whether a set of cousin X-bits should be assigned to '0' or '1':

$$CVI_i(x=0) = \sum_{c=1}^k ((0 \oplus b_{LCP-data, c, i}) \times (\text{Fanout_Num}_{c, i})) \quad (4)$$

$$CVI_i(x=1) = \sum_{c=1}^k ((1 \oplus b_{LCP-data, c, i}) \times (\text{Fanout_Num}_{c, i}))$$

where c represents the scan chain index. The $b_{LCP-data, c, i}$ represents the bit value of scan cell i in scan chain c in the LCP data. For those k cousin X-bits at bit position i , they are all assigned to either '0' or '1' depending on $CVI_i(x=0)$ and $CVI_i(x=1)$. If $CVI_i(x=0) > CVI_i(x=1)$, we fill '1' to these k cousin X bits. Otherwise, we fill '0'. The result of the completely filled data is called *provisional QC-data*. In some sense, we attempt to do test compression while making the result as similar to an LCP-based test pattern as possible. Before we illustrate the multicasting-driven X-fill process, we define two terminologies firstly.

Definition 1: (LCP-failing Scan Cell) When there is a bit mismatch between the LCP data and the provisional QC-data, the corresponding scan cell is called *LCP-failing scan cell*.

Definition 2: (Total LCP-failing Impact) When evaluating if a provisional QC-data meets the pre-defined capture power constraint, we simply sum up the impact resulting from these LCP-failing scan cells as an indicator.

Example 1: (Multicasting-Driven X-Filling) Fig.3 shows the original test pattern, its LCP-data, which is generated by using a generic LCP-Fill method, and compressed data. In this example, there are four scan chains $\{chain_1, chain_2, chain_3, chain_4\}$, each of which is 8-bit long. After the compatibility analysis, the four chains are found all compatible with one another and the compressed test data is also shown in Fig. 3, in which the original care-bits are marked in underline. Then, we

fill the remaining X-bits in the compressed test data by using LCP data as the guideline. Let us take scan cells numbered 2 among the four scan chains as example assuming that the numbers of fan-outs are all 1 for all scan cells. The CVI can be calculated as follows:

$$CVI_2(x=0) = (0 \times 1) + (0 \times 1) + (0 \times 1) + (1 \times 1) = 1$$

$$CVI_2(x=1) = (1 \times 1) + (1 \times 1) + (1 \times 1) + (0 \times 1) = 3$$

Because the $CVI_2(x=0) < CVI_2(x=1)$, it means that setting these cousin X-bits to 0 will lead to less mismatch with the LCP-data, and therefore, we fill these four X bits with '0'. But, $Cell_{4,2}$ (i.e., the 2nd cell in scan chain 4) is still an LCP-failing scan cell since it is different from its counterpart in the LCP-data. After filling all X bits, there are 11 LCP-failing scan cells $\{Cell_{1,7}, Cell_{2,1}, Cell_{2,3}, Cell_{2,5}, Cell_{2,6}, Cell_{3,1}, Cell_{3,4}, Cell_{3,5}, Cell_{3,6}, Cell_{4,1}, Cell_{4,2}\}$, implying that the *Total LCP-failing Impact* is 11 in this case, as shown in Fig. 4(a). Whenever the *Total LCP-failing Impact* exceeds a pre-defined capture power constraint, the following *clique stripping for LCP* will be further conducted.

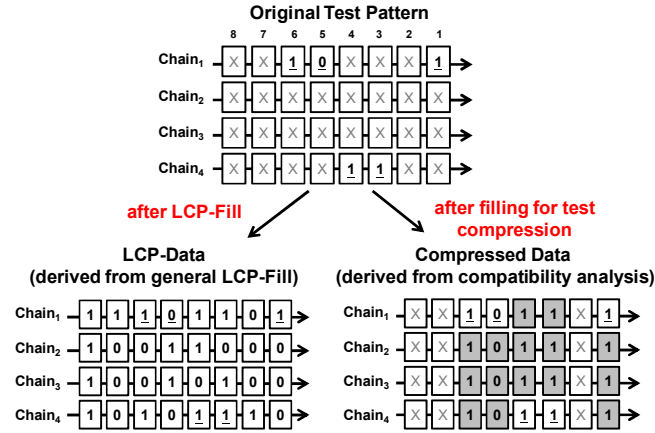


Fig. 3: Illustration of original test pattern, LCP-data, and compressed data.

C. Clique Stripping for Low Capture Power

The *clique stripping* is to remove a number of scan chains from a given clique so that the resulting one will meet a pre-defined power constraint. It is called clique stripping since it will strip a high-capture-power clique into several cliques of lower capture power. This problem involves a good selection mechanism since we need to identify those scan chains that cause the high capture power. Once identified, they will be stripped from the current clique and form a new clique of its own, while the scan chains left in the original clique will consume less capture power. In our multicasting-driven X-filling, an X-bit turns into its deterministic value (either '0' or '1') in two steps, either the test compression step or the mixing step. Both one of these two steps could cause mismatch with the LCP-data, and thus creating LCP-failing scan cells.

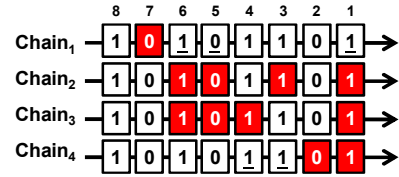
Definition 3: (*LCP-violation Contribution Factor*) This metric is defined for each scan chain, representing the total amount of LCP-failing scan cells that a scan chain should be held responsible. Such LCP-failing scan cells could occur in either the test compression step or the mixing step. Next, we use an example to explain its meaning.

Example 2: (*LCP-violation Contribution Factor & Clique Stripping for LCP*) Table 2 shows the result of the

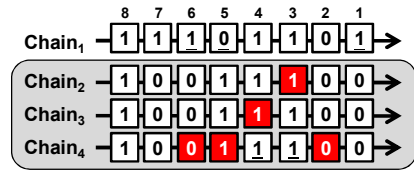
LCP-violation Contribution Factor for each scan chain for the test pattern shown in Fig. 3. Considering the test data of $chain_1$, there are three care-bits, i.e., $Cell_{1,1}$, $Cell_{1,5}$ and $Cell_{1,6}$. In the test compression step, each of these three care-bits forces their cousin bits to comply with them, and thereby creating 7 LCP-failing scan cells, including $\{Cell_{2,1}, Cell_{3,1}, Cell_{4,1}\}$, $\{Cell_{2,5}, Cell_{3,5}\}$, and $\{Cell_{2,6}, Cell_{3,6}\}$. In the mixing step, one of its known bit, at cell $Cell_{1,7}$, was assigned to '0', which is against its LCP value, '1'. Overall, the *LCP-violation Contribution Factor* of $chain_1$ is thus $(7+1) = 8$. In other word, $chain_1$ is held responsible to 7 LCP-failing assignments in the test compression step and 1 LCP-failing assignment in the mixing step. The scan chain with the largest *LCP-violation contribution factor* is removed from the clique. In this example, $chain_1$ is selected as the major capture power contributor. Fig. 4(b) shows the result after clique stripping. We put $chain_1$ into an independent clique and then perform the multicasting-driven X-filling again. Finally, as shown in Fig. 4(b), the total number of LCP-failing scan cells can be reduced from 11 to 5.

Table 2: Illustration of LCP-violation contributor factor computation

Chain Index	LCP-failing Case	LCP-failing Scan Cell List	LCP-violation Contribution Factor
Chain ₁	Case1	Cell _{2,1} , Cell _{3,1} , Cell _{4,1} , Cell _{2,5} , Cell _{3,5} , Cell _{2,6} , Cell _{3,6}	7 + 1 = 8
	Case2	Cell _{1,7}	
Chain ₂	Case1	None	0
	Case2	None	
Chain ₃	Case1	None	0
	Case2	None	
Chain ₄	Case1	Cell _{2,3} , Cell _{3,4}	2 + 1 = 3
	Case2	Cell _{2,4}	



(a) Provisional QC-data before clique stripping



(b) Provisional QC-data after clique stripping

Fig. 4: Illustration of clique stripping for low capture power (LCP).

D. Clique Stripping for Low Shifting Power

To cool down the shifting power, the stripping priority goes with the *PWTM* (*Potential Weighted Transition Metric*). The scan chain with the highest PWTM will be removed first from a clique violating the power constraint.

Example 3: (*Clique Stripping for LSP*) Fig. 5 demonstrates the results with and without clique stripping for low shifting power (LSP). Fig. 5(a) shows that the original peak WTM is 30. If $clique_1$ containing $\{chain_2, chain_3, chain_4\}$ violates the predefined WTM constraint, we will conduct the clique stripping process. Fig. 5(b) shows the result. Since we found in this example that $chain_4$ has the highest PWTM in $clique_1$, it is removed first. Then, the maximal-clique partitioning is

processed again over the other scan chains to form *clique*₂ containing {*chain*₁, *chain*₄}. Finally, we found that the peak WTM can be reduced from 30 to 18.

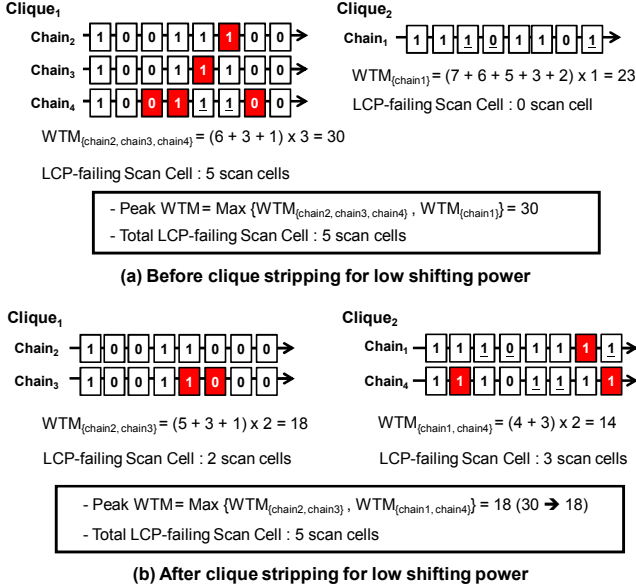


Fig. 5: Illustration of clique stripping for low shifting power (LSP).

IV. EXPERIMENTAL RESULTS

In our experiments, *QC-Fill* uses *Preferred Fill* [16] as our basis low-capture-power algorithm and *UMC-Scan* [23] as our underlying test compression scheme.

We have evaluated the proposed method by three real designs with the gate count ranging from 68K to 268K, as shown in Table 3. We use *TetraMAX* for test pattern generation and *PrimePower* for power estimation, both are from *Synopsys*. The clock frequency is set to 10MHz for the scan test.

Table 3: Benchmark circuits in our experiments

Design	Gate Count	FF No.	Pattern No.	Care-Bit Ratio (%)
Design1	68K	2807	216	5.0%
Design2	268K	4352	571	2.3%
Design3	155K	12443	724	1.2%

Table 4 shows the results on power reduction as compared to four other methods, namely *Random-Fill*, *Adjacent-Fill*, *Preferred-Fill*, and *UMC-Scan with direct LCP-fill*. For the comparison on power consumption, we use the *Random-Fill* method as the reference. For comparing the test compression ratio with other X-fill methods, we use *UMC-Scan* to compress the fully specified test patterns filled by different X-fill methods, as shown in Table 5.

A. *Random-Fill* vs. *QC-Fill*

The results of power consumed with *Random-Fill* can approximately stand for the result of LFSR-based test compression schemes. LFSR-based test compression schemes can provide excellent test compression ratio. However, the test power would be an issue. *QC-Fill* can save 39.6%, 27.7%, 88.8%, and 42.1% power consumption for average *capture*

power, *peak capture power*, *average shifting power* and *peak shifting power* respectively, when comparing to *Random-Fill*.

Table 4: Results on capture power, shifting power

Design	Method	Capture Power (mW) (reduction %)		Shifting Power (mW) (reduction %)	
		Avg. Power	Peak Power	Avg. Power	Peak Power
Design1	Random-Fill	9.78 (100%)	221.1 (100%)	34.26 (100%)	257.8 (100%)
	Adjacent-Fill	7.11 (-26.5%)	211.3 (-4.4%)	15.66 (-53.6%)	215.4 (-16.4%)
	Preferred-Fill	5.42 (-44.6%)	184.3 (-16.6%)	12.58 (-63.3%)	190.0 (-26.3%)
	UMC-Scan	8.95 (-8.5%)	209.1 (-5.4%)	7.54 (-78.0%)	254.4 (-1.3%)
	QC-Fill	6.05 (-38.1%)	186.0 (-15.9%)	3.90 (-88.6%)	193.4 (-25.0%)
Design2	Random-Fill	28.77 (100%)	1680.0 (100%)	71.76 (100%)	1540.0 (100%)
	Adjacent-Fill	13.79 (-52.1%)	1642.0 (-2.3%)	18.36 (-74.4%)	674.5 (-56.2%)
	Preferred-Fill	12.08 (-58.0%)	1023.0 (-39.1%)	30.26 (-57.5%)	919.1 (-40.3%)
	UMC-Scan	13.77 (-52.1%)	1319.0 (-21.5%)	5.57 (-92.2%)	1112.0 (-27.8%)
	QC-Fill	13.16 (-54.3%)	1118.0 (-33.5%)	4.97 (-93.1%)	919.6 (-40.3%)
Design3	Random-Fill	7.99 (100%)	483.4 (100%)	32.56 (100%)	872.5 (100%)
	Adjacent-Fill	6.41 (-19.7%)	285.2 (-41.0%)	17.06 (-47.6%)	207.5 (-76.2%)
	Preferred-Fill	5.28 (-33.9%)	256.2 (-47.0%)	16.43 (-49.5%)	282.6 (-67.6%)
	UMC-Scan	7.02 (-12.1%)	475.8 (-1.6%)	6.69 (-79.5%)	746.7 (-14.4%)
	QC-Fill	5.87 (-26.5%)	320.5 (-33.7%)	5.00 (-84.6%)	339.8 (-61.1%)

Table 5: Results on test compression with different x-fill methods

Design	Test Compression (X)			
	Adjacent-Fill (LSP-Fill)	Preferred-Fill (LCP-Fill)	UMC-Scan	QC-Fill
Design1	5.6X	3.1X	9.7X	8.6X
Design2	16.9X	2.6X	29.0X	28.6X
Design3	17.5X	6.0X	54.8X	44.1X

B. *Adjacent-Fill* vs. *QC-Fill*

Adjacent-Fill (or called *Minimum Transition Fill*) [3][18][20] is a well-known method for shifting power reduction. However, it may result in higher capture power in some cases shown in our experiments. As compared to *Adjacent-Fill*, although *Adjacent-Fill* provides higher reduction on the peak shifting power (44.7%) than our *QC-Fill* (42.1%) for the three designs, *QC-Fill* improves the average shifting power reduction from 58.5% to 88.8%. As for the capture power, ours can improve the average and the peak capture power from 32.8% to 39.6% and 15.9% to 27.7%, respectively. In addition to lower power consumption, our *QC-Fill* also achieves much higher test compression ratio over the *Adjacent-Fill*. For example, the compression ratio is only 17.5X for design 3 using *Adjacent-Fill*, while boosted to 44.1X using ours.

C. *Preferred-Fill* vs. *QC-Fill*

In our experiments, we found that *Preferred-Fill* does maintain the highest capture power reduction among all methods. However, without incorporating the techniques proposed in this paper, the test compression ratio of it when integrated with the most flexible *UMC-scan* drops significantly from 54.8X to 6.0X for design 3. On the other hand, our *QC-Fill* can still maintain a good test compression ratio as high as 44.1X without sacrificing much power reduction.

D. *UMC-Scan* vs. *QC-Fill*

UMC-Scan provides the highest test compression ratio for all cases. However, it may induce higher peak shifting power when the broadcasting mode is operated. Comparatively, *QC-Fill* improves the peak shifting power from 14.5%

reduction to 42.1% reduction and the peak capture power reduction from 9.5% reduction to 27.7% reduction, while providing effective test compression ratio.

V. CONCLUSION

Existing low capture power X-fill methods and the multicasting scan architecture have been proven quite successful for reducing capture power and test time, respectively. However, there is rare work to link the two methodologies together successfully. In this paper, we made two contributions. First, we provide a formulation that allows any low capture power X-fill method (e.g., the most recently Preferred-Fill) to be integrated with the multicasting scan architecture. The major techniques we propose in this paper include the multicasting-driven X-fill and the clique-stripping scheme. Secondly, with the clique stripping support, the peak shifting power issue in broadcast mode of the multicasting scan architecture can also be well controlled. Experimental results indicate that *QC-Fill* can achieve up to 44.1X test compression ratio in both test data volume and test time for a real design with 1.2% care bit ratio in the test set and save 39.6% and 88.8% power consumption on the average capture power and shifting power for three real designs.

ACKNOWLEDGEMENTS

We are grateful to *CIC (Chip Implementation Center)* [27], Taiwan, for their help in providing the needed commercial tools, including *TetraMAX*, *Verilog-XL*, and *PrimePower* used in our experiments. We also thank Prof. C.-W. Wu and Prof. T.-Y. Chang from Tsing-Hua Univ., Taiwan, for providing us the designs they developed for being used in our experiments.

REFERENCES

- [1] A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, and M. Grinchuk, "Scan Test Cost and Power Reduction Through Systematic Scan Reconfiguration," *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 5, pp. 907-917, May 2007.
- [2] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, "A Gated Clock Scheme for Low Power Scan Testing of Logic ICs or Embedded Cores," *Proc. of Asian Test Symp.*, pp. 253-258, 2001.
- [3] K. M. Bulter, J. Saxena, T. Fryars, G. Hetherington, A. Jain, and J. Lewis, "Minimizing Power Consumption in Scan Test: Pattern Generation and DFT Techniques," *Proc. of Int'l Test Conf.*, pp. 355-364, 2004.
- [4] A. Chandra, and K. Chakrabarty, "Combining Low-Power Scan Testing and Test Data Compression for System-on-a-Chip," *Proc. of IEEE/ACM Design Automation Conf.*, pp. 166-169, 2001.
- [5] A. Chandra, and K. Chakrabarty, "A Unified Approach to Reduce SoC Test Data Volume, Scan Power and Testing Time," *IEEE Trans. on Computer-Aided Design*, Vol. 22, pp. 352-362, March 2003.
- [6] A. Chandra, F. Ng, and R. Kapur, "Low Power Illinois Scan Architecture for Simultaneous Power and Test Data Volume Reduction," *Proc. of IEEE/ACM Design Automation and Test in Europe Conf.*, March 2008.
- [7] B.-H. Chen, W.-C. Kao, B.-C. Bai, S.-T. Shen, and C.-M. Li, "Response Inversion Scan Cell (RISC): A Peak Capture Power Reduction Technique," *Proc. of Asian Test Symp.*, pp. 425-430, Oct. 2007.
- [8] D. Czych, G. Mrugalski, J. Rajska, and J. Tyszer, "Low Power Embedded Deterministic Test," *Proc. of VLSI Test Symp.*, 2007.
- [9] R. V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. M. Reddy, "Techniques for Reducing Power Dissipation During Test Application in Full Scan Circuits," *IEEE Trans. on Computer-Aided Design*, Vol. 17, No. 12, pp. 1925-1933, Dec. 1998.
- [10] P. Girard, "Survey of Low-Power Testing of VLSI Circuits," *IEEE Design and Test of Computers*, pp. 82-92, May-June 2002.
- [11] A. Hertwig and H. J. Wunderlich, "Low-Power Serial Built-In Self Test," *Proc. of European Test Workshop*, pp. 49-53, 1998.
- [12] K.-J. Lee, T.-C. Huang, and J.-J. Chen, "Peak-Power Reduction for Multiple-Scan Circuits during Test," *Proc. of Asian Test Symp.*, pp. , 2000.
- [13] K.-J. Lee, S.-J. Hsu, and C.-M. Ho, "Test Power Reduction with Multiple Capture Order," *Proc. of Asian Test Symp.*, pp 26-31, Nov. 2004.
- [14] S.-P. Lin, C.-L. Lee, J.-E. Chen, K.-L. Luo, and W.-C. Wu, "A Multiplayer Data Copy Test Data Compression Scheme for Reducing Shifting-in Power for Multiple Scan Design," *IEEE Trans. on Very Large Scale Integration (VLSI) System*, vol. 15, no. 7, July 2007.
- [15] G. Mrugalski, J. Rajska, D. Czych, and Jerzy Tyszer, "New Test Data Decompressor for Low Power Applications," *Proc. of IEEE/ACM Design Automation Conf.*, pp. 539-544, June 2007.
- [16] S. Remersaro, X. Lin, Z. Zhang, S.M. Reddy, I. Pomeranz, and J. Rajska, "Preferred Fill: A Scalable Method to Reduce Capture Power for Scan Based Designs," *Proc. of Int'l Test Conf.*, Oct. 2006.
- [17] P. Rosinger, B. M. Al-Hashimi, and N. Nicolici, "Scan Architecture With Mutually Exclusive Scan Segment Activation for Shift- and Capture-Power Reduction," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 7, pp. 1142-1153, July 2004.
- [18] R. Sankaralingam, R. R. Oruganti, and N. A. Touba, "Static Compaction Technique to Control Scan Vector Power Dissipation," *Proc. of VLSI Test Symp.*, pp. 35-40, 2000.
- [19] R. Sankaralingam, B. Pouya, N. A. Touba, "Reducing Power Dissipation During Test Using Scan Chain Disable," *Proc. of VLSI Test Symp.*, pp.319-324, April 2001.
- [20] R. Sankaralingam, and N. A. Touba, "Controlling Peak Power During Scan Testing," *Proc. of VLSI Test Symp.*, pp. 153-159, May 2002.
- [21] J. Saxena, K. M. Butler, and L. Whetsel, "An Analysis of Power Reduction Techniques in Scan Testing," *Proc. of Int'l Test Conf.*, pp. 670 - 677, Sept. 2001.
- [22] P.-C. Tsai and S.-J. Wang, "Multi-Mode Segmented Scan Architecture with Layout-Aware Scan Chain Routing for Test Data and Test Time Reduction," *Proc. of IEEE Asian Test Symp.*, pp. 225-230, Nov. 2006.
- [23] C.-W. Tzeng, and S.-Y. Huang, "UMC-Scan Test Methodology: Exploiting the Maximum Freedom of Multicasting," *IEEE Design and Test of Computers*, Vol. 25, No. 2, pp. 132-140, March-April, 2008.
- [24] L.-T. Wang, C.-W. Wu, and X. Wen, "Design for Testability: VLSI Test Principles and Architectures", Elsevier (Morgan Kaufmann), 2006.
- [25] S.-J. Wang, Y.-T. Chen, and S.-M. Li, "Low Capture Power Test Generation for Launch-off-Capture Transition Test Based on Don't-Care Filling," *Proc. of Int'l Symp. on Circuits and Systems*, pp. 27-30, May 2007.
- [26] X. Wen, Y. Yamashita, S. Kajihara, L.-T. Wang, K. K. Saluja, and L. Kinoshita, "On Low-capture-power Test Generation for Scan Testing," *Proc. of VLSI Test Symp.*, 2005.
- [27] CIC Referenced Flow for Cell-based IC Design, Chip Implementation Center, CIC, Taiwan, Document no. CIC-DSD-RD-08-01, 2008.