Cross-coupling in 65nm Fully Integrated EDGE System On Chip

Design and Cross-coupling prevention of complex 65nm SoC

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***Abstract*— Entry mobile phone market is a mass volume segment where the modem and application technologies are commoditized and fully proven. Nevertheless the cost and power reduction target continues to heavily drive leading edge innovations. Semiconductor companies strive to integrate more and more Printed Circuit Board (PCB) components into one single chip, without discontinuing the technology node shrink roadmap, from 130nm down to 65nm. This duality between integration level and aggressive silicon feature size reduction generates an innovative environment where design engineers must create new methodologies to cope with complex cross coupling mechanisms and additional power dissipation. This paper describes one aspect of the design methodology to reduce the die and package cross-talks, and focus on the package co-design flow. The chip being considered is a 65nm single chip System on Chip (SoC) including EDGE RF, Power Management Unit (PMU), Audio Front End (AFE) and FM Radio (FMR) circuits.**

Keywords: eWLB; Chip&Package Co-Design; SoC integration, cross-coupling, aggressors, victims

I. DESIGN ENVIRONMENT

A. Shrink and Component Integration Roadmap

The mobile phone industry pursues the fight against price erosion on the low tier market segment. This low end segment is mainly driven by cost and power consumption optimization.

But the mobile phone market expects the chip manufacturer not only to drive the cost and power reduction road map, but also rely on the manufacturer to integrate the commoditized feature set, both in terms of processing/audio performances and connectivity enhancements. Features like advanced audio codec players (MP3, AAC, eAAC+), FM radio, Camera, USB and Memory card support migrate into the low end market segment. Moreover a key feature of the low end phones is to provide internet capability to the emerging market where most people have no fix-line internet connection.

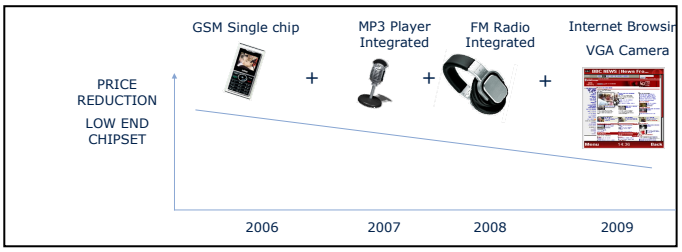

Figure 1. Single chip integration for PCB cost reduction

During the last decade, design activities were focusing on one of two directions:

- Either shrinking the technology nodes and keeping the integration level constant
- Or keeping the technology node constant and integrating into one single chip the next commoditized mobile phone features.

Moreover the 130nm and 90nm RF integration were achieved by integrating mature RF circuits, already widely distributed among many GSM systems. This was achieved with qualified package technology, and low clock speed. By moving one step forward at a time, it was possible to control the complexity of the cross-coupling by relying on already mature and high volume existing circuits. Cross-coupling and spur hunting were measured on silicon, and respectively addressed thru chip re-spins, selective package routing modifications or Printed Circuit Board modifications. The design complexity remains at the module level, the number of cross-coupling use cases among the different die modules being rather low. The main cross-coupling problem is generally between the RF and the processing part of the chip, thus silicon substrate, power lines, package and PCB routing.

Following the new market requirements to shrink, integrate and reduce power consumption as well as to increase the chipset performances, the complexity of the design activities of a low end phone chipset increases exponentially in 65nm.

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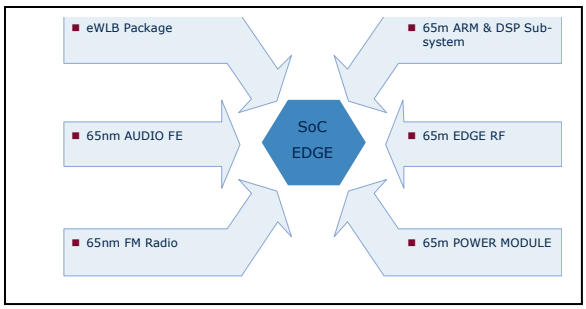

Figure 2. Increased complexity of 65nm SoC Integration

The design teams now must cope with 5 new challenges

- Both shrink the current system as well as integrate fully new analog circuits (RF, PMU, audio front end)
- Develop new circuits to reduce the power consumption and increase power efficiency. Those circuits are often noisy and could dramatically increase the noise coupling mechanism.
- Further integrate commoditized feature set (FM radio, Camera, Audio codec, …)
- Simulate and validate multiple cross-coupling scenarios thru silicon substrate, supply and ground network, package and PCB routing, with double digital frequency range
- With new package and sometimes new PCB technology

This result is more than 100 possible cross coupling scenarios with high probability of failure due to increased frequency range, increased number of noisy parts and immature intellectual properties (IP). New simulation models and methodology are required to prevent and control the coupling mechanism. The new methodologies would not only tackle the die cross–coupling, but will also address the mechanism thru the package and the PCB.

B. *65 Single Chip EDGE*

The focus will be the package co-design flow of a 65nm Single Chip. The chip being considered includes the 5 main components of a mobile phone PCB:

- the base band processors and DSP, along with the respective embedded ROM and RAM memories
- the RF transmitter/receiver
- the audio amplifiers, receivers and measurement unit
- the power and energy management circuits (incl. charger, LED and other accessory detection circuits)
- the FM radio circuit

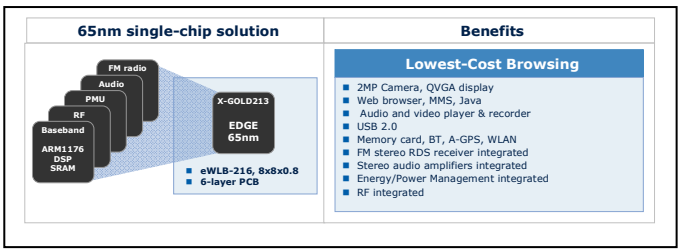

Figure 3. Description of circuit example

The device is designed on a standard 65nm Low Power CMOS. The package is an extended Wafer Level BGA (eWLB) 8x8mm. This new package technology brings the benefit to reduce the electrical parasitics, and to increase the power dissipation by reducing the thermal resistance. It also allows the designer to bring power right to the center of the die and thus increase the decoupling capacitance effect. The miniaturization of the package is also a pre-condition of the die shrink, as the number of IOs stays stable. eWLB design increases the I/O density on the die and avoid pad limitation designs. The design activities are nevertheless more complex, and require a more complex design flow.

C. *Cross-coupling Mechanisms*

The signal and power integrity must be checked at 3 levels:

- silicon substrate cross-talks
- Power and ground silicon integrity
- Package and PCB signal integrity

The number of aggressors and victims increases exponentially with the number of integrated components. Aggressors are the DSP and ARM sub-systems, but also new noisy circuits for power reduction like step down and step up converters, power amplifiers or charge pump for external audio accessories. Victims are audio circuits with high SNR requirements, FM radio and RF transmitter/receivers.

The graphics below describes the possible cross-coupling mechanisms between the analog/digital areas of the circuits, thru substrate, metal layers and package.

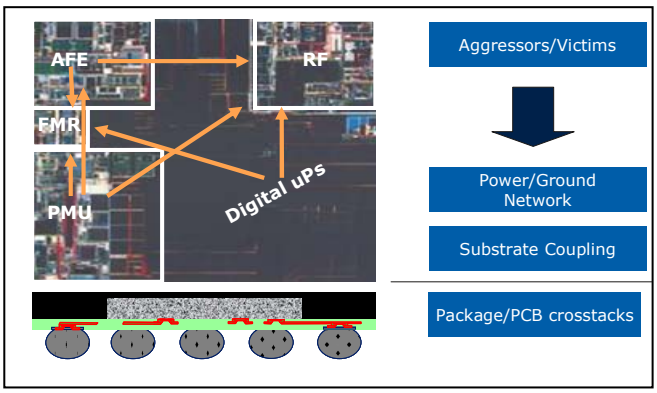

Figure 4. Cross-coupling in hihly integrated 65nm SoC

It is of high importance to clearly identify the possible cross-coupling mechanisms before designing the circuits, as the

resulting measures and methodology will depend on the possible aggressors/victims. Package design is one of the most critical parameter to consider and is at the center part of the co-design flow. Substrate coupling can be minimized with careful floor planning, and substrate contact topology, while power/ground integrity can be strengthen with embedded and external de-coupling capacitance. The package design must take into account all constraints from silicon substrate to power/ground and signal integrity and decoupling up to final PCB routing.

A simple package design approach is not possible as the floor plan, ball out, and cross talk simulation iterations are increasing exponentially with the number of aggressors/victims.

The co-design flow described in next paragraph allows the design team to collect all requirements in one data base and to run one design methodology between numerous experts and design teams, with as various expertise as digital, analog, RF or PCB design.

II. PACKAGE CO-DESIGN FLOW

A. Embedded Wafer Level BGA Package Concept

Each production technology of devices or systems follows the global tendency of cost savings together with an upgrade of the product properties in comparison to the predecessor version or technology. Miniaturization, thermal and electrical performance and the increase of functionality (e. g. embedded passives) are main drivers for the packaging technology beneath the reduction of packaging cost.

In the recent years a new packaging technology has come up, which is able to solve the requirements of future packages: The Wafer Level Ball Grid Array (WLB) is an attractive solution for low cost packaging with small form factor and high performance. In comparison to standard packaging technologies all process steps are performed on wafer level. This way, the interposer and the first level interconnect of classical packages melt into a thin-film redistribution layer applied on the wafer with high parallelism.

Fig. 5 shows the embedded Wafer level BGA package (eWLB) with additional fan-out area around the chip. We applied this basic packaging concept containing one thin film redistribution layer (RDL) for the described product design. The main advantages of eWLB packages are the high integration density (small size, even the height) and very good electrical performance.

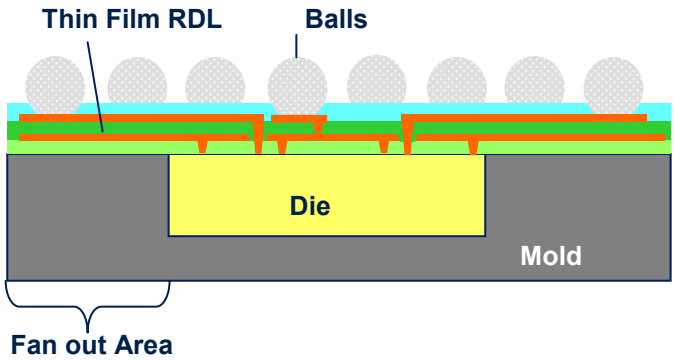

Figure 5. Embedded Wafer Level BGA Package (eWLB)

The thinned, diced and tested good silicon chip is the starting point for process flow of eWLB technology [1, 2]. We rearrange the dice face down on a carrier system and encapsulate them with a mold compound. The encapsulation process is the core process in eWLB technology. In the following step we use thin-film technology to realize redistribution layers on the obtained "molded reconfigured wafer". Thus, the package allows additional fan-out area around the chip. This overcomes the restrictions of standard wafer level packages of the limited I/Os count at a given pitch. Further, the obtained eWLB package has a height of 0.4 mm only. The thin-film technology offers the advantage of high precision and low temperature. In addition, it enables very flexible and highly customizable package designs. The eWLB technology enables the integration of several dice of different IC technologies and passive components. Thus, the packaging technology can be used for System-in-Package applications. From a manufacturing point of view, we require no additional process steps and thus additional costs to integrate passives in package. For single-chip applications, we obtain chip-scale-packages (CSP). The eWLB package technology shows very attractive RF characteristics [3, 4].

In comparison to other standard package types the redistribution layer of the package is located close to the chip metal routing. The small dielectric height between chip and package routing of about 6µm causes coupling. Main challenge in comparison to other standard packages these couplings can not be neglected during product design. For standard flip chip packages e.g. the distance between chip and package routing is in the order of about 50-100µm. In most cases the coupling between chip and package routing can be neglected for these applications. For wafer level packages the chip package coupling has to be considered during product design. The design method has to support respective coupling investigations. Main challenge here is to overcome the barrier between chip and package design environments which are completely different.

B. Basic Chip&Package Co-Design Flow

Due to significant interactions between WLB-RDL and Chip the design environment requires:

- Concurrent implementation of sensitive chip macros and WLB RDL (Co-Design)

- Common RF extraction/timing analysis of WLB RDL and chip

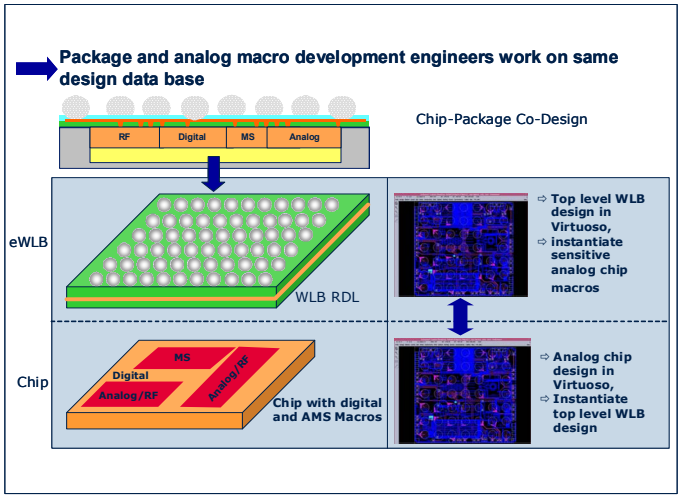

Figure 6. Physical implementation within Chip&Package Co-Design

Main critical parts from electrical point of view are the analogue parts of the chip. In order to support the concurrent editing of analogue chip and eWLB design, the physical layout implementation of both parts takes place in one design environment. We choose the Cadence Virtuoso tool for physical layout implementation. WLB design and each required analogue macro is designed in one Virtuoso design file. The designs are instantiated to each other (see figure 6). In the top level eWLB design file we instantiated the full-custom macros and the abstracts of semi-custom macros. In each of the critical full custom analog macro chip design files we instantiated the relevant eWLB structures. Therefore the chip designer had access to the WLB design in each design state and the WLB designer had access to the chip design continuously. Routing across critical chip areas was avoided due to the transparence of design situations on chip and WLB level. The chip designers were able to react on required changes in package design and in the other way around. Design modifications in both domains (chip and package) were done from one window and one person.

For example the very critical RF macro was designed in a way where the chip structures and the pertaining eWLB structures were designed from one chip design person. The part of the eWLB structures was linked to the top level eWLB layout file and finally integrated in the complete eWLB design.

The system connectivity was maintained in the very early state of the project within excel. Later the connectivity was imported in the design environment using the Cadence Composer (figure 7). Doing this the maintenance of the system connectivity follow up on modifications was handled in an efficient way. The system connectivity was direct visibility in layout. Additionally connectivity issues were easily recognized.

Design rule check (DRC) and connectivity check (LVS) for eWLB package are provided for Calibre and can be started similar to chip design procedure within design environment. The design rules of eWLB structures we checked from bump openings on chip side (vias) until the solder stop of eWLB. For the connectivity check two versions of LVS runset exist. One version is the LVS runset in WLB design package checking connectivity from solder stop to top-level metal. The Second LVS runset we used in chip design package for checking connectivity from top-level metal down to transistor level.

The link between digital chip design and eWLB design works with exchange of respective die pad coordinates. Additionally we streamed in the eWLB routing in the digital top level layout environment (Blast Fusion) for final review and final check.

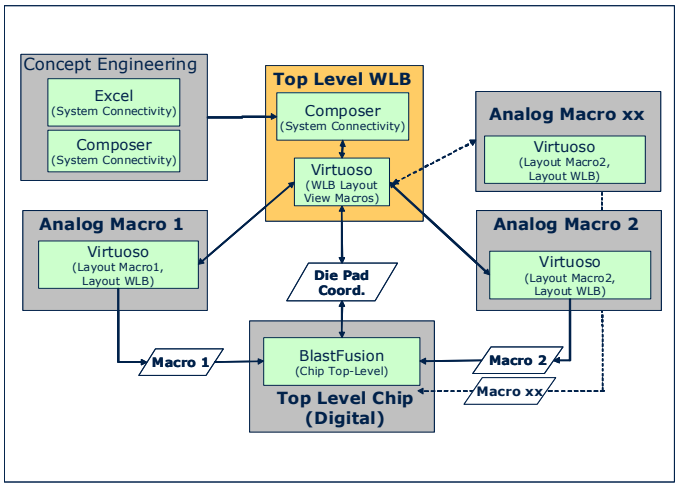

Figure 7. Chip&Package Co-Design Flow

C. *Electrical Simulation*

In order to allow RF and high speed relevant product design electrical simulations of critical parts are required. The parasitics of package and chip routing including the relevant coupling has to be considered in electrical simulations. Base for the circuit simulation of analogue parts and timing analysis of digital parts are the extracted parasitic elements (L, R, C) of the layout structures.

Standard chip simulation tools (extraction tools) typically not allow the extraction of parasitic inductances. For pure on chip routing structures the effects of parasitic resistances and capacitances dominates. Neglecting the parasitic inductances is possible here. However, for the package structures with longer lines and larger distances the parasitic inductances are much more important in order to describe the effects in the right way. Inductances have to be considered. The package parasitic extraction tool has to be capable to calculate the scattering parameter or the respective inductances, capacitances and resistances values.

We applied standard 3D full wave solvers like Ansoft HFSS for parasitic extraction. Having chip and package design data in one design environment (Candence Virtuoso) allows straight forward import of standardized gdsII data in extraction

tool (figure 8). For lower frequencies we applied the quasi static solver Ansoft Q3D for the parasitic extraction, which calculates the L/R/C Matrix for the entire structure.

The applied 3D finite element method (FEM) allows a very accurate calculation of the parasitics. We verified the simulation models of typical eWLB structures and embedded passives with measurements upfront [3, 4]. This verification work gave us a high level of confidence about simulation accuracy.

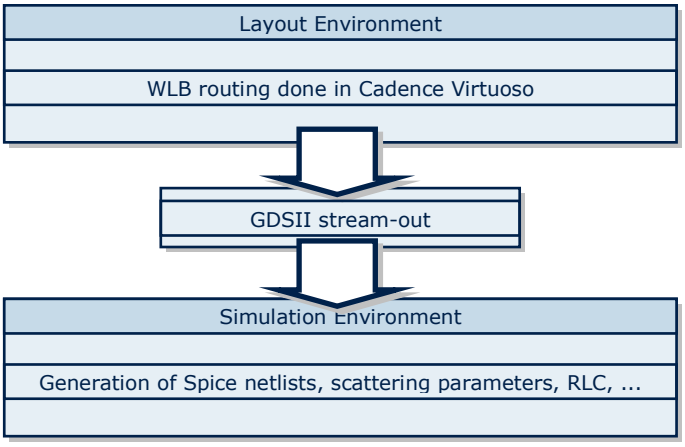

Figure 8. Simulation flow for package parasitic extraction

We extracted the complete WLB package and the entire routing. We considered the parasitics of the complete signal paths from the chip to eWLB interconnect (via) until the BGA balls. We used these results mainly for electrical simulation of parts with low coupling and for final verification of digital parts.

To calculate the influence of the coupling between chip and package we extracted the relevant WLB and chip routing structures together. Layout data export of chip and WLB structures into the simulation tool was working again on base of gdsII data. Due to the availability of the layout data in one tool environment the data transfer to the simulation tool worked straight forward.

Dependent on the requirements selected WLB and PCB structures where calculated considering the interaction as well (figure 9). PCB design was performed in typical PCB design tool. PCB and WLB routing structures were exported separately form the respective design tool and combined in the simulation tool. Than we calculated the parasitics of the PCB and WLB structures and generated the respective spice model. The model was considered in the circuit simulation. The model for PCB and WLB was required for design optimization of the RF critical parts within the RF macro.

Results of parasitic extractions are typically the scattering parameters (S-parameter). Most circuit simulations require spice models. These spice models we generated on base of the S-Parameter using broadband spice. Additionally L/R/C Models can be delivered. L/R/C-Models we mainly used for digital analysis.

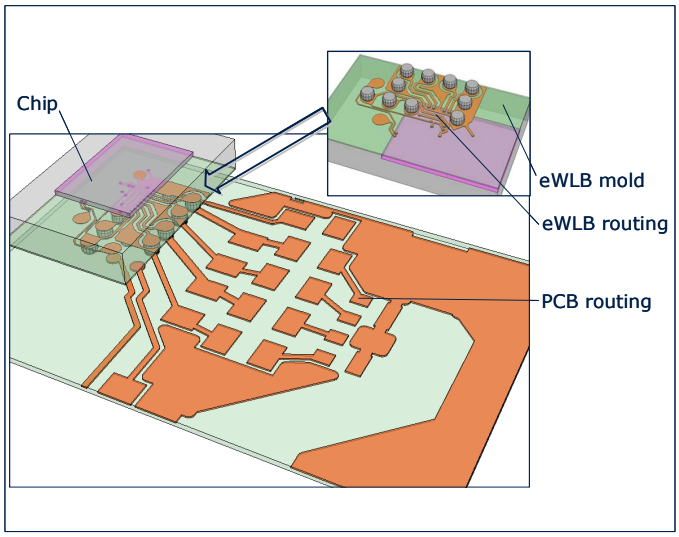

Figure 9. Parasitic extraction of eWLB and PCB structures

Finally we performed circuit simulations of analogue active structures including the package parasitic models. The simulation results gave information about the influence of package parasitics on overall performance of the device. Coupling between different signal routing structures in eWLB package and on chip were considered. We considered non ideal ground structures including the respective coupling as well. On base of the simulation results we optimized the desin structures on chip and in the eWLB package. An investigation about the optimized placement of embedded inductor component was possible as well applying the same procedure. Case studies to compare the overall functionality of the circuit applying on chip embedded inductor or in eWLB package integrated inductor where possible.

D. Result for SoC in eWLB package

Following the described chip&package co-design flow the design of chip and eWLB package was performed in an efficient way. Figure 10 shows a layout of eWLB packaging the chip with analog RF functionality. Electrical simulations considering parasitic effects of chip routing, eWLB routing, PCB routing and the relevant coupling were performed. The simulation method enabled us to consider the entire eWLB package structures from chip pad openings until the BGA balls. Parasitic inductances, capacitances and resistances were calculated. On base of the analysis results we optimized the design.

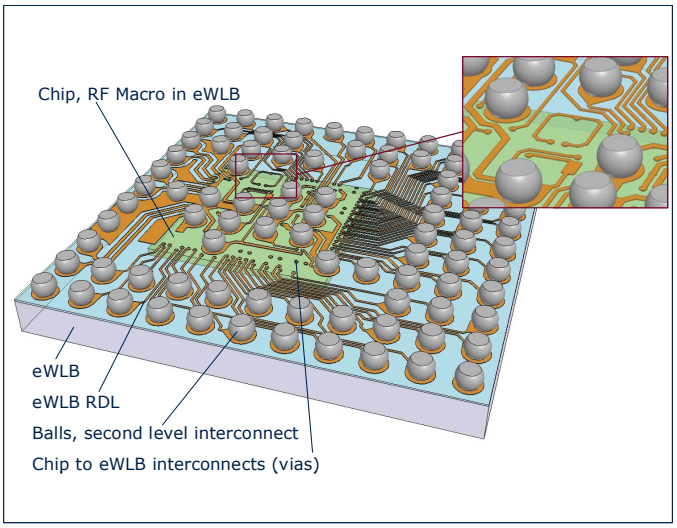

Figure 10. SoC in eWLB package, layout view

III. SUMMARY

With improved electrical and thermal performances, the eWLB package technology is one of the key success factors to reach such level of integration and the required GSM RF performances. By also setting different cross coupling constraints, it was necessary to develop a new tooling flow, for both design optimization and parasitics extraction. This flow environment allowed the design team to master the coupling mechanisms at the package level, enabling a complete benefit of the new eWLB package technology. Along with die cross coupling analysis, it was possible to achieve the first EDGE SoC, integrating baseband, audio frontend, power and energy management, RF, and FM radio in 65nm CMOS technology.

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