An Overview of Non-Volatile Memory Technology and the Implication for Tools and Architectures

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Abstract— **Novel nonvolatile memory technologies are gaining significant attentions from semiconductor industry in the competition of universal memory development. We used Spin-Transfer Torque Random Access Memory (STT-RAM) and Resistive Random Access Memory (R-RAM) as examples to discuss the implication of emerging nonvolatile memory for tools and architectures. Three aspects, including device and memory cell modeling, device/circuit co-design consideration and novel memory architecture, are discussed in details. The goal of these discussions is to design a high-density, low-power, high-performance nonvolatile memory with simple architecture and minimized circuit design complexity.**

Keywords - Universal memory; STT-RAM; R-RAM; MTJ device modleing; memory yield improvement.

I. INTRODUCTION

As the traditional memory technologies, e.g., DRAM, SRAM, and Flash, are approaching the end of their lives, a new concept called "Universal Memory" rises above the horizon. The expected characteristics of a universal memory include high-density (low-cost), high-speed (for both read and write operations), low-power (both access and standby powers), random-accessibility, non-volatility and unlimited endurance. These characteristics allow universal memory to meet the requirements of various applications: from a large, expensive supercomputer to a low-cost, ubiquitous, consumer handheld device. Some promising candidates of universal memory are phase change memory [1], magnetic memory (including both toggle-mode magnetic memory [2] and spin-transfer torque memory [3]), and resistive memory. In this paper, we will mainly focus on the latter two memory technologies: spin-transfer torque random access memory (STT-RAM) and resistive random access memory (R-RAM).

The basic component of magnetic random access memory (MRAM) is magnetic tunneling junction (MTJ). Data storage is realized by switching the resistance of MTJ between high- and low-resistance states. MRAM features non-volatility, fast writing/reading speed (<10ns), almost unlimited programming endurance (>10^{15} cycles) and zero standby power [2].

In conventional MRAM design (known as "toggle-mode"), MTJ resistance is changed by using the current induced magnetic field to switch the magnetization of MTJ. When the size of MTJ scales, the amplitude of the required magnetic field is increased correspondingly. The high write power consumption severely limits the scaling of conventional MRAM. Recently, a new write mechanism based on spin polarization current induced magnetization switching, is introduced to MRAM design. This new MRAM design, called spin-transfer torque random access memory (STT-RAM), is believed to have a better scalability than conventional MRAM. Various designs of STT-RAM were proposed by both industry and academia in the past several years [3].

Resistive random access memory (R-RAM) can generally denote all memory technologies that rely on the resistance change to store the information. Many R-RAM technologies with various storage mechanisms have been extensively studied, including (but not limited to) space-charge-limited-current (SCLC), filament, programmable-metallization-cell (PMC), Schottky contact and traps (SCT), etc. R-RAM not only has all the characteristics of MRAM including non-volatility, high speed, high endurance and zero standby power, but also can achieve high density.

In this work, we use STT-RAM and R-RAM as the examples to discuss the implication of emerging nonvolatile memory for circuit design tools and memory architectures. The rest of our paper is organized as follows: Section II provides the preliminaries of STT-RAM and R-RAM; Section III illustrates the desired cell modeling in emerging nonvolatile memory design, by using STT-RAM as an example; Section IV demonstrates some device/circuit co-design principle for high-density, high-performance memory; Section V discusses some novel architectures for yield enhancement and performance/ cost tradeoff.

II. PRELIMINARIES OF STT-RAM AND R-RAM

A. Preliminary of STT-RAM

MTJ – the data storage element of STT-RAM – includes two ferromagnetic layers and one oxide barrier layer, e.g., MgO. MTJ resistance is determined by the relative magnetization directions of the two ferromagnetic layers: when the magnetization directions are anti-parallel (parallel), MTJ is in high- (low-) resistance state, as shown in Fig. 1. In STT-RAM, the magnetization direction of one ferromagnetic layer (called "reference layer") is fixed by coupling to a pinned magnetization layer; the magnetization direction of the other

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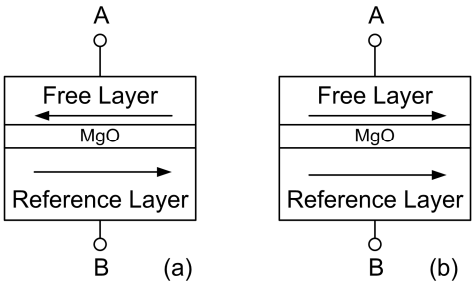

Figure 1. MTJ structure. (a) Anti-parallel (high resistance) (b) Parallel (low resistance)

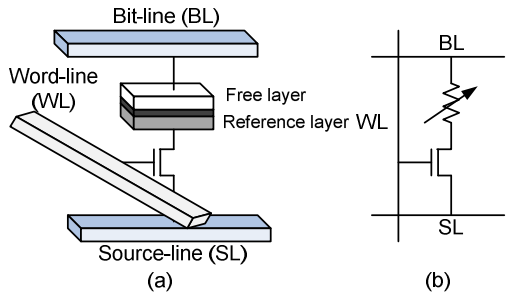

Figure 2. 1T1J strucutre. (a) Device view (b) Equivalent schematic.

ferromagnetic layer (called "free layer") is changed by passing a driving current polarized by reference layer [3]: When applying a positive voltage on point B in Fig. 1, the magnetization direction of free layer rotates to the opposite direction of reference layer. MTJ resistance switches from low to high. When applying a positive voltage on point A, the magnetization direction of free layer rotates to the same direction of reference layer. MTJ resistance switches from high to low.

Because of its simplicity, one-transistor-one-MTJ (or 1T1J) structure [3], where one MTJ is connected to one NMOS transistor in series, becomes the most popular design of STT-RAM. As shown in Fig. 2(a), we usually call interconnects connected to MTJ, to the source/drain and to the gate of NMOS transistor as bit-line (BL), source-line (SL) and word-line (WL), respectively. MTJ is modeled as a variable resistor in the equivalent circuit schematic, as shown in Fig. 2(b). The direction of the switching current of MTJ is polarized by the different biasing on BL and SL.

B. Basics of R-RAM

Although R-RAM technology involves many different storage mechanisms, there are only two "conventional" operation types in R-RAM design: unipolar switching and bipolar switching. Within this context, unipolar operation executes the programming/erasing by using short and long pulse, or by using high and low voltage with the same voltage polarity. In contrast, bipolar operation is achieved by short pulses with opposite voltage polarity.

One typical unipolar switching example appears in filament-based R-RAM device [4]. A filament or conducting path is formed in an insulating dielectric after applying a sufficiently high voltage. Once the filament is formed, it may be set (leading to a low resistance) or reset (leading to a high resistance), by appropriate voltages.

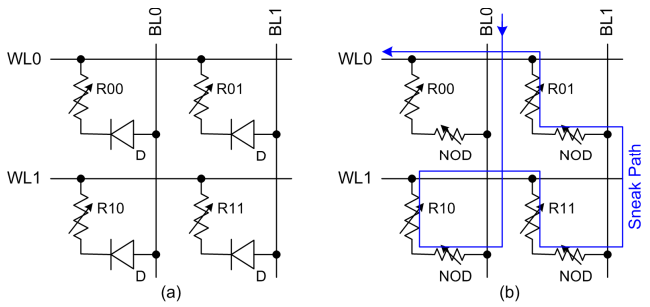

Figure 3. R-RAM memory array. (a) 1D1R structure (b) use NOD as selection device.

One typical bipolar switching example is PMC device, which is composed of two solid metal electrodes – one relatively inert the other electrochemically active. A thin electrolyte film is allocated between two electrodes. When a negative bias is applied to the inert electrode, metal ions in the electrolyte and some originating from the positive active electrode flow into the electrolyte and are reduced by the inert electrode. Finally, the ions form a small metallic "nanowire" between the two electrodes. As a result, the resistance between two electrodes is dramatically reduced. When erasing the cell, a positive bias is applied on the inert electrode. Metal ions will migrate back into the electrolyte, and eventually to the negatively-charged active electrode. The nanowire is broken and the resistance increases again [5].

For unipolar R-RAM memory, a diode in series with data storage cell structure can be used as selection device (1D1R) as shown in Fig. 3(a). The selection device in bipolar R-RAM memory can be NMOS transistor or non-ohmic device (NOD) as shown in Fig. 3(b). Memory cell with NOD can achieve high array density. However, it results in sneak path which has three or more cells in series. In such design, the voltage across the selected cell must be much higher than the one across the other cells in the sneak path to guarantee proper functionality.

III. Device and Cell Modeling

The emerging nonvolatile memory cell normally includes the data storage device(s) and the select device(s), e.g., a NMOS transistor or a diode. Although many studies have been conducted on the theoretical modeling of data storage devices, few of them focus on the interaction between the dynamics of the data storage device and the select device. In this section, we use a 1T1J STT-RAM model to illustrate the importance of a memory cell model that can simulate the coupling between data storage device and select device in emerging nonvolatile memory design.

A. Coupling Between MTJ and NMOS Transistor

In normal operation region (write pulse width > 10ns), the required magnitude of switching current of MTJ can be calculated as [3]:

$$I_C = I_{C0}\left\{1-\left(\frac{kT}{E}\right)\ln\left(\frac{\tau}{\tau_0}\right)\right\}. \quad (1)$$

where τ is write pulse width; I_C is the critical switching current, which is the minimal required current magnitude to switch the MTJ resistance by τ; I_{C0} is the critical switching current at 0K; E is the magnetization stability energy barrier; τ_0 is the inverse of the attempt frequency, or the write pulse width at 0K; k is Boltzmann constant; T is operation temperature. Reducing the write current applied to MTJ I_C leads to longer write pulse width τ. We use R_H and R_L to denote the high or low MTJ resistance, respectively. Then the tunneling magneto resistance ratio (TMR) can be defined as $(R_H\text{-}R_L)/R_L$.

We note that the driving strength of NMOS transistor is affected by the IR drop across MTJ. When driving current from BL to SL, V_{DD} is applied to BL and WL. SL is connected to ground. The biasing conditions of NMOS transistor is:

$$V_{GS} = V_{DD}, V_{DS} = V_{DD} - IR . \quad (2)$$

here, I is the current through MTJ; R is the MTJ resistance; V_{GS} is the potential difference between the oxide gate (G) and the source (S) of NMOS transistor; V_{DS} is the potential difference between the drain (D) and the source (S) of NMOS transistor.

When driving current from SL to BL, V_{DD} is applied to SL and WL. BL is connected to ground. We have:

$$V_{GS} = V_{DD} - IR, V_{DS} = V_{DD} - IR . \quad (3)$$

Eq. (2) and (3) show that when the size of NMOS transistor is fixed, the change of MTJ resistance (R) results in different biasing conditions of NMOS transistor and consequently, different current through MTJ (I).

In the conventional static STT-RAM cell model, the dynamics of MTJ is decoupled with the transience of NMOS transistor [6]: After applying write current with a pre-characterized write pulse width, the resistance of MTJ switches from R_L (or R_H) to R_H (or R_L) abruptly. However, in the write operation of STT-RAM, the resistance of MTJ continuously changes with some fluctuations that are generated by magnetic damping [7]. To avoid overestimating the driving strength of NMOS transistor, R_H is always assumed in the calculation of the current through MTJ. This assumption, however, always leads to pessimistically long write pulse width (when NMOS transistor size is fixed) or unnecessarily large NMOS transistor size (when write pulse width is fixed).

B. Dynamic Model of STT-RAM Cell

The traditional spin-transfer torque model of MTJ in [8][9] can be easily extended to consume the timing varying electrical inputs like driving current. For example, the dynamics of MTJ free layer magnetization can be calculated by Landau-Lifshiltz-Gilbert (LLG) equation with spin polarized torque term:

$$\frac{d\vec{m}}{dt} = \alpha\vec{m}\times(\vec{m}\times\vec{h}_{\text{eff}}) - \vec{m}\times(\vec{h}_{\text{eff}} + \beta\vec{m}\times\vec{p}) . \quad (4)$$

where $\vec{m}$ is the normalized magnetization; $\vec{h}_{\text{eff}} = \vec{H}_{\text{eff}} / M_s$ is the normalized magnetic field (by shape and anisotropy etc.); α is the damping parameter; $\beta = (\eta, M_s, d, S, I)$ is the normalized spin torque polarization magnitude, which is a function of spin polarization efficiency β, magnetic film saturation M_s, thickness d, surface S and the current through MTJ I [8][9]; $\vec{p}$ is an unit vector pointing to spin polarization direction. In the procedure that MTJ resistance changes, the magnitude of current I is a time-varying quantity that is determined by the biasing conditions and the parasitic of NMOS transistor, as well as the MTJ resistance.

Fig. 4 shows the simplified schematic to model the dynamic behavior of STT-RAM cell: MTJ is represented by a variable resistor; NMOS transistor is modeled as a voltage (V_{GS}, V_{DS} and V_{SB}) controlled current source (VCCS) I_T, which can be pre-characterized by SPICE simulation, and a set of parasitic capacitors. Here C_{GD}, C_{GS}, C_{DB}, C_{SB} and C_{GB} denote the capacitances between gate and drain, gate and source, drain and body, source and body, gate and body, respectively. Usually C_{GB} can be ignored [10].

The dynamic electrical behavior of 1T1J STT-RAM cell can be expressed by:

$$\begin{aligned} &I_M + I_{GD} = I_{DB} + I_T \\ &I_{GD} = C_{GD}\cdot\left(-\frac{dV}{dt}\right) \\ &I_{DB} = C_{DB}\cdot\left(\frac{dV}{dt}\right) \\ &I_M \cdot R(t) = V_{DD} - V \quad (\text{current from BL to SL}) \text{ or} \\ &I_M \cdot R(t) = -V \quad (\text{current from SL to BL}) \end{aligned} . \quad (5)$$

Here, I_M, I_{GD}, I_{DB} and I_T are the currents through MTJ, C_{GD}, C_{DB} and NMOS transistor, respectively. V is the voltage at the point between MTJ and NMOS transistor. $R(t)$ is the timing-varying MTJ resistance.

By combining Eq. (4) and Eq. (5), a dynamic STT-RAM cell model that can take into account both the magnetic response of MTJ and the electrical response of NMOS transistor is achieved.

Compared to the conventional static STT-RAM cell model, the above dynamic STT-RAM cell model is much closer to the realistic physical mechanism of STT-RAM write operation.

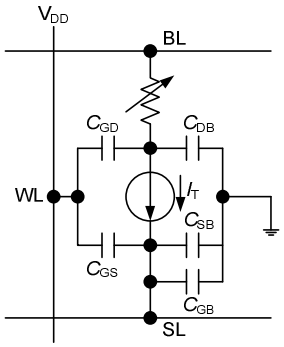

Figure 4. Dynamic model of STT-RAM cell.

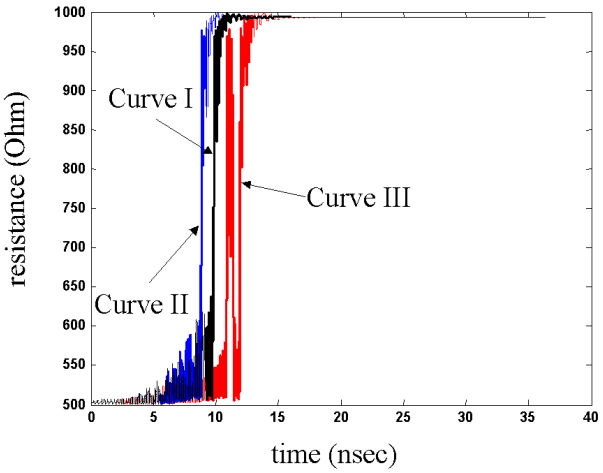

Figure 5. Dynamic response of MTJ resistance

C. *Benefit of Dynmaic STT-RAM Cell Model*

By using the dynamic STT-RAM cell model, we simulated the dynamic response of MTJ resistance when it switches from R_L to R_H at TSMC 90nm Technology. The result is shown as the curve I in Fig. 5. NMOS transistor provides a driving current of 300μA and 264μA when MTJ is in the steady low- or high-resistance state, respectively. We refer to this result as scenario-I. For comparisons, the following two scenarios are also simulated:

Scenario-II (optimistic case): The MTJ is assumed to be driven by a constant current of 300μA. This scenario overestimates the average current applied to MTJ and results in an optimistic result of the switching time of MTJ.

Scenario-III (pessimistic case): The MTJ is assumed to be driven by a constant current of 264μA. This scenario is actually the assumption of conventional static STT-RAM cell model. It underestimates the average current applied to MTJ and results in a pessimistic value of the switching time of MTJ.

Scenario-II and Scenario-III are also shown in Fig. 5 as the curve II and III, respectively. The corresponding switching times of MTJ in Scenario-I, -II and –III are 10ns, 9.17ns, and 12.05ns, respectively. Results clearly show that Scenario-III (pessimistically) overestimated the switching time of MTJ by 20.5%, compared to Scenario-I. In STT-RAM design, we normally have a certain performance requirement, i.e., a fixed write pulse width. Scenario-III always leads to a pessimistic (larger) estimation of NMOS transistor size.

Also, Scenario-II (optimistically) underestimated the switching time of MTJ by 8.3%, compared to Scenario-I. This result proved that R_L can never be used in conventional static MTJ model to simulate the performance of the write operation of STT-RAM.

The main disadvantage of the above dynamic STT-RAM cell model is the incompatibility to SPICE tool: The magnetic model solver cannot be embedded into SPICE tool. One possible solution is to propose a SPICE macromodel or Verilog-A model to emulate the dynamics of data storage device.

IV. DEVICE/CIRCUIT CO-DESIGN

To achieve high density memory array, the data storage device and the select device must be small enough. Without loss of generality, the cell area of STT-RAM or R-RAM is mainly determined by:

- The required switching current of data storage device. The smaller switching current is, the smaller select device is required;
- The driving strength of select device. For the same switching current of data storage device, the higher driving strength of select device per unit area is, the smaller area of select device can be achieved;
- The interconnect and terminal configurations of memory cell. When the size of select device is small enough, the memory cell area of R-RAM is determined by the layout rule under certain cell structure.

A. *Magnetic Solution for STT-RAM Scaling*

The possible smallest areas of 1T1J STT-RAM cell at different technology nodes are shown in TABLE I as columns "Norm.". We use row "90" in TABLE I as our STT-RAM cell scaling baseline, which has been calibrated with the experimental measurement [11] under TSMC 90nm technology. PTM model is used in the simulation of 45nm and 22nm results [12]. The switching time of MTJ resistance is fixed at 10ns in all cases. I_{drv} is the maximum driving current that NMOS transistor needs to provide when driving current from SL to BL. Please note that memory cell area is measured by F^2, where F is the half pitch of the bit-line at a certain technology node. The corresponding MTJ parameters are shown in TABLE II. The TMRs of MTJ at all cases are assumed as 100%. The thermal stability parameter of MTJ is characterized as $K_{eff}V_{eff}/k_BT$, which are shown in column "KV/kT" in TABLE II. Here K_{eff} is the effective anisotropy due to the magnetic device shape and the intrinsic crystal anisotropy; V_{eff} is the effective volume considering non-uniform magnetization reversal; k_BT is the thermal excitation energy.

Without any circuit design or magnetic optimization, the

TABLE I. PARAMETERS OF STT-RAM CELL

Tech (nm)	V_{DD} (V)	Channel Width (nm)		Area (F^2)		I_{drv} (μA)
		Norm.	Over.	Norm.	Over.	
90	1.2	456	326	20.6	15.8	300
45	1.0	273	172	21.2	14.5	170
22^0	1.0	106	73	17.4	12.9	100
22^1	1.0	75	51	13.2	10.0	75
22^2	1.0	45	35	9.1	9.0	54

TABLE II. MTJ PARAMETERS

Tech. (nm)	MTJ Geometry (nm)			R_L (Ω)	RA_L (Ω·μm^2)	KV/kT
	Length	Width	Thickness			
90	110	60	2.2	600	4.5	52
45	90	40	2.3	1000	3.6	52
22^0, 22^1	45	22	3.2	1500	1.5	50
22^2	22	22	2.0	1500	1.5	50

minimal STT-RAM cell area of 1T1J structure is $17.4F^2$ at 22nm technology node, as shown in row "22^0". The factor limiting the cell area is the large switching current of MTJ.

One magnetic solution to reduce the MTJ switching current is adding perpendicular anisotropy at out-of-plane y direction [13]. After applying this solution, the STT-RAM cell area at 22nm technology node can be further reduced to $13.2F^2$, as shown in rows "22^1" in both TABLE I and II. The thermal stability of MTJ is not affected.

However, to maintain the required thermal stability, certain physical dimensions of MTJ must be kept, i.e., 2:1 ratio at x and y directions. Such geometry determines the minimal contact shape of MTJ and consequently, limits the cell area to be larger than $12F^2$. Another magnetic solution, which introduces surface anti-ferromagnetic coupled (AFC) magnetic layer with relatively low Curie temperature [14], can further reduce MTJ shape to a circle with 1F diameter. In such a situation, the theoretically minimal area of 1T1J STT-RAM cell can be achieved is $9F^2$. Our simulation result shows a $9.1F^2$ STT-RAM cell area at 22nm technology node, as shown in row "22^2".

B. STT-RAM Cell with Overdriving Scheme

Based on the analysis in Section III-A, overdriving the gate voltage of NMOS transistor can increase V_{GS} and consequently, enhance the driving strength of NMOS transistor: when driving current from BL to SL, V_{DD} is applied to WL and BL while SL is connected to ground; when driving current from BL to SL, V_{DD} is applied to SL and BL is connected to ground. An overdriving voltage $V_{DD} + \Delta V$ is applied to WL. Here $\Delta V = IR_L$, which is the voltage drop across the MTJ.

In the overdriving scheme of MTJ, because V_{DS} keeps the same as that in the normal operation scheme, the hot carrier effect is unaffected. The increased potential difference between the gate and the body of NMOS transistor may incur potential reliability issues, i.e., oxide time-dependent dielectric degradation (TDDB).

The parameters of STT-RAM when overdriving scheme applied are shown in column "Over." in TABLE I. STT-RAM cell area is significantly reduced by the enhanced driving strength of NMOS transistor. However, to achieve $9F^2$ cell area, the 2nd magnetic solution (row"22^2") is still needed to ensure that the shape of MTJ is a circle. In such a case, the required minimal channel width of NMOS transistor is actually smaller than 2F. The STT-RAM cell area (of $9F^2$) is limited by the layout design rule. Similarly, the STT-RAM cell area of "22^1" is $12F^2$, even though the required minimal channel width of NMOS transistor is only 51nm.

The limitation of overdriving scheme is that writing "0" (driving current from SL to BL) and writing "1" (driving current from BL to SL) require different word-line voltages. Therefore, values "0" and "1" cannot be simultaneously written into the bits that sharing the same word-line. Some possible solutions can be: 1) Two-step writing: writing "0" and "1" are completed at different steps for the bits that share the same word-line; 2) Erase/program scheme: all bits in the memory block are pre-written (erased) to "0" (or "1") first. In the write operation, only value "1" (or "0") is written (programmed) into the bits selectively.

We note that diode usually has much higher driving strength than MOS transistor for the same area. However, diode can only provide one-directional current and is mainly used to drive the unipolar device, e.g., some types of R-RAM cells. Diode-based driven scheme can reach a cell area of $4F^2$ by suffering from large driving strength variation normally.

V. STT-RAM/R-RAM YIELD ENHANCEMENT FACTORS

The memory technologies that use device resistance as the data storage media, e.g., STT-RAM and R-RAM, usually uses the read-out scheme shown in Fig. 6: Applying a read voltage (current) to the selected memory cell; the generated current (voltage) on the bit line is compared to a reference signal in sense amplifier. If the generated current (voltage) is higher than the reference, the data storage device in the memory cell is in the low- (high-) resistance state.

The reference signal is normally generated by applying the same read voltage (current) on the dummy cell, whose resistance is $(R_L+R_H)/2$ ideally. Similar to any other memory manufactured in the scaled technologies, emerging nonvolatile memories also suffer from the large process variation.

Process variation incurs the resistance distribution of data storage device in memory cell as well as the dummy cell. Fig. 7 shows STT-RAM read failure due to MTJ resistance variation: MTJ resistance variation among different memory cells results in BL voltage variation (V_H or V_L if MTJ is in high- or low-resistance state) when the same amount of read current applied. Moreover, the resistance variation of dummy cell, which is normally constructed by data storage devices, also introduces the reference voltage (V_{REF}) variation. If there is the generated

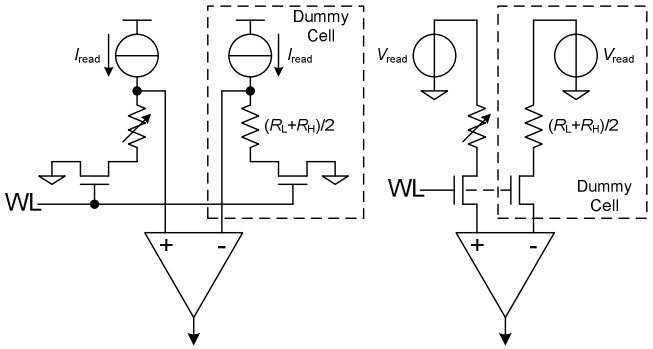

Figure 6. Read-out scheme of STT-RAM and R-RAM.

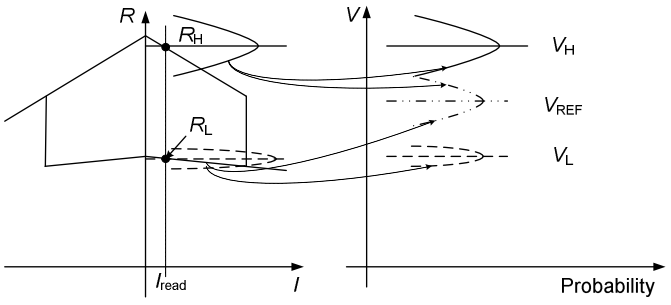

Figure 7. MTJ resistance distribution incurred read failure.

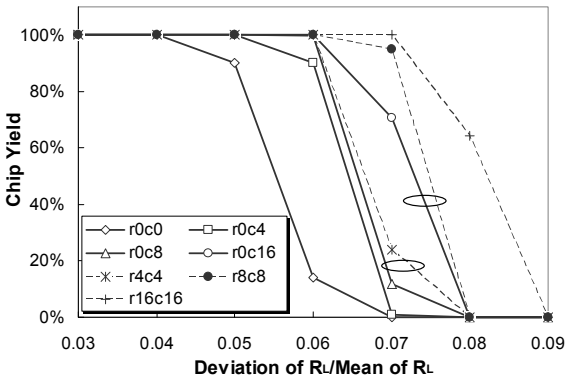

Figure 8. Chip yield under different reducndancy scheme.

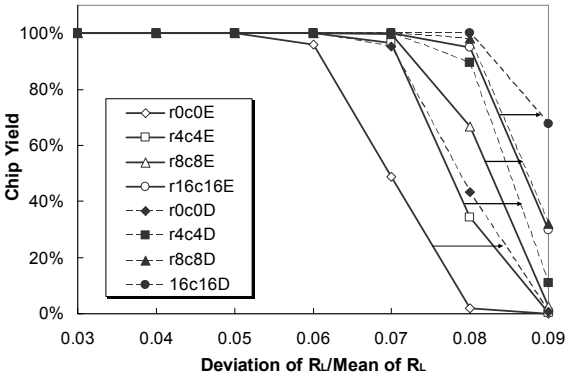

Figure 9. Chip yield under ECC and duplicate dummy columns.

V_H (V_L) is lower (higher) than V_{REF}, the data stored in memory cell is read wrongly. We call it as "read failure". Beside the manufacture defects, read failure significantly affects the yield of nonvolatile memory.

The read failures can be fixed by dummy column/row and ECC technologies etc. To evaluate the effectiveness of dummy and ECC technologies, we modeled a 16Kbit (128X128) STT-RAM. We assume the means of R_L and R_H are 1000Ω and 2000Ω, respectively. The deviation of R_H is assumed two times of the one of R_L. The simulated yield of the chip with various dummy schemes when the deviation of R_L is 0.03 to 0.09 of the mean of R_L are shown in Fig. 8 and 9. Here "rxcy" means there are x redundant rows and y redundant columns in chip design.

Based on results of r0c16 vs. r8c8, which are have the almost same redundant cells, simultaneous row and column redundancy has better chip yield than that of row or column redundancy only. Similar observation is made when comparing the results of r0c8 vs. r4c4.

We also implement a (12, 4) hamming code ECC for chip yield enhancement. Fig. 9 shows the results as rxcyE. Comparing to the results in Fig. 8 with the same redundant configuration, ECC can significantly improve the chip yield.

The resistance variation in the dummy column constrains the chip yield. To solve this problem, a duplicate dummy column scheme is proposed: Instead of using one dummy column to generate the reference signal, another duplicate dummy column is added. In the product qualification process, the dummy column that results in lower read failure rate is routed to the sense amplifier. In our design, we divided the dummy column into segments that have 8 bits each. For each 8 rows, the dummy segment that incurs lower read failure rate is selectively connected to the sense amplifier by a multiplexer. The simulation results are also shown in Fig. 9 as "rxcyD". A significant chip yield is observed.

VI. CONCLUSION

In this paper, we used STT-RAM and R-RAM as examples to illustrate the implication of resistance-based nonvolatile memory for device modeling, design consideration and the architecture. Dynamic memory cell modeling for new physical mechanism, a close circuit/device co-optimization and novel memory architecture for chip yield are highly desired by emerging nonvolatile memory design.

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