A **NoC at the Age of Six: Advanced Topics, Current Challenges and Trends**

Organiser: Axel Jantsch, Royal Institute of Technology, SE

Speakers: Axel Jantsch, Royal Institute of Technology, SE
Luca Benini, DEIS – Bologna U, IT
Timothy M Pinkston, National Science Foundation and USC, US
Kees Goossens, NXP Semiconductors, NL
Pieter van der Wolf, NXP Semiconductors, NL
Alain Fanet, Arteris, FR
Marcello Coppola, STMicroelectronics, FR

The tutorial briefly reviews the current state of the art in NoC research and what has been accomplished during the last six years. The main challenges for research and industrial applications are elaborated.
-Memory organisation: The pressing need to integrate the communication architecture with the memory architecture is analysed in the context of multimedia applications.
-Design for performance: The tutorial presents a throughput-driven NoC design and evaluation approach that enables the designer to reason about various network design trade-offs.
-Quality of Service: For many applications not only average but also worst case performance matters. Concepts and techniques for providing guaranteed bandwidth and latency.
-Middleware: The software environment, middleware services and abstractions, required to efficiently support NoC-based platforms will be discussed in detail.

Finally, two industrial NoC based platforms, Arteris and Spidergon, are discussed and analysed.
The tutorial targets researchers, engineers and teachers that want to gain a thorough understanding of the current state of the art of NoC research, of the main challenges and the near future possibilities for industrial exploitation of this technology.

B **Reconfigurable Computing: Architectures, Tools and Applications**

Organisers: Juergen Becker and Michael Huebner, Karlsruhe U, DE

Speakers: Juergen Becker, Karlsruhe U, DE
Michael Huebner, Karlsruhe U, DE
Andreas Herkersdord, TU Munich, DE
Walter Stechele, TU Munich, DE
Adam Donlin, Xilinx, US

Recent methods and reconfigurable architectures provide an increased design space by exploiting the dynamic and partial reconfiguration of hardware. The multi-adaptivity of this heterogeneous reconfigurable architectures reaches from adaptation to performance, to power consumption in relation of energy budgets, and to real-time adaptation for on-demand user requirements. The tutorial presents major issues in multi-adaptive system design:
- Hardware and techniques providing multi adaptivity during operation.
- Abstraction levels for operating dynamically reconfigurable architectures, incl. system level tool support.
- Efficient application exploitation of provided architectures and methods.

A detailed knowledge about the development of reconfigurable embedded systems will be provided by presenting a bottom-up approach from architecture and basic mechanisms up to high-level tools for system integration incl. application exploitation. The tutorial is addressed to hardware and system engineers as well as to researchers.

C **DFM Challenges and Practical Solutions in 65nm and 45nm**

Organiser: Andrew B Kahng, UC San Diego, US
Speakers: N S Nagaraj, Texas Instruments, US
Jean-Pierre Schoellkopf, STMicroelectronics, FR
Mike Smayling, Applied Materials, US
Ban P Wong, Chartered Semiconductor, US
Andrew B Kahng, UC San Diego, US

In the 65nm and 45nm nodes, DFM tools and methodologies must solve growing challenges of systematic and random manufacturing variations, leakage power, reliability, and random defectivity - while remaining consistent with productivity and flow requirements. This tutorial will first discuss interactions between layout and manufacturability for devices and interconnects, including circuit impacts of both intrinsic and transient variability. Special circuits (analogue, SRAM), layout techniques (layout regularity, restricted design rules, new router capabilities, high-yielding cell libraries), modelling (stress and strain engineering), and IP development techniques (integration in arbitrary SoC density contexts) will be discussed.

Toward the system level, the tutorial will discuss how on-die and on-wafer test and calibration structures can accelerate yield learning and adaptivity, as well as the process abstractions used by design optimisations. Also treated will be the topic of IP qualification, portability and integratability in the face of fab-specific manufacturing challenges. Finally, the tutorial will review current and emerging DFM tools and methodologies (e.g., "yield score" metrics, parametric yield optimisations, and design for reliability), along with concrete opportunities for high-ROI DFM deployment.

The tutorial is targeted to IC and SOC designers and product engineers, IP core providers and integrators, R&D engineers in EDA and mask/equipment supplier industries, foundry interface engineers, and managers who are trying to solve parametric and defect yield challenges, and who would like to learn how DFM techniques can help.

D **Simulink for Design and Programming Multiprocessor SoC**

Organiser: Ahmed Jerraya, TIMA Laboratory, FR
Speakers: Wayne Wolf, Princeton U, US
Pieter Mosterman, The MathWorks, US
Janos Sztipanovits, Vanderbilt U, US
Edward Power, SELEX Sensors and Airborne Systems, UK
Tom Pitchforth, SELEX Sensors and Airborne Systems, UK
Ahmed Jerraya, TIMA Laboratory, FR
Gabriela Nicolescu, Ecole Polytechnique de Montreal, CA

Multi-processor SoC (MPSoC) are required for many emerging applications such as multimedia, telecommunication, and even consumer and automotive. Simulink/Matlab is emerging as the solid candidate for MPSoC design and programming. This tutorial introduces state-of-the art technologies based on Simulink/Matlab for the design of MPSoC:

- Prof. Wolf will give a brief introduction for designing and programming MPSoC.
- Dr Mosterman will talk about using Matlab/Simulink for embedded system design.
- Prof. Sztipanovits will talk about applying model-based techniques to refine Simulink models.
- Edward Power and Tom Pitchforth will detail a case study using Model Driven Design Techniques
- Dr Jerraya will introduce an approach using Simulink to program heterogeneous MPSoC.
- Prof. Nicolescu will present the usage of Simulink for modelling and simulation of heterogeneoussystems.

E **Software Defined Radios: Design for Scalability and Low Energy**

Organisers: Liesbet Van der Perre and Bruno Bougard, IMEC, BE
Speakers: Trevor Mudge, U of Michigan, US
Kees Van Berkel, NXP, NL
Gerd Vandersteen, VUB/IMEC, BE
Bruno Bougard, IMEC, BE
Liesbet Van der Perre, IMEC, BE

"Anything, anywhere, anytime", still, the motto having celebrated its 10th anniversary, today ubiquitous broadband wireless communication bringing multimedia services is not yet fully available. One of the major bottlenecks is the need for low cost, low power, multi-purpose chipsets. Indeed, the variety of wireless standards is large and evolving rapidly. Multi-mode terminals will be needed to provide optimised access according to virtually all those standards. Software Defined Radios (SDRs) turn out to be the only valid solution to enable such versatile chipset in deeper submicron technology. Low power consumption SDR architectures are a vital asset of multi-mode wireless multimedia terminals.

In this tutorial, we will first introduce and motivate the needs and opportunities for SDRs. Next, we will go deeper into the technological challenges. Energy-aware SDRs require both an energy-scalable reconfigurable digital baseband modem and a energy-scalable reconfigurable RF section. The trends and most promising approaches to implement reconfigurable digital baseband processing will be first discussed. Special focus will be set on opportunistically partitioned heterogeneous MPSOC platform, SIMD processor architecture dedicated to baseband processing and hybrid coarse-grain-array/SIMD accelerators. Next, technologies and challenges to design reconfigurable RF front-end will be discussed. We will then show how a cross-layer optimisation methodology and a multi-level adaptive control approach can be used to translate the flexibility and energy-scalability into low-energy operation. Last but not least, we will analyse the consequence of the design paradigm shift induced by SDR on the design flow and tools, also identifying missing technologies towards future generations of SDRs

Target audience: The tutorial is targeted towards designers (system, architectures, circuits, methods and tools) with interest in integrated wireless systems.

F1 **Microfluidic Lab-on-a-Chip Systems: Emerging Opportunities for EDA Researchers and Practitioners**

Organiser: Krishnendu Chakrabarty, Duke U, US
Speakers: Krishnendu Chakrabarty, Duke U, US
S (Krish) Krishnamoorthy, CFD Research Corporation, US

Advances in microfluidic technology have opened up non-traditional applications for electronic circuits and systems. Miniaturised lab-on-chip systems, which combine microfabrication and microfluidics with biological/chemical sciences, can be used for DNA sequencing, immunoassays, blood chemistry, environmental monitoring, etc.

This tutorial will first provide an introduction to microfluidics, underlying physical principles, applications, and advances in design automation techniques. Attendees will learn about continuous-flow systems, where tiny quantities of samples and reagents flow through microchannels and are subjected to analysis. Component level design issues involving filling, dispensing, mixing, dispersion, separation, heating, and biochemical assays will be illustrated, and solution strategies will be assessed with the help of simulations. The next part of the tutorial will focus on "digital" microfluidics, where discrete droplets are manipulated on-chip. The "digital core" of a lab-on-a-chip system can be viewed as a programmable processor, while the continuous-flow components can be used to implement specialised tasks such as chemical separation.

This tutorial is targeted towards EDA researchers and practitioners who are interested in the emerging area of microfluidic lab-on-a-systems, and who are looking for exciting new application areas for EDA algorithms.

G1 Modelling, Analysis and Design of Bus-based SoC Communication Architectures

Organiser: Nikil Dutt, UC Irvine, US
Speakers: Nikil Dutt, UC Irvine, US
Kanishka Lahiri, NEC Laboratories America, US
Sudeep Pasricha, UC Irvine, US

On-chip communication architectures often dominate and critically affect the performance, power and cost of SoC (System-on-Chip) designs. Bus-based on-chip communication architectures that are frequently used in SoC designs today are evolving rapidly due to the combined effect of rapid changes in VLSI technology, coupled with the need to map ever more complex applications on to SoCs. This tutorial covers modelling abstractions suitable for communication-centric design, analysis techniques for estimating power, performance and reliability of different communication configurations, and the synthesis of current bus protocols and standards such as AMBA, CoreConnect and OCP-IP. We will also focus on advanced architectural concepts in bus-based communication architecture design, and present design examples from industry.

The tutorial is intended for designers, architects, managers, CAD tool developers, researchers and students interested in System-on-Chip design, platform-based design methodologies, interconnect issues at the system level and trends in on-chip communication architectures. Attendees should have a basic (undergraduate-level) knowledge of VLSI Design and SoC design flows. No specific knowledge of CAD tools or modelling languages is required for this tutorial.

H1 Scan Delay Testing of Nanometer SoCs

Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue U, US
Speaker: Adit D Singh, Auburn U, US

Scan based delay testing is being widely considered as a cost effective solution for detecting delay defects that are emerging to be a major problem in nanometer technologies. This tutorial presents the basics of the scan based delay test methodology, including application of launch-on-capture and launch-on-shift patterns, and timing issues associated with the scan enable control signal. We also discuss challenges in effectively applying scan delay tests, including addressing poor test coverage, multi-cycle faults, false paths, power supply noise, clock stretching etc. Recently proposed methods to enhance delay test effectiveness, including targeting small delay defects, is also be presented. Prerequisites are basic familiarity with test and DFT.

The tutorial is targeted at designers and DFT engineers of integrated circuits (ICs) and system-on-chips (SoCs), IP core providers and integrators, test engineers, researchers, and managers responsible for ensuring the tested quality and reliability of advanced semiconductor components.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)

F2 Die and Package Power Delivery Analysis and Design for High-Performance and Low-Power Systems

Organiser: Eli Chiprout, Intel Strategic CAD Labs, US
Speakers: Byron Krauter, IBM Corp., US
Rajendran Panda, Freescale Semiconductor, US
Eli Chiprout, Intel Strategic CAD Labs, US

Power supply fluctuations can result in loss of performance or even system failure. This tutorial covers the underlying impact, analysis and design of a power delivery network (PDN) from the die to the package. It describes the impact of reliability, performance, and signal integrity constraints on PDN design. It covers electrical modelling approaches used on die, the tradeoffs involved and the dynamic impact of a die-wide model including interaction with the package. It includes practical modelling and analysis from an industrial point of view. Additionally, it covers recent progress in simulation-based and static PDN excitation approaches.

The tutorial is targeted at designers of power delivery constrained systems, engineers wishing to learn about power delivery issues and solutions, and CAD developers and researchers.

G2 ESL, New Models and Methods to Advance System Level Design

Organiser: Sandeep K Shuklla, Virginia Tech, US
Speakers: Arvind, MIT, US
Rajesh Gupta, UC San Diego, US
Sandeep K Shukla, Virginia Tech, US

ESL can be an enabler for advancing system level design, especially for effective SoC integration. In this tutorial, we examine recent advances in models, and methods that can lead to meaningful ESL tools. Some of these are incremental, e.g., enhancements to high-level modelling languages such as SystemC. Some represent ongoing work in improving abstraction and reuse of IP blocks. We focus on innovations being pursued related to capture and use of meta-data, meta-modeling and reflection mechanisms for reuse. We discuss how these can lead to easier system modelling. Another area we cover is the paradigm of atomic action-oriented modelling for high level concurrency control, corresponding behavioural synthesis, and trade-offs. In particular, we will cover Bluespec's programming model for a powerful ESL methodology that relieves designers from concurrency control concerns, thereby increasing productivity.

The tutorial targets designers of integrated circuits (ICs) and system-on-chips (SoCs), IP core providers and integrators, researchers, and managers who are involved in embedded system design at the system

H2 Practices in Analogue, Mixed-Signal and RF Testing

Organisers: Dimitris Gizopoulos, Piraeus U, GR and Kaushik Roy, Purdue U, US
Speakers: Salem Abdennadher, Intel Corporation, US
Saghir A Shaikh, Sun Microsystems, US

This tutorial describes the existing industry ATE-, DFT- and BIST-based testing solutions for mixed-signal and RF SoCs. Firstly, it looks at the basic concepts in analogue and RF measurements (i.e. eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, etc.). Secondly, it presents several examples of production testing of wired (SERDES) and wireless transceivers, as well as high-speed IO interfaces (e.g. PCI-Express and XAUI, etc). In addition, block-DFT solutions are also discussed for PLLs, equalisers, filters, mixers, AGCs, LNAs, DACs and ADCs.

A prerequisite for this tutorial is a basic knowledge of the design and production-test flows for mixed-signal devices. The tutorial is aimed specifically at design, test and DFT engineers involved in the actual implementation of mixed-signal and wireless devices and systems. However, architects and engineering managers would also benefit considerably from this session.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)