EDAA/DATE PhD Forum

The EDAA/DATE PhD Forum offers the opportunity for PhD students to present their thesis work to a broad audience in the design automation and test community from both academia and industry. During the presentation at the DATE Conference it helps students to establish contacts when entering the job market. On the other side, representatives from industry and academia get a glance of state-of-the-art research in design automation and test.
This year we received a total of 125 submissions out of which 53 have been accepted for presentation at a dinner reception. The review process was conducted by a team of 10 internationally renowned reviewers. Our thanks go to all presenters, the PhD Forum Committee and all who were involved in conducting the review process and arranging and organizing the Forum event at DATE in Nice. We also thank the EDAA and DATE organizers and representatives for making this Forum possible.

Jörg Henkel
Chair 2007 EDAA/DATE PhD Forum

PhD Forum Committee

J. Henkel (Chair), Univ. Karlsruhe, Germany
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A. Shrivastava, Arizona State University, USA
F. Slomka, Univ. Oldenburg, Germany
Y. Xie, Penn. State University, USA

Presentations

Angiolini, F., Univ. Bologna, "NoCs: From Idea to Implementations"
Arteaga, A., Univ. Seville, "Digital Background Calibration of Pipeline ADCs"
Babighian, P., Intel Ireland Ltd., "Methodologies and Techniques for Power Optimization of Digital Circuits"
Bacivarov, I., ETH Zürich, "Performance evaluation for heterogeneous MPSoC design"
Boden, M., Fraunhofer-Inst. Dresden, "Hierarchical High-level Synthesis of Dynamically Reconfigurable Hardware Tasks Including their Optimized Implementation on RTL"
Bombieri, N., Univ. Verona, "A TLM Design for Verification Methodology"
Braun, A., Univ. Tübingen, "A semi-automated heuristics for guided performance optimization"
Dittmann, F., Nixdorf Inst. Paderborn, "A Reconfiguration Port Scheduling Layer for Real-Time Execution on FPGAs"
Dopatka, F., Univ. Siegen, "A Framework for Implementing Realtime Industrial Ethernet Networks with Variable COmpatibility to Standard Ethernet including Hot-Pluggable Asynchronous Devices"
Erbas, C., Univ. Amsterdam, "System-level Modeling and Design Space Exploration for Multiprocessor Embedded System-on-Chip Architectures"
Faurax, O., Lab. SESAM Gardanne, "Model and tools for the evaluation of circuit robustness against fault attacks"
Fawaz, N., HS Offenburg, "Biomedical Telemetry Application of an Electronic Capsule with Enhanced Performance"
Fey, G., Univ. Bremen, "Increasing Robustness and Usability of Circuit Design Tools by Using Formal Techniques"
Gorden-Ross, A., Univ. California Riverside, "Dynamic Optimization of Highly Configurable Caches for Reduced Energy Consumption"
Hack, S., Univ. Karlsruhe, "Register Allocation for Programs in SSA-Form and possible Implications for Processors"

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Hamann, A., Univ. Braunschweig, “Compositional Design Space Exploration for Embedded Systems”
Harutyunyan, G., Yerevan Univ. Armenia, “Minimal March Tests for Fault Detection. Location an Diagnostics of Static and Dynamic Faults in SRAMS”
Henia, R., Univ. Braunschweig, “Context-aware Performance Analysis for Embedded Systems”
Hübner, M. Univ. Karlsruhe “Dynamic and Partial Reconfigurable Hardware System Architecture with Real-time On-demand Functionality”
Kikkeri, N., South. Meth. Univ. Dallas, “Towards efficient Formal Hardware Verification by Theorem Proving”
Klingauf, W., Univ. Braunschweig, “Transaction-level HW/SW System Modeling with SystemC”
Kobayashi, Y., Univ. Osaka, “Compilation Technique for Low Energy VLIW Processors Using Operation Shuffling and L0 Cluster Generation”
Lange, S., Univ. Leipzig, “Concepts and Methods for Hyperreconfigurable Architectures”
Lara, C., R. K. Univ. Heidelberg, “The SysMES architecture: System Management for Embedded Systems”
Lin, I., Penn. State Univ., “System Level Power and Reliability Modeling and Estimation”
Ma (Ms.), M., McGill Univ. Montreal, “Model Order Reduction Methods for Efficient Modeling and Simulation fo Interconnect Networks”
Morra, C., Univ. Karlsruhe, “A flexible framework for hardware/software design space exploration using rewriting logic”
Muenker, C., Infineon Munich, “Spectral PLL BIST for Integrated Cellular Transceivers”
Murgan, T., Univ. Darmstadt, “High-Level Optimization of Performance and Power in Very Deep Sub-Micron Interconnects”
Narayanan, S., Penn. State Univ., “DATE 2007 PhD Forum Submission”
Neumann, B., RWTH Aachen, “Design and quantitative analysis of ASIPs with eFPGA-based accelerators as flexible ISA-extension”
Nilsson, A., Univ. Linköping, “Design of programmable multi-standard baseband processors”
Octavian, P., Univ. Linköping, “Analysis and Optimization of Hierarchically Scheduled Distributed Embedded Systems”
Ozcan, A., STMicro Grenoble, “An extensible Toolset for Component-based Software Development”
Paci, G., Univ. Bologna, “Exploring temperature-aware design in low-power MPSoCs”
Padmanabhan, A., Lindquist Center Iowa, “SOG: A Self-organized Grouping Infrastructure for Grid Resource Discovery”
Pasricha, S., Univ. California Irvine, “COMMSYN: On-Chip Communication Architecture Synthesis for Multi-Processor System-on-Chips”
Patel, H., Virginia Tech. Blacksburg, “ISLAND: Ingredients for Successful System Level Automation & Design Methodology”
Rodríguez, F., Univ. Madrid, “Avoiding CAM structures on memory-disambiguation hardware”
Ruggiero, M., Univ. Bologna, “Abstract”
Shukla, S., Univ. Queensland, “QUKU: A Coarse Grain rSoC Architecture on FPGA”
Siozios, K., Univ. Thrace, “Application-domain-specific Reconfigurable FPGA Platform: An Integrated Hardware and Software Design Approach”
Soffke, O., Univ. Darmstadt, “Modeling and Simulation of Printed RFID Tags in Inductively Coupled Systems”
Stitt, G., Univ. California Riverside, “Synthesis from Software Binaries”
Teichmann, P., Inst. Mikroel.& Mech Erfurt, “Using BISC to improve integration level and yield of ISM-band receiver ICs”
Telandro, V., Lab.Mat. & Microel. Toulon, “On-chip Voltage Regulator Protecting Smart Cards Against Power Analysis Attacks”
Troeger G., Univ. Heidelberg, “Improving Radiation Tolerance of FPGAs in High-Energy Physics applications”
VahidfarM. , Univ. Pavia, “A high IIP CMOS Front-End Receiver for Zero-IF Multi-Standard Applications”
Viana P., Univ. Bosque, Brasil, “A Methodology to Explore the Deisgn Space of Memory Hierarchies for Embedded Systems”
Wang F., Penn. State Univ., Reliable “System Design atop of Unreliable Components”
Wang Y., Tsinghua Univ. Beijing, “Circuit-level Leakage Reduction Techniques in Deep Submicron IC Designs”
Wedler M., Univ. Kaiserslautern, “Model generation for SAT-based property checking”
Wei Y., Univ. Stony Brook, “Research Abstract”
Zhu G., Univ. Waterloo, “Nonlinear Circuit Sensitivity Calculation and Distortion Decomposition”