Reduction of Detected Acceptable Faults for Yield Improvement via Error-Tolerance

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Abstract

Error-tolerance is an innovative way to enhance the effective yield of IC products. Previously a test methodology based on error-rate estimation to support error-tolerance was proposed. Without violating the system error-rate constraint specified by the user, this methodology identifies a set of faults that can be ignored during testing, thereby leading to a significant improvement in yield. However, usually the patterns detecting all of the unacceptable faults also detect a large number of acceptable faults, resulting in a degradation in achievable yield improvement. In this paper, we first provide a probabilistic analysis of this problem and show that a conventional ATPG procedure cannot adequately address this problem. We then present a novel test pattern selection procedure and an output masking technique to deal with this problem. The selection process generates a test set aimed to detect all unacceptable faults but as few acceptable faults as possible. The masking technique then examines the generated test patterns and identifies a list of output lines that can be masked (not observed) during testing so as to further avoid the detection of acceptable faults. Experimental results show that by employing the proposed techniques, only a small number of acceptable faults are still detected. In many cases the actual yield improvement approaches the optimal value that can be achieved.

1 Introduction

As the advance of VLSI process technologies approaches physical limits, process variations as well as quantum effects of nanometer circuits make it difficult to manufacture defect-free chips [1][2]. Thus, one severe problem with these new nanometer technologies is low yield. Classical techniques to increase chip yield, such as fault-tolerance and defect-tolerance, appear to be inadequate to overcome this problem [3][4]. In addition, currently system-on-a-chip (SOC) and/or embedded systems are widely used, especially for non-critical applications such as cell phones and iPods. Consequently, the concept of error-tolerance has received much attention [1][3][4]. Under this concept, error-producing defective chips that provide acceptable performance with respect to a specific application are marketable, thus resulting in an increase in effective yield. Due to human insensitivity to tiny vibrations in sounds, smells and colors, this concept can be applied in a wide range of multimedia applications [5][6]. The need for error-tolerance was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS) [1], where it was stated that "relaxing the requirement of 100% correctness in both transient and permanent failures of signals, logic values, devices, or interconnects may reduce the cost of manufacturing, verification and testing." How to cost-effectively identify acceptable defective chips is one of the central themes in this emerging field. Several attributes have been employed to evaluate the acceptability of defective chips and some corresponding measurement methods have also been developed in previous work [3]-[8]. One of these attributes is error-rate.

In [7] a fault-oriented test methodology (see Figure 1) supporting error-tolerance based on error-rate estimation [4] for each target fault in a circuit was proposed. This test methodology first makes use of a sampling-based method to estimate the error-rate of each individual fault in the target circuit. The estimated error-rate data along with the maximum acceptable system error-rate specified by the user (system developer) are then used to identify a set of faults that can be ignored during manufacture testing without violating the system error-rate requirement. Therefore, the quality of the tested chips can be maintained at an acceptable level and the effective yield can be significantly enhanced.

Under this novel concept, the "target" of testing is transformed to only the *unacceptable faults* rather than all possible faults as considered in conventional testing. To detect only unacceptable faults during testing, the generation of appropriate test patterns is crucial [5][6][8].

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It can be expected that without careful consideration, the patterns generated for all of the unacceptable faults can also detect a large number of acceptable faults, resulting in a drastic degradation in achievable yield improvement. This "over-detection" problem, if not appropriately dealt with, can invalidate the effectiveness of the error-tolerance methodology based on error-rate estimation.

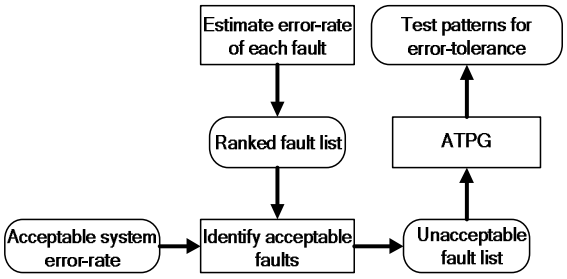

Figure 1: Error-rate based test methodology

In this paper, we first formally formulate the over-detection problem based on a probabilistic analysis, followed by a discussion of the key factors affecting the success of test pattern generation. Then we propose a novel test pattern selection and an output masking technique to address this problem. The proposed test pattern selection technique can effectively generate an appropriate test set that detects all of the unacceptable faults but as few acceptable faults as possible. Although this procedure avoids the detection of most acceptable faults, some acceptable faults are still detected. Thus we next discuss an output masking technique that identifies a list of output lines that should not to be observed during testing so as to further reduce the number of detected acceptable faults. Experimental results show that by means of the proposed techniques, only a small number of acceptable faults are still detected. In many cases the actual yield improvement approaches the predicted optimal value.

This paper is organized as follows. In Section 2, a brief review on the identification of acceptable faults will be given and the over-detection problem will be analyzed and discussed. The proposed test pattern selection method and the output masking technique are described in Sections 3 and 4, respectively. Experimental results showing the effectiveness of the proposed techniques are presented in Section 5. In Section 6, conclusions are delineated.

2 Analysis of Over-Detection Problem

In this section, the over-detection problem of acceptable faults and its impact on yield improvement are analyzed and discussed. We first give a brief review on how to identify acceptable faults for a chip. According to [7], the expected error-rate of a chip passing a test that ignores k faults indexed by 1, 2, …, k can be represented by

$$E_k = 1 - (1 - f_1) \times (1 - f_2) \times \ldots \times (1 - f_k) \quad (1)$$

where E_k is the expected error-rate of the chip and f_i is the probability that fault i will cause erroneous operation.

If E_k is less than or equal to the acceptable error-rate, denoted by AE, then this chip is acceptable and thus these k faults can be identified as acceptable faults, as formulated below.

$$E_k = 1 - (1 - f_1) \times (1 - f_2) \times \ldots \times (1 - f_k) \le AE \quad (2)$$

Under the equal occurrence rate assumption of each fault [7], to maximize yield improvement we should maximize the number of acceptable faults. This can be done by sorting the faults according to their f_i values and then fitting these f_i's into Eq.(2) in the ascending order of f_i. The maximum number of f_i's that can be fit into Eq.(2) then represents the maximum number of acceptable faults [7].

To effectively improve yield within the framework of error-tolerance, acceptable faults should not be detected by the applied test patterns. However, as will be shown next, the patterns generated by an ordinary ATPG tool to detect all of the unacceptable faults usually also detect many acceptable faults. We begin with the detection probability of faults by a random pattern. The following notations will be used.

- $EV_{a,i}$: The event that a random pattern detects i acceptable faults
- $EV_{u,j}$: The event that a random pattern detects j unacceptable faults
- Prob ($EV_{a,i}$ | $EV_{u,j}$): the probability that event $EV_{a,i}$ occurs under the condition that event $EV_{u,j}$ has occurred

The expected number of detected acceptable faults by a random pattern detecting at least one unacceptable fault, denoted by $\#DAF_{exp}$, can then be obtained as follows.

$$\#DAF_{\exp} = \sum_{i=1}^{n_A} i \times \left(\sum_{j=1}^{n_U} \mathrm{Prob}(EV_{a,i} | EV_{u,j}) \right) \quad (3)$$

where n_A and n_U are the numbers of acceptable and unacceptable faults, respectively.

The exact calculation of Eq. (3) involves consideration of the circuit structure and the relation between faults, hence requiring high computation cost [9]. To simplify this problem so as to facilitate the analysis procedure, we will assume that the expected numbers of unacceptable and acceptable faults that will be detected are independent. We collect and classify these two kinds of faults into two separate groups and take the average value of error-rates of them as the expected error-rates of faults in these two groups. Then the problem can be simplified to the calculation of the probability that a fault in one group is detected under the condition that a fault in the other group is detected using a random pattern. This can be formulated using the following notations.

- $EV_{a,avg}$: the event that a random pattern detects a certain acceptable fault
- $EV_{u,avg}$: the event that a random pattern detects a

certain unacceptable fault

- Prob ($EV_{a,avg}$ | $EV_{u,avg}$): the probability that event $EV_{u,avg}$ occurs under the condition that event $EV_{u,\,avg}$ has occurred

The expected number of detected acceptable faults by a random pattern detecting a certain unacceptable fault is given by the equation

$$\#DAF_{exp,avg}=\text{Prob}(EV_{a,avg}|EV_{u,avg})*n_A \quad (4)$$

Based on Eq. (4), if *#tp* random patterns that detect all of the unacceptable faults are applied during testing, then the expected total number of detected acceptable faults will be

$$\#DAF\_total_{exp,avg}=(1-(1-\text{Prob}(EV_{a,avg}|EV_{u,avg}))^{\#tp})*n_A \quad (5)$$

Under the assumption that the detection of an acceptable fault is independent of that of an unacceptable fault, this expression reduces to

$$\#DAF\_total_{exp,avg}=(1-(1-\text{Prob}(EV_{a,avg}))^{\#tp})*n_A \quad (6)$$

Without loss of generality, assume faults 1, 2, …, n_A are acceptable. Then Prob($EV_{a,avg}$) is given by

$$\text{Prob}(EV_{a,avg}) = \sum_{j=1}^{n_A} e_j \,/ n_A,$$

where e_j represents the error-rate of fault j [7].

The yield improvement realized by ignoring acceptable faults is $EY = (1\text{-}p)^{n-n_A}$, where p is the occurrence rate of each fault [7] and n is the total number of possible faults. The impact on expected yield improvement due to detection of acceptable faults is

$$EY_{\text{exp,avg}} = (1\text{-}p)^{n-n_A+\#DAF\_total_{\text{exp, avg}}} \quad (7)$$

To illustrate this impact we considered five ISCAS 85 benchmark circuits and used the test patterns generated by an ATPG tool targeting only unacceptable faults. Prob ($EV_{a,avg}$) is obtained according to the error-rate estimation results for each fault with 10,000 sample patterns [7]. Table 1 shows the analysis results based on Eq. (6) and (7) under various natural yields (*NY*) when the acceptable system error-rate is set to 0.01. The value of *PDAF* represents the expected percentage of the acceptable faults that will be detected by the applied patterns (i.e., $\#DAF\_total_{exp,avg}/\ n_A$ *100%). From Table 1 one can see that on average, a large fraction of acceptable faults are detected, thus degrading the yield improvement. For example, when the natural yields are 0.9, 0.5 and 0.1, the *PDAF* for C7552 will be 58.48%, 57.14% and 42.30%, and the effective yields (*EY*) will be reduced from 0.984 to 0.934, from 0.680 to 0.571 and from 0.187 to 0.144, respectively. These results show that appropriately dealing with the over-detection problem is critical for the success of error-tolerance based on error-rate estimation.

From Eq. (5) one can find that the number of detected acceptable faults depends on a) the number and error-rates of acceptable faults, b) the number of test patterns applied during manufacturing test, and c) the occurrence of the event $EV_{a,i}|EV_{u,j}$. Given an acceptable error rate, in general we would like to ignore the maximum number of acceptable faults and hence factor a) should be kept intact. Therefore, b) and c) are the two key factors to consider for the over-detection problem.

In our experiments, we found that the test patterns generated by a commercial ATPG procedure detect a large number of acceptable faults. Thus a new test generation procedure has to be developed. In this work, we address factors b) and c) given above by proposing a new test pattern selection technique, as described next.

Table 1: Degradation in yield improvement

		C499	*C1908*	*C3540*	*C5315*	*C7552*
***NY* =0.9**	***EY***	0.971	0.979	0.991	0.991	0.984
	PDAF(%)	48.17	51.07	45.74	45.51	58.48
	$EY_{exp,avg}$	**0.936**	**0.938**	**0.948**	**0.948**	**0.934**
***NY* =0.5**	***EY***	0.620	0.711	0.735	0.671	0.680
	PDAF(%)	39.57	25.79	46.12	62.03	57.14
	$EY_{exp,avg}$	**0.569**	**0.649**	**0.615**	**0.559**	**0.571**
***NY* =0.1**	***EY***	0.164	0.258	0.231	0.163	0.187
	PDAF(%)	19.02	13.70	36.57	57.84	42.30
	$EY_{exp,avg}$	**0.149**	**0.227**	**0.170**	**0.123**	**0.144**

3 Test Pattern Selection Technique

The flow chart of the proposed test pattern selection technique is shown in Figure 2. Our selection procedure starts with the same sample patterns that were pseudo-randomly generated by a linear feedback shift register (LFSR) to determine the error-rate of each fault [7]. The reason we use these patterns is that, in general, those faults having a large impact on system error-rate are likely to be associated with a high error-rate, hence are relatively easy to be detected by random patterns. Since the sample patterns are random and their effect on all faults has already been determined when calculating the error-rates, it is advantageous to make use of this fault detection information that is already available. We next describe the details of Figure 2. Some notations used are given below.

T_{IDL}: the set of all ***ideal test patterns***, where an ideal test pattern is a pattern that detects only unacceptable faults of the target circuit.

T_{SEC}: the set of all ***secondary test pattern***, where a secondary test pattern is one that detects at least one unacceptable fault and at least one acceptable fault of the target circuit.

U-UF: ***undetected unacceptable faults***, i.e., the faults that are unacceptable and have not been detected by the current test set.

In our test pattern selection procedure, the set of ideal test patterns is first considered in an attempt to detect as many unacceptable faults as possible. If some unacceptable faults remain untested after this process, then the set of secondary test patterns are considered.

Referring to Figure 2, based on the sample patterns as well as the acceptable and unacceptable fault lists obtained by the identification method in [7], we first perform a fault simulation procedure to construct a fault dictionary. Then based on this dictionary, we identify the ideal and secondary test patterns from the sample patterns and classify them into T_{IDL} and T_{SEC}, respectively. Then we check whether there are any undetected unacceptable faults, represented by U-UF. If there are, we check whether there are unselected patterns in T_{IDL} that can detect any of the remaining U-UF's. If yes, then we select an appropriate test pattern based on the following mechanism.

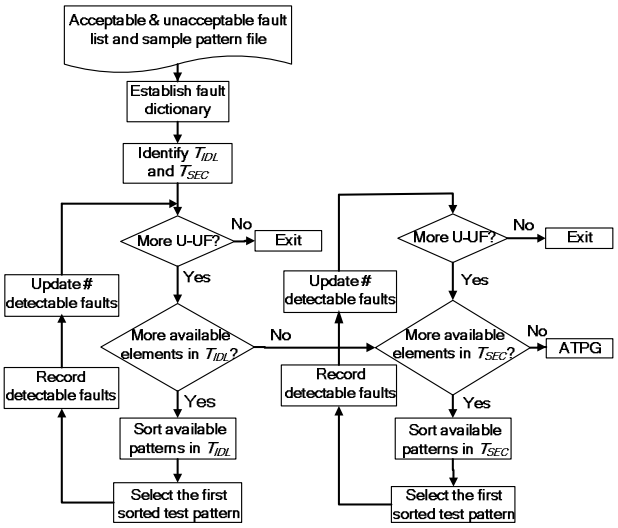

Figure 2: Flow chart of test pattern selection technique

We first sort the test patterns in T_{IDL} in decreasing order of the number of undetected unacceptable faults they detect (this information can be obtained from the fault dictionary). We then select the first element in this list, i.e., the test detecting the most number of U-UF's, and record the faults detected by this pattern (the information is stored in the fault dictionary). Next, the undetected acceptable and undetected unacceptable faults that can be detected by the selected pattern are recorded and the numbers of such faults are updated. The above procedure is repeated until all unacceptable faults are detected or the elements in the sorted list are exhausted. The procedure either stops when the former case is encountered, or proceeds to the loop shown on the right side of Figure 2. For the latter case, patterns in T_{SEC} will be selected. These patterns are ordered in the increasing number of the undetected acceptable faults they detect. The objective of this heuristic is to reduce the number of acceptable faults detected by each of the selected test patterns. The selection procedure of T_{SEC} is similar to that of T_{IDL}. Note that patterns detecting no unacceptable faults will not be taken into consideration during this procedure. After both procedures have been executed, if some unacceptable faults still remain undetected, then an ATPG procedure targeting these faults is executed.

4 Output Masking Technique

After applying the test pattern selection method described in Section 3, some acceptable faults may still be detected by the selected test patterns. To further avoid the detection of these faults, we consider the fact that in general a fault can be detected by more than one test pattern and the fault effects stimulated by each pattern can be propagated to more than one output line. Since it is sufficient to detect an unacceptable fault by observing only one erroneous output of one test pattern, many erroneous output bits can be viewed as redundant and can be "masked" during test application time, i.e., we can intentionally not observe these output lines so as not to detect acceptable faults. The basic idea of our output masking technique is to mask as many output bits as possible that detect acceptable faults while still assuring all unacceptable faults can be detected. The flow chart for this technique is shown in Figure 3 and explained below.

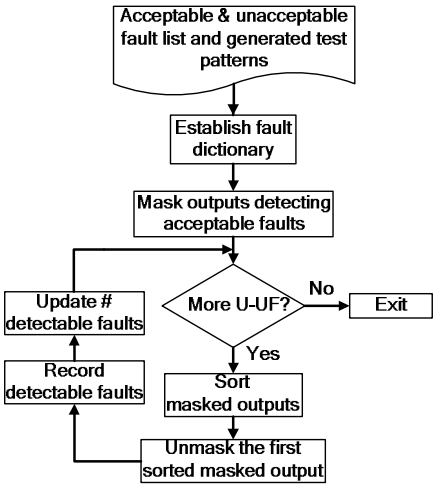

Figure 3: Flow chart of output masking technique

We begin with the list of acceptable and unacceptable faults as well as the test patterns generated by the procedure described in Section 3. Via fault simulation, we determine the relationship between faults, test patterns and which output lines of the target circuit contain an error. For each test pattern, all output lines that detect at least one acceptable fault are first masked. After this step, if all of the unacceptable faults can still be detected, then the detection of acceptable faults is totally avoided and no further action is needed. If some unacceptable faults become untested, we have to "un-mask" some output lines to assure the detection of these faults.

The loop in Figure 3 first checks if all of the unacceptable faults can be detected. If yes, this procedure terminates. Otherwise, the procedure to un-mask masked

outputs is executed. In this procedure, the masked output lines are sorted in decreasing order of their values of ($\#DUF_i - \#DAF_i$), where $\#DUF_i$ and $\#DAF_i$ represent the total numbers of unacceptable and acceptable faults that can be detected at output line i for each test pattern, respectively. This information can be obtained from the fault dictionary. This heuristic aims to un-mask the output that detects most unacceptable but fewest acceptable faults. We un-mask the first element of the sorted output lines and record the faults that become newly detected. Next, the numbers of undetected acceptable and undetected unacceptable faults are updated. This procedure (loop) is repeated until all unacceptable faults are detected.

5 Experimental Results

Five ISCAS 85 benchmark circuits are employed in our experiments and the results are shown in Table 2. The acceptable system error-rates (*AE*) are set to 0.001, 0.005 and 0.01, and the natural yields (*NY*) are set to 0.9, 0.5 and 0.1 for each system error-rate. Row *#tp* in Table 2 indicates the number of required test patterns generated by a conventional ATPG tool to obtain 100% fault coverage for all irredundant faults. Row n_A indicates the total number of acceptable faults. The effective yield *EY* is obtained as described in Section 2. *EY* can be considered as the optimal yield that can be obtained by ignoring all acceptable faults. Theoretically, as the number of acceptable faults increases, so does the effective yield, even if *AE* is small. For example, when *AE* = 0.001 and *NY* = 0.5, the *EY* of C7552 increases to 0.567, and reaches 0.680 when *AE* = 0.01. We see that very significant results are obtained for several circuits. For example, when *AE* = 0.01, the yield of C3540 can be increased from 0.5 (*NY*) to 0.735 (*EY*), an increase of about 47%.

Row *#tp'* indicates the number of test patterns generated by a commercial ATPG tool that targets unacceptable faults but does not consider the fact that acceptable faults should not be detected. Row *#DAF'* indicates the number of acceptable faults detected by these test patterns. The resulting effective yield *EY'* is then obtained using the equation $EY' = (1\text{-}p)^{n-n_A+\#DAF'}$. Clearly the test patterns generated by the ATPG tool targeting unacceptable faults detect a large number of acceptable faults (over 50% in many cases), hence resulting in a significant degradation in yield improvement. For example, for C499 circuit, with *AE* = 0.01 and *NY* = 0.9, the five ATPG-generated test patterns detect 67.4% of the acceptable faults. This reduces the effective yield from 0.971 (*EY*) to 0.923 (*EY'*).

Row having headings with the subscript "o" contain the results obtained by the proposed test pattern selection and output masking techniques. The value of EY_o is obtained by the equation $EY_o = (1\text{-}p)^{n-n_A+\#DAF_o}$, where $\#DAF_o$ is the number of acceptable faults still detected after applying the two techniques. The row labeled *Masked (%)* indicates the fraction of output bits that are not observed due to output masking.

Compared with the ATPG-generated test patterns, much fewer acceptable faults are detected. For example, for C499 when *AE* is 0.01 and *NY* is 0.9, 14 test patterns are selected and 18.75% of all output lines are masked. The number of detected acceptable faults decreases from 368 to 10 and the resulting effective yield is 0.970 (EY_o), which is quite close to the predicted optimal yield improvement of 0.971 (*EY*).

6 Conclusions

By ignoring a set of acceptable faults, a fault-oriented test methodology can be employed to effectively improve yield. In this paper, we have shown that a conventional ATPG procedure targeting only unacceptable faults will generate test patterns that also detect many acceptable faults, thereby greatly degrading the yield improvement. To address this issue, we propose a novel test pattern selection procedure and an output masking technique. Experimental results show that the number of detected acceptable faults is significantly reduced and hence the yield improvement based on the concept of error-tolerance can be achieved in practice.

Acknowledgement

This work was supported in part by the National Science Council of Taiwan under Contract No. NSC95-2215-E-006-023 and in part by the National Science Foundation of USA under Grant No. 0428940. Any opinions, findings, and conclusions or recommendations expressed in this paper are those of the authors and do not necessarily reflect the views of the National Science Foundation.

Reference

[1] Int'l Technology Roadmap for Semiconductors, 2003, http://public.itrs.net/Files/2003ITRS/Home2003.htm.

[2] N.R. Shanbhag, "Reliable and efficient system-on-chip design," IEEE Computer, 37(3): 42-50, May 2004.

[3] M. A. Breuer, S. K. Gupta, and T. M. Mak, "Defect and error-tolerance in the presence of massive numbers of defects," IEEE Design & Test of Computers 21(3): 216-227, 2004.

[4] M. A. Breuer, "Intelligible test techniques to support error-tolerance," Proc. Asian Test Symp., pp. 386-393, 2004.

[5] H. Chung and A. Ortega, "Analysis and testing for error tolerant motion estimation," Proc. Int'l Symp. on Defect and Fault Tolerance in VLSI Systems, pp. 514 – 522, 2005.

[6] I. Chong and A. Ortega, "Hardware testing for error tolerant multimedia compression based on linear transforms," Proc. Int'l Symp. on Defect and Fault Tolerance in VLSI Systems, pp. 523 – 531, 2005.

[7] K.-J. Lee, T.-Y. Hsieh and M. A. Breuer, "A novel test methodology based on error-rate to support error-

tolerance," Proc. Int'l Test Conf., pp. 1136-1144, 2005.

[8] Z. Jiang and S. K. Gupta, "An ATPG for threshold testing: obtaining acceptable yield in future processes," Proc. Int'l Test Conf., pp. 824-833, 2002.

[9] H. Farhat, A. Lioy and M. Poncino, "Computation of exact random pattern detection probability," Proc. Custom Integrated Circuits Conf., pp. 26.7.1-26.7.4, 1993.

Table 2: Experimental results pertaining to the proposed two techniques

	AE	**0.001**			**0.005**			**0.01**		
	NY	0.9	0.5	0.1	0.9	0.5	0.1	0.9	0.5	0.1
C499 (758 possible faults)	***# tp***	53	53	53	53	53	53	53	53	53
	n_A	202	93	49	428	188	122	546	235	163
	EY	**0.926**	**0.544**	**0.116**	**0.955**	**0.594**	**0.145**	**0.971**	**0.620**	**0.164**
	# tp'	12	25	36	7	12	19	5	12	13
	# DAF'	80	39	21	264	66	43	368	113	47
	EY'	**0.915**	**0.525**	**0.109**	**0.921**	**0.559**	**0.127**	**0.923**	**0.559**	**0.142**
	$\#\ tp_o$	39	37	41	19	28	27	14	33	23
	$\#\ DAF_o$	25	9	9	96	13	4	10	33	10
	EY_o	**0.922**	**0.540**	**0.113**	**0.943**	**0.587**	**0.143**	**0.970**	**0.601**	**0.159**
	Masked(%)	2.88	2.79	0.76	4.28	0.89	1.50	18.75	3.22	1.36
C1908 (1,879 possible faults)	***# tp***	110	110	110	110	110	110	110	110	110
	n_A	898	523	275	1255	866	616	1496	954	774
	EY	**0.946**	**0.606**	**0.140**	**0.966**	**0.688**	**0.213**	**0.979**	**0.711**	**0.258**
	# tp'	16	31	58	8	19	22	6	12	19
	# DAF'	423	184	97	639	428	213	786	470	329
	EY'	**0.924**	**0.566**	**0.124**	**0.932**	**0.588**	**0.164**	**0.937**	**0.598**	**0.172**
	$\#\ tp_o$	30	89	85	46	17	83	29	44	41
	$\#\ DAF_o$	17	60	43	248	4	130	271	24	117
	EY_o	**0.946**	**0.593**	**0.133**	**0.952**	**0.687**	**0.181**	**0.964**	**0.705**	**0.224**
	Masked(%)	1.60	3.33	2.35	18.70	0.00	4.14	19.72	12.00	0.88
C3540 (3,428 possible faults)	***# tp***	146	146	146	146	146	146	146	146	146
	n_A	1658	797	488	2642	1510	936	3137	1906	1247
	EY	**0.947**	**0.587**	**0.139**	**0.976**	**0.679**	**0.188**	**0.991**	**0.735**	**0.231**
	# tp'	38	71	93	8	40	62	6	28	50
	# DAF'	856	367	162	807	710	406	1135	791	590
	EY'	**0.922**	**0.546**	**0.125**	**0.952**	**0.588**	**0.143**	**0.957**	**0.627**	**0.156**
	$\#\ tp_o$	131	121	105	48	152	141	26	141	148
	$\#\ DAF_o$	187	85	45	316	221	96	525	167	175
	EY_o	**0.941**	**0.578**	**0.135**	**0.966**	**0.649**	**0.176**	**0.975**	**0.711**	**0.206**
	Masked(%)	18.56	5.97	11.04	73.30	19.47	11.93	80.24	45.36	19.72
C5315 (5,352 possible faults)	***# tp***	113	113	113	113	113	113	113	113	113
	n_A	1813	626	354	3974	1543	783	4891	2273	1141
	EY	**0.933**	**0.542**	**0.116**	**0.973**	**0.611**	**0.140**	**0.991**	**0.671**	**0.163**
	# tp'	43	65	69	15	51	59	6	33	52
	# DAF'	1295	368	155	2351	1150	495	1734	1622	834
	EY'	**0.909**	**0.516**	**0.109**	**0.928**	**0.525**	**0.113**	**0.957**	**0.543**	**0.114**
	$\#\ tp_o$	328	209	84	135	344	265	15	300	347
	$\#\ DAF_o$	572	66	10	609	485	125	355	671	304
	EY_o	**0.921**	**0.536**	**0.116**	**0.961**	**0.572**	**0.133**	**0.984**	**0.614**	**0.143**
	Masked(%)	8.54	1.59	0.30	36.40	6.62	2.78	50.35	9.60	4.89
C7552 (7,548 possible faults)	***# tp***	168	168	168	168	168	168	168	168	168
	n_A	2829	1368	933	5099	2536	1577	6416	3355	2059
	EY	**0.936**	**0.567**	**0.133**	**0.966**	**0.631**	**0.162**	**0.984**	**0.680**	**0.187**
	# tp'	36	58	89	16	38	55	8	30	43
	# DAF'	1788	607	373	3574	1533	795	3933	2242	1145
	EY'	**0.913**	**0.536**	**0.119**	**0.919**	**0.548**	**0.127**	**0.932**	**0.553**	**0.132**
	$\#\ tp_o$	238	169	101	103	242	216	40	168	256
	$\#\ DAF_o$	682	115	30	931	541	149	1812	674	375
	EY_o	**0.927**	**0.560**	**0.132**	**0.954**	**0.600**	**0.155**	**0.960**	**0.639**	**0.167**
	Masked(%)	7.29	0.77	0.19	32.09	6.16	1.20	43.74	13.00	3.26