Process Tolerant β-ratio Modulation for Ultra-Dynamic Voltage Scaling *

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Abstract

Most wireless and hand-held gadgets work in burst mode, and the performance demand varies with time. When the performance requirement is low, the supply voltage can be dithered and the circuit can enter from superthreshold region to subthreshold region ($V_{dd} < V_T$). Such ultra dynamic voltage scaling (UDVS), where the supply voltage switches from $1.2V$ to $200mV$ (say), enables remarkable decrease in power consumption with "acceptable" performance penalty in the non-burst mode of operation. However, subthreshold operation is very sensitive to process variation (PV) due to the reduced noise margin, and may not work properly unless corrective measures are taken. In this paper, we model the trip voltage in both subthreshold and superthreshold regions, and analyze the impact of PV in UDVS. We also propose a circuit design technique such that the same logic gate can efficiently operate in both superthreshold and subthreshold regions under PV. We do that by modulating the β-ratio (P-to-N ratio) of the logic gates. By proper β-ratio modulation, we show that the proposed methodologies can lower energy dissipation per cycle by more than an order of magnitude (42X) in non-burst mode with reduced impact to PVs.

1. Introduction

Efficient power management is becoming increasingly important with the rapid growth of portable, wireless, and battery-operated applications such as cellular phones, personal digital assistants (PDAs), laptops, etc. One of the promising approaches to achieve ultralow power dissipation in such application is to use subthreshold logic [1, 2]. In subthreshold logic, circuits operate with a supply voltage lower than the transistor threshold voltage (V_T) and utilize subthreshold leakage current as the operating current. Previous work has demonstrated subthreshold operation in various digital applications [3, 4]. However, subthreshold type logic has limited performance due to the use of ultralow subthreshold current for computing, which inherently restricts its application to high performance circuits where timing constraints are stringent. As a result, in many real applications, Dynamic Voltage Scaling (DVS) can be combined with subthreshold operation in such a way so as to operate the circuit under normal V_{dd} (superthreshold operation) when higher throughput is required (i.e., burst-mode), while low V_{dd} can be judiciously applied during the power-saving mode. For example, such multi-V_{dd} DVS has been demonstrated with a multiply-accumulate unit [5] and a 32-bit adder [6] to show its effectiveness, and in a 64-bit microprocessor to recover from timing errors while ensuring energy savings [7].

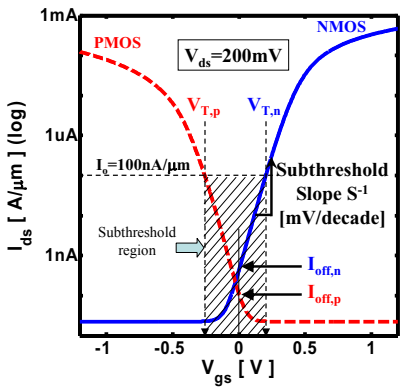

Figure 1. Definition of electrical parameters in typical PMOS and NMOS I-V curves for subthreshold operation.

However, with aggressive scaling of transistor dimension in sub-$100nm$ regime, variation in process parameters is an increasingly significant factor during the design phase. Such concerns are even more important when we consider UDVS when circuit may operate in superthreshold ($V_{dd} > V_T$) or subthreshold ($V_{dd} < V_T$) regions based on workload. While major source of current flow in the superthreshold operation can be explained by the drift mechanism, subthreshold current is mainly due to the diffusion mechanism. This critical difference in the current flow mechanism can pose severe problems in UDVS. In normal (superthreshold operation) CMOS logic cells, the ratio be-

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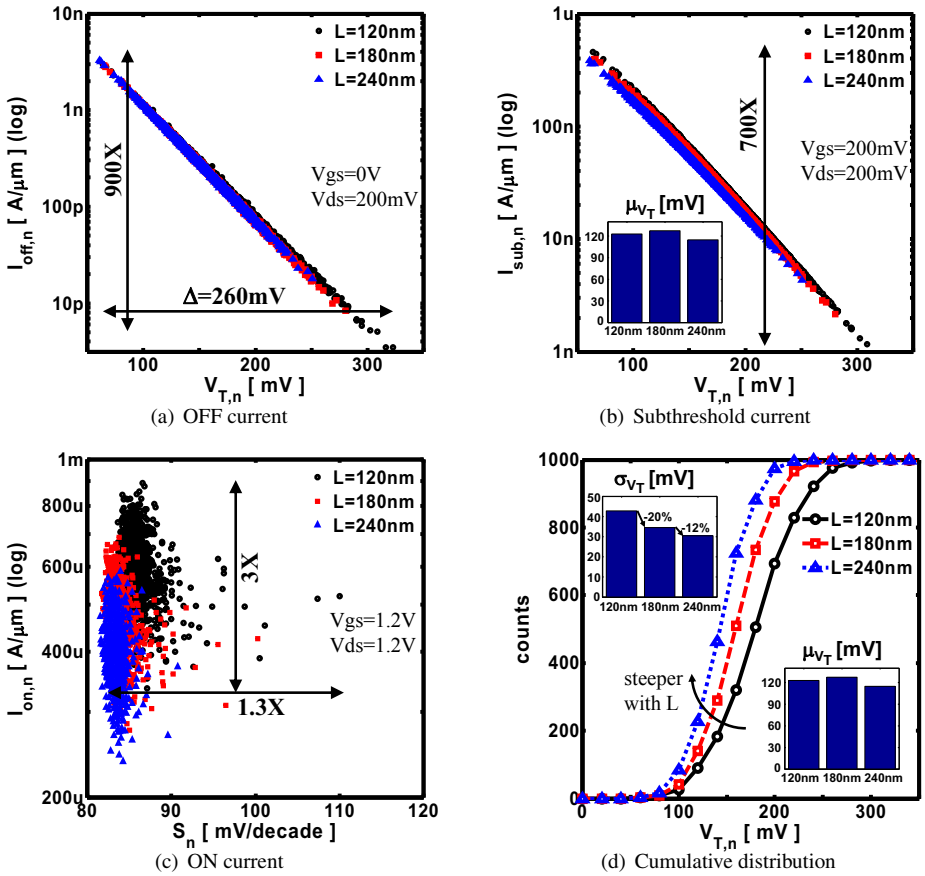


(a) OFF current (b) Subthreshold current

(c) ON current (d) Cumulative distribution

Figure 2. Impact of PVs for different channel lengths (L=$120nm, 180nm, 240nm$ and W=$160nm$).

tween the pull-up and pull-down transistors (i.e., defined as β-ratio) is optimized in order to maximize the noise margin of the cell. However, this optimal β-ratio in superthreshold operation is not identical to that required for subthreshold operation. If the logic cell is solely designed considering the superthreshold operation, the resulting β-ratio (e.g., 2$\sim$3) can lead to a large skew between pull-up and pull-down transistors in subthreshold operations. Such large skew can result in 1) lower performance, 2) higher short circuit power, 3) reduced robustness, and 4) even possible functional failure under PVs [8, 9].

This motivates us to propose an adaptive β-ratio modulation technique to dynamically change the β-ratio depending on the region of operation. During the burst mode, a processor operates in superthreshold region ($V_{dd} > V_T$) where performance is of primary concern. During the non-burst mode, subthreshold operation ($V_{dd} < V_T$) may be sufficient to support the low computational need. Depending on the specific technology node, optimal β-ratios of logic cells are pre-computed for the corresponding operating regions considering the underlying variations in process parameters.

Rest of the paper is organized as follows. In section 2, we analyze the impact of PVs in different operating regions. In section 3, we develop an analytical framework to model trip-point of a logic gate (V_M) under PV in both subthreshold and superthreshold regions. After determining a guideline for PV tolerant circuit design using UDVS in section 4, we propose a circuit technique which increases circuit robustness while operating back-and-forth between superthreshold and subthreshold regions in section 5. The conclusions are drawn in section 6.

2. Impact of PVs in subthreshold and superthreshold operations

As briefly discussed in the introduction, the impact of parameter variation can have severe influence in implementing logic circuits to be operated in both superthreshold and subthreshold regions. To better understand the problem, let us first consider how parameter variations affect the performance of nano-scale transistors. Fig. 1 shows the region of interest for subthreshold operation. The subscripts, p and n refer to PMOS and NMOS transistors, respectively. Simulations were performed in HSPICE using 0.13-μm IBM technology. V_{dd} (=V_{ds}) was set to $200mV$ (subthreshold operation) while V_{gs} was swept from $0V$ to $1.2V$. The OFF current (I_{off}) is defined as a conduction current when V_{gs}

is set to $0V$. The subthreshold current (I_{sub}), the ON current during subthreshold operation, is defined as a conduction current when V_{gs} is set to V_{dd} (@V_{ds}=V_{dd}). Note that V_{dd} in this example is lower than V_T, enabling subthreshold operation.

We have considered both inter-die and intra-die variations in this analysis. Fig. 2 shows the impact of PV for different regions of operation from 1000 Monte-Carlo simulations on a NMOS transistor. In Fig. 2(a), it can be observed that the OFF current (I_{off}) has a wide range of variation (900X) due to PVs, which is equivalent to a ΔV_T=$260mV$ at the supply voltage of V_{dd}=$200mV$. The subthreshold current (I_{sub}) also shows an exponential dependency on changes in V_T for subthreshold operation. With variation in process parameters, I_{sub} fluctuates over a range of $700X$ (Fig. 2(b)). On the other hand, compared to the variations in I_{off} and I_{sub}, the superthreshold ON current (I_{on}) is less sensitive to the impact of PVs, and has a spread of 3X at V_{dd}=$1.2V$ (Fig. 2(c)). It is well known that I_{on} is an *n-th* order (n=$1.2\sim1.5$ for a nano-scale device) function of the gate bias voltage [10]. If V_{dd} is much larger than V_T, I_{on} is less impacted by variation in V_T (ΔV_T). Thus, increasing V_{dd} suppresses the impact of any variation in V_T.

Fig. 2(d) shows the cumulative distributions of V_T under PVs for different L's, and their corresponding standard deviation (σ_{V_T}) and mean (μ_{V_T}) values. Steeper slope in the figure means smaller standard deviation. Increasing device area (increasing L in this case) reduces the impact of PV (e.g., random dopant fluctuation (RDF)) on V_T (see the top inset). One may also consider an area increase through W to reduce the impact of PV [11]. It is interesting to observe a decrease in μ_{V_T} when L increases from $180nm$ to $240nm$ (see the bottom inset). This is due to the reverse short channel effect (RSCE) [12]. However, RSCE has slight impact on I_{on} in superthreshold region where V_{gs} is larger than V_T and the dominant current flowing mechanism is not diffusion but drift.

In summary, PV results in considerable spread in device electrical parameters in subthreshold operation while it is relatively tolerable in superthreshold operation. Hence, a PV tolerant design is necessary at both device and circuit design phase for robust UDVS.

3. Modeling robustness under OFF current mismatch in subthreshold operation

In this section, we first propose an analytical framework to estimate circuit robustness under PV. In the voltage transfer characteristic (VTC) of a static CMOS inverter, the trip voltage (V_M) is defined as the point where the input DC voltage is equal to the output DC voltage (i.e., V_{in}=V_{out}). Ideally, the noise margin is maximized when V_M is at the mid-point of the available voltage swing (i.e., V_M=$V_{dd}/2$). In order to keep V_M close to the half V_{dd} point, it is desirable to have pull-up and pull-down transistors to be of equal strength. Hence, conventionally, in superthreshold logic circuits, the device widths (W_n for NMOS, W_p for PMOS) are usually ratioed in a way to compensate for the mismatch between pull-up and pull-down devices. If due to some reason (e.g., PVs), V_M deviates from its optimal point (i.e., $V_{dd}/2$), the resultant circuit will suffer from an imbalance between the rise and fall times, leading to degraded noise margin and hence robustness. Such deviation can, however, be catastrophic for subthreshold operation.

Let I_o be the subthreshold leakage of a MOS transistor of unit width with its V_{gs}=V_T, V_{bs}=$0V$ and V_{ds}=V_{dd} (see Fig. 1). Then, the subthreshold leakage current can be modeled as [13]:

$$I_{sub} = I_o 10^{\frac{V_{gs}-V_T+\eta V_{ds}+\gamma\sqrt{V_{bs}}}{S}}, \quad (1)$$

where S is the subthreshold slope, η is the drain induced barrier lowering (DIBL) factor, and γ is the body effect coefficient. The OFF current (I_{off}) is defined at V_{gs}=V_{bs}=$0V$ and V_{ds}=V_{dd} in (1). Using I_{off}, the subthreshold current can be rewritten for the pull-up and pull-down transistors in an inverter at V_{gs}=V_M as:

$$\begin{aligned} I_{sub,p} &= W_p \cdot I_{off,p} 10^{\frac{(V_{dd}-V_M)+\eta_p(-V_M)+\gamma_p\sqrt{V_{bs,p}}}{S_p}} \\ I_{sub,n} &= W_n \cdot I_{off,n} 10^{\frac{V_M+\eta_n(V_M-V_{dd})+\gamma_n\sqrt{V_{bs,n}}}{S_n}}. \end{aligned}$$

Let $I_{off,n}$≠$I_{off,p}$, and α=$\frac{I_{off,p}}{I_{off,n}}$ and β=$\frac{W_p}{W_n}$. An analytical expression for V_M can be obtained by equating the currents of the transistors, i.e., $I_{sub,p}$=$I_{sub,n}$:

$$\alpha\beta = 10^{\frac{V_M+\eta_n(V_M-V_{dd})}{S_n} - \frac{(V_{dd}-V_M)+\eta_p(-V_M)}{S_p}}, \quad (3)$$

where we assume zero body bias (i.e., $V_{bs,p}$=$V_{bs,n}$=0). In the devices under consideration, HSPICE simulations show that the DIBL factor, body effect coefficient, and subthreshold slope of the pull-up transistor are comparable to those of the pull-down transistor and they are almost invariant with respect to device size. Assuming η_n≈η_p≈η, γ_n≈γ_p≈γ, and S_n≈S_p≈S, we can simplify (3) to:

$$\begin{aligned} \alpha\beta &= 10^{\frac{(1+\eta)(2V_M-V_{dd})}{S}} \\ \text{or } S\log(\alpha\beta) &= (1+\eta)(2V_M - V_{dd}). \end{aligned}$$

Hence, the trip voltage can be modeled as:

$$V_M = \frac{1}{2}\left[V_{dd} + \frac{S\log(\alpha\beta)}{1+\eta}\right]. \quad (4)$$

To move V_M towards V_{dd}, a large β-ratio is required, which is equivalent to making the pull-up transistor wider.

Our figure of merit, the deviation of V_M from $V_{dd}/2$, referred to as χ_{sub}, can be expressed by:

$$\chi_{sub} = \left| \frac{V_{dd}}{2} - V_M \right| = \left| \frac{S \log(\alpha\beta)}{2(1+\eta)} \right|. \quad (5)$$

Note that any I_{off} mismatch which reduces circuit robustness in subthreshold operation, can be compensated by **modulating the β-ratio**. To express V_M as a function of V_T mismatch and I_{off} mismatch between the pull-up and pull-down transistors, we substitute α and β from (**??**) to (4):

$$\begin{aligned} V_M &= \frac{V_{dd}}{2} + \frac{S}{2(1+\eta)}(\log\alpha + \log\beta) \\ &= K\left(\log I_o 10^{\frac{-V_{T,p}+\eta V_{dd}}{S}} - \log I_o 10^{\frac{-V_{T,n}+\eta V_{dd}}{S}}\right) \\ &\quad + K(\log W_p - K\log W_n) + \frac{V_{dd}}{2} \\ &= \frac{K}{S}(V_{T,n} - V_{T,p}) \\ &\quad + K(\log W_p - \log W_n) + \frac{V_{dd}}{2}, \end{aligned} \quad (6)$$

where K is $\frac{S}{2(1+\eta)}$. If there is no V_T (or I_{off}) mismatch between the pull-up and pull-down transistors ($V_{T,p}$=$V_{T,n}$ or $I_{off,p}$=$I_{off,n}$) for β=1, V_M in (6) becomes $V_{dd}/2$. In addition, any mismatch between $I_{off,n}$ and $I_{off,p}$ moves V_M from $V_{dd}/2$, reducing the robustness of the inverter.

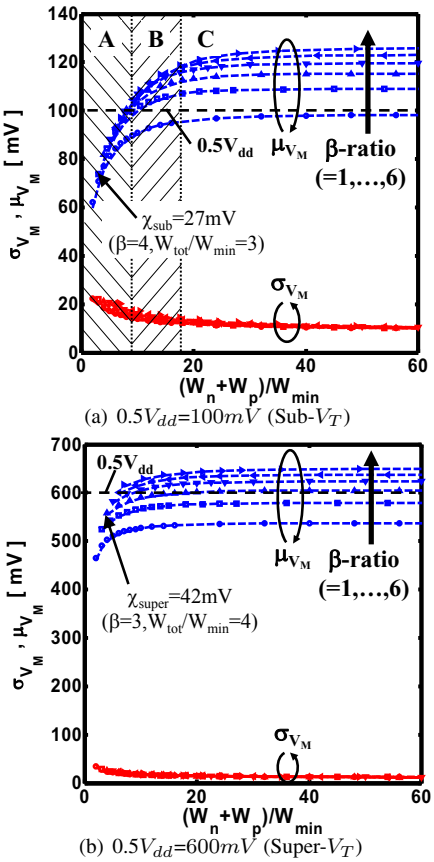
4. Impact of I_{off} mismatch on UDVS

In this section, we will focus on I_{off} mismatch. Note that I_{off} mismatch can occur across a chip due to possible PV. V_M in (6) consists of two terms: the threshold voltage difference and the width difference between the pull-up and pull-down transistors. V_M is a linear function of the V_T difference between the pull-up and pull-down devices. By ignoring geometrical variations (e.g., W variation), the mean and variance of V_M distribution due to V_T fluctuation can be expressed by:

$$\mu_{V_M} = \frac{V_{dd}}{2} + \frac{K}{S}\left(\mu_{V_{T,n}} - \mu_{V_{T,p}}\right) + K\log\beta \quad (7a)$$

$$\sigma_{V_M} = \frac{K}{S}\sqrt{\sigma^2_{V_{T,n}} + \sigma^2_{V_{T,p}}}. \quad (7b)$$

Fig. 3 shows μ_{V_M} and σ_{V_M} of V_M distribution as a function of total device width, W_{tot}=$W_n + W_p$, in an inverter for both subthreshold and superthreshold operations. Each curve corresponds to a different β-ratio. Numerical values from the 1000 Monte-Carlo simulations are plotted with the different markers for β=1,. . .,6. Analytical values from (6) are shown with dotted lines. We assume η_n=η_p=$127mV/V$, and $S = 85mV/decade$. In Fig. 3(a), the entire spectrum



(a) $0.5V_{dd}$=$100mV$ (Sub-V_T)

(b) $0.5V_{dd}$=$600mV$ (Super-V_T)

Figure 3. Variation of V_M for different total widths (W_n+W_p) and β-ratios in an inverter for UVDS operations.

of different width can be categorized into three regions: A, B and C. In region A, where the pull-up transistor is too weak, increasing β-ratio which effectively shifts μ_{V_M} towards $V_{dd}/2$ improves logic robustness. In region B, where the pull-up transistor is strong, decreasing β-ratio improves logic robustness. In region C, σ_{V_M} does not reduce anymore and saturates to a non-zero value around W_{tot}/W_{min}=15 which is 3X∼5X larger than minimum sized design. Note that for small sizes of the PMOS and NMOS, increasing W reduces $\sigma_{V_{T,p/n}}$ and hence reduces σ_{V_M}. However, beyond a certain point, increasing the size of a device does not reduce σ_{V_M} any further. The reason is that even though an increase in device area clearly suppresses the impact of intra-die effect such as RDF [14], it can not suppress the impact of the other inter-die variations which arise from statistical variation during lithographic exposure, chemical reactivity, photon absorption rate, and molecular composition of the photoresist [15, 16]. Further, circuit design in region C requires large area and can result in large power consumption. Hence, our regions of interest are A and B. It is important to note that μ_{V_M} can be shifted by **modulating the β-ratio**. Besides increasing size of the transistors, *changing the "relative" strength ratio* between the pull-up

and pull-down transistors can also reduce the impact of PVs.

V_M in superthreshold operation can be obtained by equating the superthreshold ON currents (i.e., $I_{on,p}$=$I_{on,n}$):

$$\kappa_p W_p \cdot (V_{dd} - V_M - V_{T,p})^{n_p} [1 + \lambda_p (V_{dd} - V_M)] = \kappa_n W_n \cdot (V_M - V_{T,n})^{n_n} (1 + \lambda_n V_M), \quad (8)$$

where κ_p and κ_n are the transconductance parameters of PMOS and NMOS transistors, respectively. In general, PMOS and NMOS transistors have a very similar n factor (n_p and n_n) [10] in the superthreshold region. For simplicity, let us assume the n factors are same (i.e., $n_p \approx n_n \approx n$), and κ_p/κ_n be κ. We solve for the case in which the supply voltage is high enough (super-V_T regime) so that the devices can be assumed to be velocity-saturated. Then, by ignoring λ (DIBL) factors, V_M in superthreshold operation can be simplified to:

$$V_M = \frac{(\kappa\beta)^{\frac{1}{n}} (V_{dd} - V_{T,p}) + V_{T,n}}{1 + (\kappa\beta)^{\frac{1}{n}}}. \quad (9)$$

In conventional circuit design, the PMOS and the NMOS are sized such that for superthreshold operation, an optimal β-ratio (β^{opt}_{super}) is obtained, i.e., $\kappa\beta^{opt}_{super}$=1, to compensate the mobility difference between carriers in PMOS and NMOS transistors. With this optimal β-ratio, (9) can be further simplified as:

$$V_M = \frac{1}{2} [(V_{T,n} - V_{T,p}) + V_{dd}]. \quad (10)$$

For the transistors (β=3 in Fig. 3(b)), the coefficients ($\kappa_p W_p$ and $\kappa_n W_n$) in PMOS and NMOS devices are similar to each other since the nominal value of V_M is very close to $V_{dd}/2$ when their sizes are large. Then, the figure of merit (deviation of V_M from $V_{dd}/2$) in superthreshold operation for the minimum-sized inverter of β=3 can be simplified as:

$$\begin{aligned} \chi_{super} &= \frac{1}{2} |V_{T,p} - V_{T,n}| \\ &= \frac{S}{2} \log \left(\frac{I_{off,p}}{I_{off,n}} \right) \\ &= \frac{S}{2} \log \alpha. \end{aligned} \quad (11)$$

With the nominal values of S=$85mV/decade$ and $I_{off,p}/I_{off,n}$=8.97, χ is $40.5mV$, which is close to the simulation value of $42mV$ at V_{dd}=$1.2V$ (Fig. 3(b)). Similarly, in subthreshold operation where the nominal values of $S = 82mV/decade$ and $I_{off,p}/I_{off,n}$=4.3, by using (6), χ for β_{sub}=4 is $26mV$ which is comparable with simulation value of $27mV$ at V_{dd}=$200mV$ (Fig. 3(a)).

In summary, under PV, the distribution of V_M (or μ_{V_M} as well as σ_{V_M}) should be considered for a robust circuit design. While an increase in area can suppress the range of variation (σ_{V_M}), a modulation in β-ratio can shift the mean of variation (μ_{V_M}) to $V_{dd}/2$.

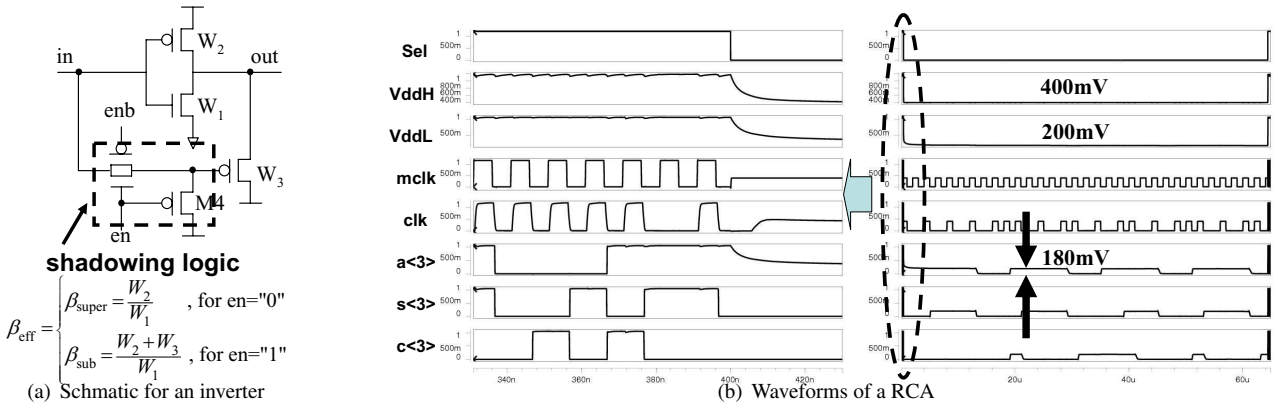
5. Device Shadowing Technique for UDVS

In this section, we propose a circuit technique, henceforth referred to as "device shadowing technique (DST)" which can dynamically reconfigure the β-ratio during operation. Fig. 4(a) shows the basic concept of DST with an example of an inverter, where we assume that the pull-down transistor is weaker than the pull-up transistor. In principle, DST increases the effective width of the weaker network (i.e., PUN or PDN). Two control signals, "en" and "enb" are complementary to each other. In non-burst mode, en=1 and enb=0, and in burst mode, en=0 and enb=1. These control signals turn on the shadowing logic for subthreshold operation (en=1 and enb=0) and turn off it for superthreshold operation (en=0 and enb=1). As a result, the effective β-ratio is W_2/W_1 for $en = 0$ in superthreshold operation, and $(W_2 + W_3)/W_1$ for $en = 1$ in subthreshold operation, to modulate the β-ratio while providing larger current driving capability at low V_{dd}. The additional transistor $M4$ prevents the gate input node of $W3$ from being tri-stated during superthreshold operation.

Fig. 4(b) demonstrates the operation of an 8-bit ripple carry adder (RCA) where β_{super}=2 and β_{sub}=4 obtained by using DST. The supply voltage is $1.2V$ when high computational power is required, and reduced to $200mV$ (V_{ddL}) for non-burst mode. The control signal of "Sel" selects the region of circuit operation: superthreshold operation for Sel=1, and subthreshold operation for Sel=0. To speed up the response time of the transmission gate in the shadowing logic, we have used a clock signal level of $400mV$ (V_{ddH}). Note that all other core logic operates at the supply voltage of $200mV$ during non-burst mode.

Since the conducting current reduces exponentially with supply voltage scaling, subthreshold operation improves energy dissipation in the non-burst mode. For instance, HSPICE simulations with RCA shows that, including clock signal, the energy per cycle is 33.4fJ-sec in subthreshold operation which is 42X smaller than that in superthreshold operation with 9% area overhead. It can be observed that in subthreshold operation the output signal does not have full-swing and its swing range is about $180mV$ even with V_{dd}=$200mV$. This is due to the fact that OFF leakage is not negligible compared to the operating current ($I_{sub}/I_{off} \sim 10^2$, whereas $I_{on}/I_{off} \sim 10^5$, see Fig.2), and the supply voltage level is divided resistively across the pull-up and pull-down transistors in subthreshold operation.

The proposed DST has some drawbacks in superthreshold operation: area overhead and performance degradation due to extra shadow logic. In general, non-burst mode requires considerably lower performance than burst mode. In most applications, only some of the digital blocks operate in non-burst mode and support the minimum computational requirement. At the same time, DST has several other ad-



(a) Schmatic for an inverter (b) Waveforms of a RCA

Figure 4. The proposed DST for adaptive β-ratio modulation.

vantages besides increasing circuit robustness:

- DST makes the weaker network (PUN or PDN) stronger by increasing the effective transistor width. This equalizes the low-to-high and high-to-low transitions, and reduces the short circuit power which, based on our simulations, accounts for 12% of total power consumption in subthreshold operation;
- due to the boosted current, DST enables faster charging or discharging of load capacitance. Especially in the presence of long interconnects, such as a bus, DST provides additional current and decreases buffer delay.

6. Conclusions

In this work, we considered I_{off} mismatch and V_T mismatch between NMOS and PMOS devices in UDVS. Mismatches in I_{off} and V_T pose serious problems as the supply voltage is reduced and may even cause functional failure at ultra-low supply voltage.

Since it is prudent to have the trip voltage of an inverter (V_M) at $V_{dd}/2$, it is essential to design PV tolerant circuits where μ_{V_M} is $V_{dd}/2$ and σ_{V_M} is minimum for a given supply voltage of V_{dd}. Narrowing σ_{V_M} alone is not enough to achieve circuit robustness.

We have developed an analytical framework to model V_M under PV in subthreshold and superthreshold regions. In order to improve circuit robustness even under severe PV and extreme I_{off} mismatch, we have proposed β-ratio modulation which can push μ_{V_M} towards $V_{dd}/2$. Further, DST has been presented as a possible circuit technique to efficiently modulate the β-ratio of CMOS gates based on the operational mode and computational demands.

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