Simulation methodology and experimental verification for the analysis of substrate noise on LC-VCO's

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***Abstract*— This paper presents a methodology for the analysis and prediction of the impact of wideband substrate noise on a LC-Voltage Controlled Oscillator (LC-VCO) from DC up to Local Frequency (LO). The impact of substrate noise is modeled a priori in a high-ohmic 0.18μm 1P6M CMOS technology and then verified on silicon on a 900MHz LC-VCO. Below a frequency of 10MHz, the impact is dominated by the on-chip resistance of the VCO ground, while above 10MHz the bond wires, parasitics of the on-chip inductor and the PCB decoupling capacitors determine the behavior of the perturbation.**

I. Introduction

Thanks to the aggressive downscaling of the transistor dimensions, an increasing amount of analog and digital functionality can be placed on the same die. This allows a reduction of cost and power consumption for many applications. However, this low cost implementation is jeopardized by the problem of crosstalk from the noisy digital to the sensitive analog circuits via the common substrate. On a lightly doped substrate, the most important substrate noise generation mechanism is the coupling of power-supply noise into the substrate [1].

When large digital circuits are switching, high current peaks are drawn from the supply network, which results in ringing on the supply lines. This ringing is injected into the substrate by a resistive coupling of the ground node of the digital circuit via substrate contacts. It then propagates through the common substrate, and hence is called substrate noise. When this substrate noise couples into the sensitive analog and RF circuits residing on the same die, this can severely affect their performance.

Better insight in the coupling mechanisms of substrate noise to the analog/RF circuit will help the designer to take the appropriate measures to make their analog circuit more immune to problems of substrate noise. Hence, the analysis and prediction by simulations of the impact of substrate noise becomes an essential condition to improve the immunity to substrate noise for SoCs.

The VCO, present in most SoC, is a very sensitive analog/RF circuit. A substrate noise signal which couples into the VCO will modulate the oscillator signal in frequency and amplitude. These modulation effects cause sideband spurs around the local oscillator and its harmonics. Furthermore, the noise signal also directly couples to the output in a linear way without frequency translation by the VCO. Figure 1 shows the spectrum of the 900MHz LC-VCO when a sinusoidal signal with a frequency of 304MHz is injected into the substrate.

The sideband frequency spurs around the local oscillator cause the most degradation at low frequencies, because those spurs degrade the phase noise performance of the LC-VCO [3]. At higher frequencies the sideband spurs around the LO and second harmonic of the LO and also the direct coupled spurs can be very harmful. Especially FDD (Frequency Division Duplex) transceivers are very prone to substrate noise coupling. An FDD transceiver transmits and receives simultaneously in different frequency bands. Brenna et al. [4] reports an FDD receiver where transmit and receiver band are separated by 130MHz.

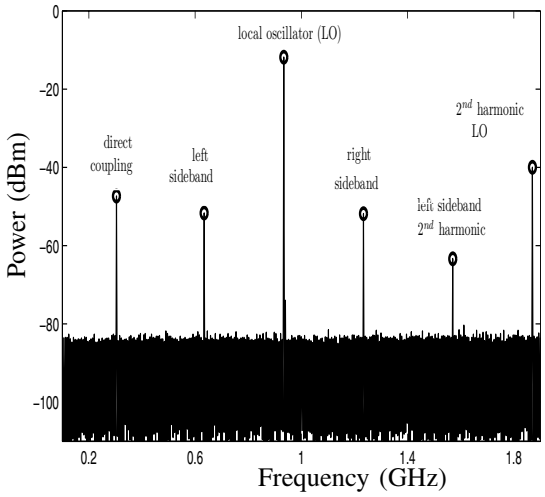

Fig. 1. Measured spectrum of the 900MHz VCO when a sinusoidal signal with frequency of 304MHz is injected into the substrate

Up till now, the impact mechanism of substrate noise is well understood for LC-VCOs from DC to 10MHz [2]. The aim of this work is to extend this frequency range from DC up to 900MHz. Section 2 describes the simulation methodology. Simulations reveal the coupling mechanisms from DC up to LO frequency. The coupling mechanisms are discussed in Section 3. In Section 4 the simulation methodology is validated by measurements. Section 5 describes the influence of the PCB decoupling capacitors on the substrate noise impact.

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II. Impact Simulation Methodology

In order to reveal the impact mechanism from DC up to LO frequency, a simulation model is built. The simulation model consists of an on-chip model and an off-chip model. The on-chip model includes the RF models of the devices, the parasitics of the interconnects, the parasitics of the on-chip inductor, its corresponding shield and the substrate. The off-chip model includes the parasitics of the PCB components and the interconnects. The corresponding netlist of the model is simulated by SpectreRF [7]. This section describes the on- and off-chip simulation model.

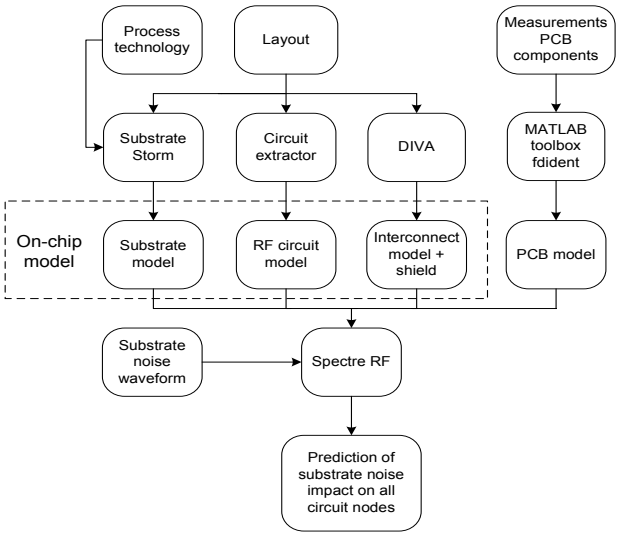

Fig. 2. Substrate noise simulation methodology

A. On-chip simulation model

The extraction of the on-chip simulation model starts from the layout. The circuit netlist containing models for the devices and the parasitics of the interconnects are extracted. To this end an extraction deck is written in DIVA^{TM} [5]. The parasitic resistances of the interconnects are determined based on the geometries and the sheet resistance. The capacitance of the interconnect is determined based on its geometry and the dielectric properties of the oxide. The interconnects are modeled as an RC - mesh in the circuit netlist.

A resistive mesh for the shield of the inductor is extracted because the RF-model of the inductor did not include a model of the shield. The connection of the shield to the substrate is modeled with a resistance because the shield under investigation is a P+ / Poly shield. The shield is connected via a capacitive mesh to the inductor. This RC-mesh is added to the circuit netlist.

The DIVA^{TM} deck recognizes all the devices in the layout and their RF-models are added to the circuit netlist.

Next, the doping profile information is used to extract an RC-netlist for the substrate with SNA^{TM} [6]. This substrate netlist contains two types of external nodes. A first type are the nodes for the connections of the die to the devices in the circuit. A second type are the substrate contacts used to inject disturbances in the substrate or the noisy nodes of a digital circuit. The circuit netlist and substrate netlist are merged into one single on-chip simulation model.

B. PCB simulation model

DC lines are generally off-chip decoupled with Surface Mounted Devices (SMD) capacitors with a set of different values (e.g. 100pF, 100nF and 100μF) in order to decouple in a broad frequency range. In order to build an accurate off-chip simulation model the different off-chip decoupling capacitors are measured with an impedance analyzer (HP4991A). The impedance analyzer returns the impedance values as a function of frequency. This impedance function is then modeled as a linear transfers function in the Laplace variable 's' [11]. This is usually a rational function in 's'. To this end the MATLAB toolbox fdident is used [12]. The selected models are Laplace domain functions with maximum order of 3. The coefficients of this transfer function are used to determine the RLC values of the corresponding network (Figure 3). The error between the model and the measurements is less then 1dB in the frequency range from 1MHz to 1GHz.

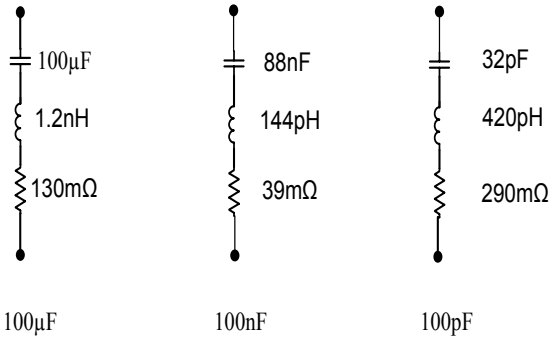

Fig. 3. The decoupling capacitors are modeled by a frequency domain estimator and mapped into an equivalent RLC network

The PCB traces and the bond wires are modeled as transmission lines. The values of the inductance and resistance of the bonding wires and the PCB trances are determined based on their geometry [13]. The models of the bonding wires, PCB traces and PCB decoupling capacitors are merged into one single PCB simulation model.

III. Coupling and impact of substrate noise

The simulation methodology is modeled in a high-ohmic 0.18μm 1P6M CMOS technology and is applied on a 900MHz LC-VCO design. The waveform resulting from substrate noise impact can be predicted on all the nodes of the circuit. The waveforms on the different nodes of the circuit provide insight in the different coupling mechanisms. This section describes the impact mechanisms of the sideband spurs from DC up to LO frequency. The impact mechanism can be divided into four frequency regions :

1) Sideband spurs are caused at low frequencies by FM modulation of the LO.
2) At intermediate frequencies the dominant impact mechanism is moving from FM toward AM modulation.
3) AM modulation is the dominant impact mechanism at high frequencies.
4) Close to the LO frequency, pulling and locking of the LO determines the behavior of the perturbation.

Literature [2], [8] describes the impact of substrate noise at low frequencies. From DC to 10MHz the substrate noise signal couples resistively into the non-ideal ground and causes a voltage drop at the source of the NMOS transistors (Figure 4). This voltage drop results in narrow band FM modulation of the LO signal. The spurs are decreasing with 20dB/decade with the offset frequency [8].

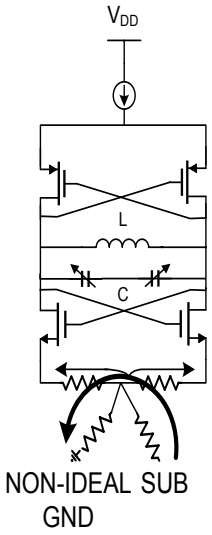

Fig. 4. From DC - 10MHz the substrate noise signal couples resistively in the non-ideal ground and causes narrow band FM of the LO signal

At intermediate frequencies (10MHz to 100MHz) the amplitude of the spurs does not decrease with 20dB/decade anymore but starts to increase with 20dB/decade. A part of the substrate noise signal is drained resistively by the non-ideal on-chip ground toward the PCB through the ground bond wire. Another part of the substrate noise signal couples resistively in the shield of the inductor. This shield is connected with the PCB with a dedicated bond wire. Part of the signal, picked up by the shield is drained toward that dedicated bond wire. Another part of the signal flows through the parasitic capacitance of the inductor (Figure 5). Hence the substrate noise signal couples capacitively to the inductor. This signal is superposed on the oscillation signal across the LC-tank. A higher voltage on the node across the LC tank will cause a larger gate source voltage (vgs) across the transistors of the cross-coupled pair of the LC-VCO. The voltage across the tank is proportional to the vgs across the switching transistors. Because the LC-VCO is operating in current-limited mode, the node across the LC tank is AM modulated. Capacitive coupling resulting in AM modulated spurs explains the increase of 20dB/decade.

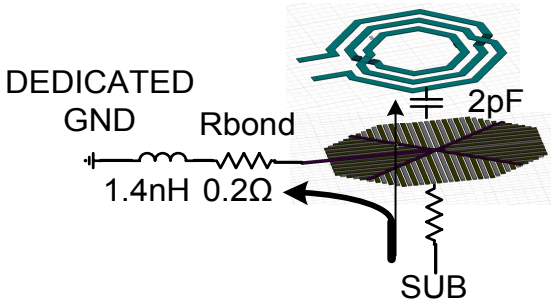

Fig. 5. Starting from 10MHz the substrate noise signal couples capacitively through the inductor

At higher frequencies the substrate noise impact is increasing with 40dB/decade. Above 100MHz the impedance of the shield toward the PCB is determined by the impedance of the bonding wire connected to the shield. Due to the inductance of that bond wire a larger part of the signal couples capacitively to the inductor and less signal is drained to the PCB. The capacitive coupling to the inductor together with the inductance of the bonding wire acts like a second order system. This explains the increase of the substrate noise impact with 40dB/decade. The dominant impact mechanism above 100MHz is AM modulation. DC decouple capacitors at the output of the VCO will attenuate the left sideband spurs resulting of an injected substrate noise signal above 650MHz.

At an offset frequency of 150MHz from the LO frequency substrate noise starts pulling the LO. When the oscillator is perturbed by a substrate noise signal close to the LO frequency, the LO frequency becomes identical to that of the perturbing signal. The VCO locks to the perturbing signal. This injection locking is a non-linear dynamical phenomenon and is not included in the presented model. However non-linear macro models can be found in [10].

IV. Experimental verification of the simulation methodology

An experimental verification of the simulation methodology is essential for the determination of the dominant contributions for substrate noise impact. This section first describes the LC-VCO under test and the measurement setup used for the experimental verification. Afterwards, the experimental validation of the methodology is discussed.

A. Description of the 900MHz LC-VCO and experimental setup

The VCO under test is a 900MHz LC-tank VCO, designed in a 0.18μm CMOS technology on a lightly doped substrate with 20Ωcm resistivity (Figure 6). It consists of a cross-coupled NMOS PMOS transistor pair and a PMOS current mirror. This topology is popular for its low phase noise potential

due to the lower flicker noise of the PMOS devices when compared to NMOS and for its reduced sensitivity to power supply noise. The VCO uses a fully integrated inductor with an inductance of 16nH and a Q factor of 9. The VCO core draws 1.2mA supply current. A worst phase noise of -90dBc/Hz @ 100kHz offset is achieved. This is acceptable given the low inductor Q factor and the rather low current consumption. The accumulation mode NMOS varactors (C_{min} = 1.5pF and C_{max} = 4.5pF) are used to tune the VCO from 750MHz to 1.05GHz. The VCO core is buffered by inverters. Bypass capacitors are added at the output to decouple the DC. The output power of the local oscillator is -12dBm.

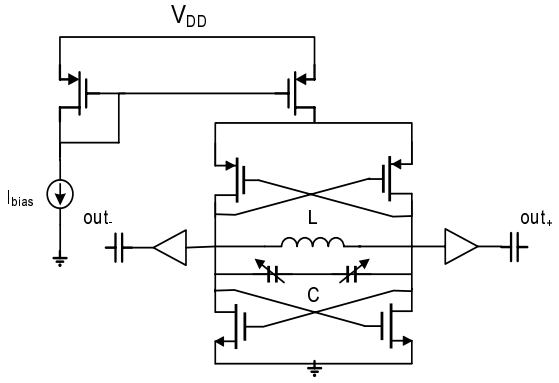

Fig. 6. Schematic of the 900MHz LC-VCO

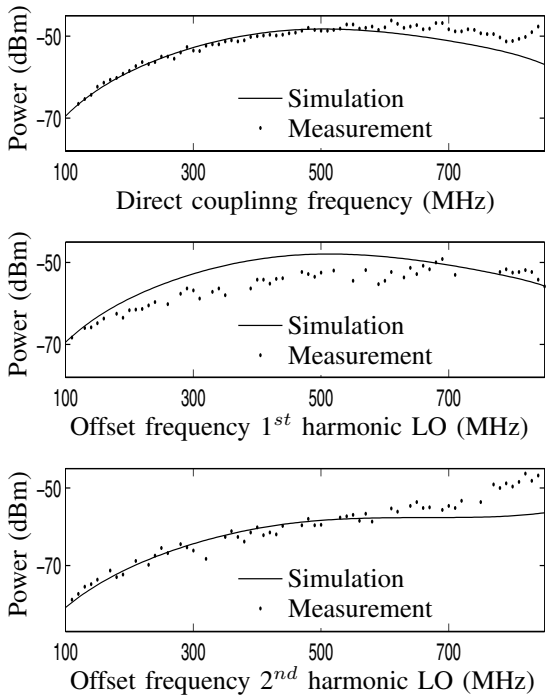

Fig. 7. The power of the direct coupled spur, left sideband spur of the first and second harmonic are measured with a spectrum analyzer for a tuning voltage of 0.9V.

B. Experimental validation of the simulation methodology

The VCO is mounted on a PCB. A large sinusoidal signal is injected into the substrate through a dedicated substrate contact. The size of the substrate contact is 10μm by 20μm. The established power on the RF source is 10dBm to guarantee enough measurement accuracy. The reflection coefficient of the substrate contact is -2.2dB at 100MHz. To avoid reflections in the cables of the bias lines, bias tees are used where the RF side of the bias tee is connected to 50Ω.

The power of all spurs (the direct coupled spur and the spurs resulting from mixing of the injected signal with the first and second harmonic of the LO) are measured with the spectrum analyzer (HP8565E). The frequency of the injected signal is varied from 1MHz up to LO frequency while the tuning voltage is varied from 0V up to 1.8V.

In order to validate the coupling mechanism of substrate noise described in Section 3 the bias lines are not decoupled on PCB.

Figure 7 shows good agreement between the measured spurs and simulation. The mean error between measurements and simulations is less than 3dB.

Figure 8 shows that in the region where FM modulation is dominant (below 10MHz) spurs left and right of the LO have the same amplitude. In the transition region from 10MHz to 100MHz the spurs do not have the same amplitude. The dominant impact mechanism moves from FM to AM modulation. Above 100MHz, where AM modulation is dominant, the spurs have the same amplitude. Since a spectral measurement does not reveal any phase information, a dedicate measurement was setup. It is know that the power of the spurious tones of an FM modulated signal, limited by a limiting amplifier, remains unchanged because the spurious tones are caused by variations of the zero-crossings at the output of the VCO. The output of the VCO is measured with an oscilloscope (TDS784C). In a first experiment the measured output of the LC-VCO is Fourier transformed using MATLAB® [9]. In a second experiment the measured output is first limited before the Fourier transformation. Comparison of both spectra shows that the impact mechanism is FM modulation from DC up to 10MHz.

A dedicated measurement was setup to show that above 100MHz the substrate noise impact is determined by the impedance of the bonding wire connected to the shield. Different PCBs with different contact resistances of the bonding wires were measured in order to show the influence of this resistance on the impact of substrate noise. The resistance of the bonding wires was measured with DC probes. DC probes were placed on unused ground bonding pads close to the bonded ground pad. A DC current is injected into the non-ideal ground. It is assumed that most of the current will flow through the bonding wire. The DC resistance of one PCB is 6.6 times larger than for the other PCB. The transfer function from the injected signal to the direct coupled spur at the output of the VCO is measured

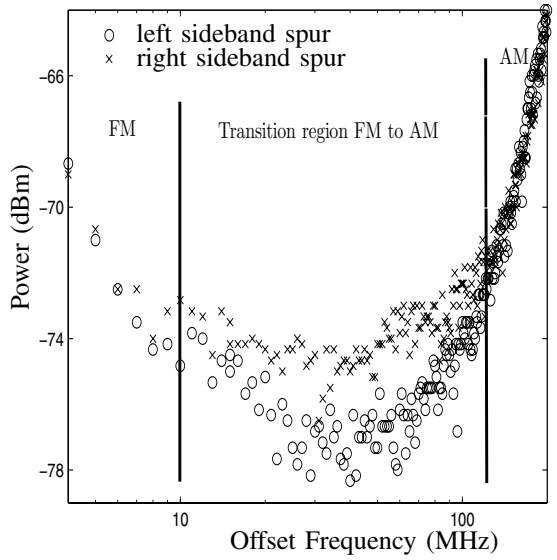

Fig. 8. Measured left and right spur

with a network analyzer (HP8753ES). The injected power is 10dBm. Measurements with different injected power levels shows that the transfer function is independent of the injected power level. The device under test is calibrated up to the connectors of the PCB. Figure 9 shows that PCB with the larger DC resistance of the bonding wire shows as predicted by simulations a higher impact of 6dB average.

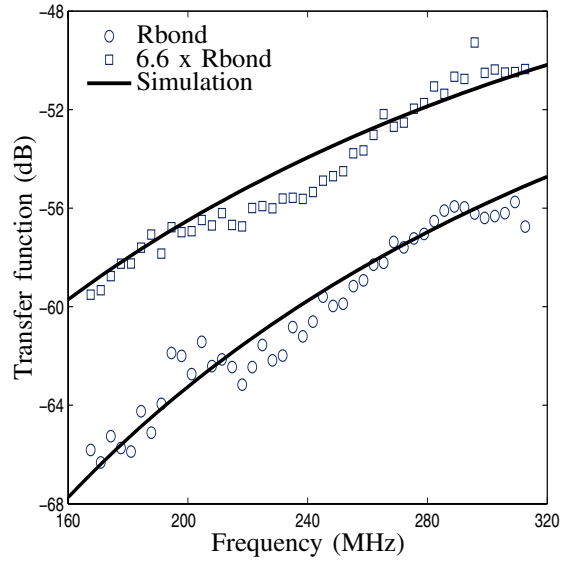

Fig. 9. The impedance of the bonding wire and also the on-chip ground resistance plays a major role in the substrate noise impact mechanism

V. Influence of PCB decoupling capacitors on substrate noise impact

As bias lines on PCB are usually decoupled to avoid ripple on the supply lines, an experiment was setup where the 100μF, 100nF and 100pF are gradually mounted on PCB. This section describes the influence of the PCB decoupling capacitors on the impact of substrate noise.

As shows in figure 10, adding the 100μF decoupling capacitors, gives a resonance frequency at 480MHz. As the 100μF decoupling capacitor is behaving like an inductor above 100kHz, the 1.2nH parasitic inductance together with the inductance of the PCB track and the bonding wire is resonating with the 19pF on-chip decoupling capacitor. Adding the 100nF decoupling capacitors, together with the 100μF capacitors elevates the resonance frequency up to 580MHz. This frequency shift is due to the parallel circuit of the parasitic inductances of the 100μF and 100nF decoupling capacitors. The 100pF decoupling capacitors have almost no influence on the substrate noise impact. The impedance of the 100nF decoupling capacitor is lower then the impedance of the 100pF in the frequency region up to 700MHz.

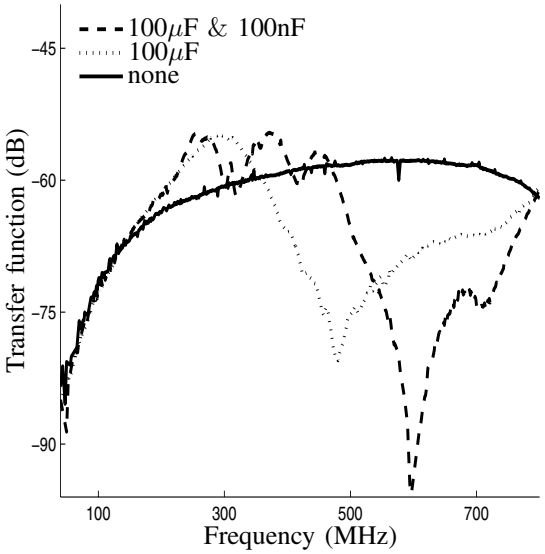

Fig. 10. Off-chip decoupling capacitors have a huge influence on the substrate noise impact on LC-VCO's

The accurate modeling of the PCB and the decoupling capacitor resulted in an accurate estimate of the transmission zero of the transfer function (Figure 11).

VI. Conclusion

This paper report a simulation methodology for the analysis and prediction of substrate noise impact on LC-VCO's from DC up to the LO frequency. The simulation methodology takes into account the substrate, on- and off-chip interconnects, shield of the inductor, bonding wires and PCB components.

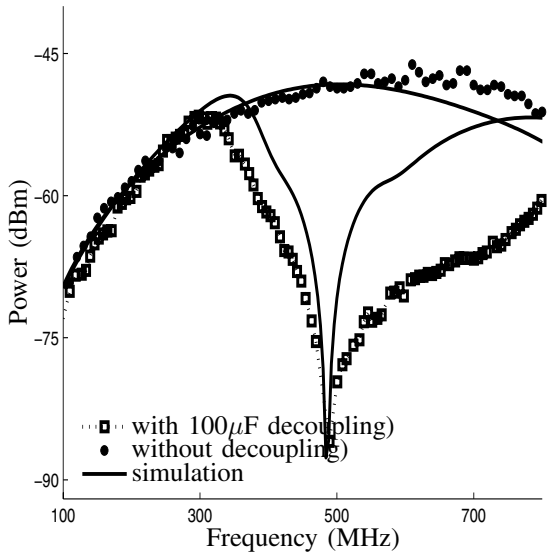

Fig. 11. Simulation versus measurement with and without decoupling of 100μF

This methodology allows to reveal the impact mechanism of substrate noise impact by simulations. The simulation model is validated with measurements from DC up to 900MHz on a 900MHz LC-VCO designed in a 0.18μm 1P6M high-ohmic CMOS technology. This paper points the influence of PCB components on the substrate noise impact on LC-VCO's.

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