A New Asymmetric SRAM Cell to Reduce Soft Errors and Leakage Power in FPGA

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***Abstract*— Soft errors in semiconductor memories occur due to charged particle strikes at the cell nodes. In this paper, we present a new asymmetric memory cell to increase the soft error tolerance of SRAM. At the same time, this cell can be used at the reduced supply voltage to decrease the leakage power without significantly increasing the soft error rate of SRAM. A major use of this cell is in the configuration memory of FPGA. The cell is designed using a 70nm process technology and verified using Spice simulations. Soft error tolerance results are presented and compared with standard SRAM cell and an existing increased soft error tolerance cell. Simulation results show that our cell has lowest soft error rate at the various supply voltages.**

I. Introduction

Soft errors in CMOS circuits occur due to charged particle strikes which are present as cosmic rays in the atmosphere and α-particles within the chip itself [1], [2], [3], [4], [5]. Soft errors in modern VLSI circuits are a major reliability concern. In past technologies, this problem was limited to radiation hostile environments like in space. However, with very-deep-sub-micron (VDSM) technologies, aggressive device size and power supply reductions have impacted severely circuit sensitivity, as they reduced aggressively the critical charge of memory cells. Thus, low energy particles can flip memory cells, making memories more sensitive to atmospheric neutrons as well as to alpha particles. Soft errors are today a concern even at the ground level, at least for those applications where reliability is an important attribute.

Motivation: SRAM-based Field Programmable Gate Arrays (FPGA) give the flexibility of on-site reconfiguration which is highly desirable in the space applications. The device reconfiguration is achieved by setting the bits of the configuration memory of the FPGA. An undesired reconfiguration can occur when a charged particle strike flips the configuration memory cell(s). This undesired reconfiguration can cause the functional error in the device as well as permanent device failure.

Modern FPGAs provide a large number of Configurable Logic Blocks (CLB) and routing resources. As shown in [6], more than 80% of transistors in a FPGA are used for the routing resources. It was observed in [6], [7] that routing resources contain more than 50% of SRAM cells which are sensitive to the charge particles strike and from 78% to 85% of the configuration bits are used for routing [8]. A flip due to a particle strike on a SRAM cell used to control the routing switch(s) which can result in a device failure and functional error. A device failure will occur if a cell flip turns ON the switch which connects logic one signal (V_{dd}) with logic zero signal (Gnd). A functional error will occur if a cell flip turns OFF the switch which disconnects the active signal path. The Soft Error Rate (SER) of a devices is the failure rate of the device due to the charged particle strikes. The SER of a FPGA can be dramatically decreased if the SRAM cells used in the routing networks are protected.

It was observed in [9] that the configuration bit-stream of FPGA contains 87% zeros across different designs. The main reason for higher number of zeros would be due to unused large number of the routing bits. The higher number of zeros enable us to use asymmetric memory cells. An asymmetric cell is a hardened cell which is difficult to flip due to a particle strike either from 0 to 1 or from 1 to 0.

The focus of this paper is to develop a hardened SRAM cell to use for the routing bits of a FPGA. This new cell has very low SER as compared to standard SRAM cell and other hardened cells and at the same time the SER of the cell stays almost same when the supply voltage is reduced to decrease the leakage power of the SRAM/FPGA. We develop a hard-0 cell which is difficult to flip form 0 to 1 due to the particle strike. Our new cell combines the features of SRAM and DRAM cells. It is a modified SRAM cell where a PMOS transistor is used on the feedback line which is controlled by a refreshing signal. Once the data is written to the cell, the pass transistor is turned OFF using the refreshing signal and only momentarily turned ON to maintain the charge stored at the cell nodes. Failure in Time (FIT) is a useful measure which is defined as one failure in a billion hours. To the best of our knowledge this is the only SRAM cell which has refreshing signal and gives advantage of 0 FIT for 0 to 1 flip even at reduced supply voltage.

Related work: An asymmetric cell was developed in [10] to reduce the leakage power in cache memories. This cell design was based on using different threshold voltage of the cell transistors. An approach was proposed in [9] to reduce soft errors in the configuration memory of FPGA. Their technique uses asymmetric cell developed in [10]. A

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technique to reduce the feedback effects of the cell using resistors was proposed in [11]. Using resistors on the feedback lines increases the critical charge of the cell with the penalty of reduced data access time. An approach for reducing the feedback effects of the cell using transistors was discussed in [12]. Using the approach can reduce the SER of the memory whereas our approach is to completely eliminate the SER due 0 to 1 or 1 to 0 flips. The impact of technology scaling on soft error tolerance in CMOS SRAM was discussed in [13].

This paper is divided into following sections. Section II discusses mechanism of soft errors in SRAM cell. Section III describes the design of our new asymmetric cell. In section IV, we analyze the soft error tolerance of our new cell and compare it with standard SRAM cell and asymmetric cell used in [9]. Section V discusses the usage of our cell in the configuration SRAM of FPGAs. We conclude in section VI.

II. Background

A Single Event Upset (SEU) in the SRAM cell occurs when a charged particle strikes at the sensitive node and flips the state of the SRAM cell. These charged particles are present in the space environment as cosmic rays and also within the chip as α-particles. With advanced silicon technologies, SEUs can also be created at ground level by secondary particles created during the interaction of atmospheric neutrons with die materials. The α-particles are emitted due to the radioactive decay of uranium and thorium impurities present in the chip materials and interconnects. SEUs in the memory cause logic error as they change the logic value stored in the cell by flipping it from 1 to 0 or 0 to 1. The is temporary i.e. the cell is not permanently damaged and it can be rewritten in the next memory write cycle.

Every memory cell has two sensitive nodes, the drain of the OFF-NMOS transistor and drain of the of the OFF-PMOS transistor. The drain and substrate of the OFF-transistor create a reverse-biased junction. The reverse-biased junctions of the cell are most sensitive nodes to the particle strike. Immediately followed by the particle strike, charges generation and collection occur. Electrons and holes are generated when the particle passes through the depletion region formed between the drain and substrate of the OFF-transistor. The generated charges are collected at the opposite voltage terminals of the reverse-biased junction i.e. electrons move towards positive voltage and holes move towards negative voltage. The movements of charges cause a current pulse at the struck node. The memory cell flips when the collected charge, Q, is more than the charge stored at the struck node. The minimum charge required to flip the cell is called Q_{crit}. The Q_{crit} not only depends on the collected charge but also on the shape of the current pulse. The current pulse is represented by an equivalent current source between the drain and the substrate of the transistor [14], [15], [16], [17].

A 1 to 0 flip occurs when a particle strike discharges the charge stored at the drain of the OFF-NMOS transistor, and similarly, a 0 to 1 flip occurs when a particle strikes at the drain of the OFF-PMOS transistor. As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C_{node} \times V_{dd}$ making SRAM more prone to soft errors.

Soft Errors in SRAM-based FPGA - SRAM based FPGA contains the configuration memory. The bits of this memory sets the function in the Look-up tables (LUT), connect logic blocks using routing signals, sets clock and control signals. An upset in the configuration memory can modify the function of the LUT or disconnects two logic block etc. Turning OFF the routing switch will only result in functional errors but turning ON can result in the device failure if it connects logic 1 (0) to logic 0 (1) [18].

III. A New Asymmetric SRAM Cell

A standard 6-transistor SRAM cell consists of two inverters and two pass transistors. A feedback loop is formed by connecting the output of the one inverter to the input of the other inverter and vice-versa. This feedback loop helps to maintain the charge stored at the inverter nodes. Two pass transistors are used to read and write the information to the inverter nodes.

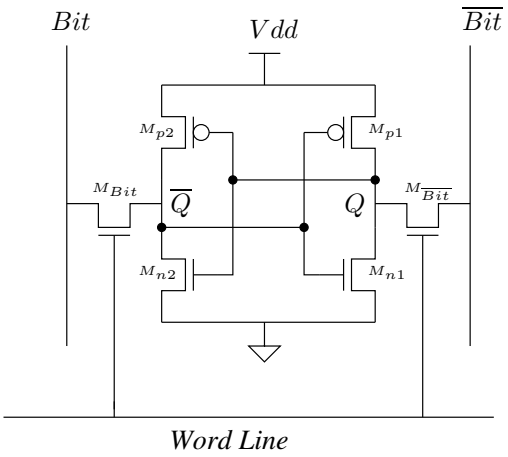

Fig. 1. Standard 6-transistor SRAM Cell.

Figure 1 shows a standard 6-transistor SRAM cell. Nodes Q and $\overline{Q}$ stores the information in the cell. If the charge collected due to a particle strike at a node is more than the charge stored at the node then the cell flips. For example, when Q is storing logic 1 and the particle strike discharges it, it turns on transistor M_{p2} and turns off M_{n2}. When M_{p2} is turned on, it pulls the logic at $\overline{Q}$ to logic 1 which turns on M_{n1} and turns off M_{p1}. The node Q flips state from logic 1 to 0 and $\overline{Q}$ flips from 0 to 1.

If the feedback line is disconnected then the cell will not flip its state instead the particle strike will only generate a glitch at

the struck node. This glitch will disappear immediately after a particle strike and node will restore its original state. Our idea to develop a radiation hardening cell is by eliminating the feedback effect using a pass transistor which is controlled by a refreshing signal. After the data is written to the cell its feedback line is disconnected by turning off the pass transistor. Nodes of the cell keeps logic values due to the charge stored in the node capacitance. As the charge decays with time a refreshing signal is used to turn on the pass transistor momentarily to recharge the node capacitance.

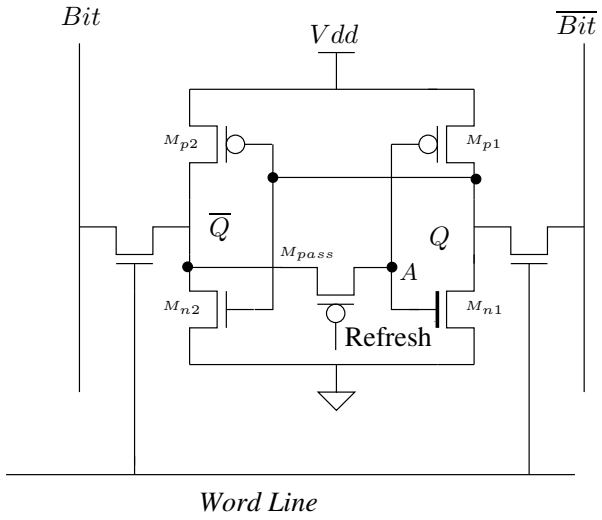

Fig. 2. A New Asymmetric SRAM Cell.

Figure 2 shows a new asymmetric memory cell developed for radiation hardening. This cell is hard-0 cell, meaning, most of the time it can't be flipped when this cell is storing logic 0. A PMOS transistor, M_{pass}, is inserted on the feedback line which connects node $\overline{Q}$ and A. The gate of M_{pass} is connected to a refreshing signal. The refreshing signal is only turned ON (i.e. goes low to turn on M_{pass}) in two cases: a) when the new data is being written to the cell, b) momentarily to maintain charge stored at the cell nodes (i.e. to refresh the cell nodes). The refreshing rate of nodes depends on the circuit design which concerns the nodes parasitic capacitance, V_{dd} and nodes leakage current. The PMOS transistor, M_{pass}, will not transfer logic zero from node $\overline{Q}$ to A instead the minimum voltage at node A will be Vdd-V_{tp}, where V_{tp} is the threshold voltage of M_{pass}. This can cause transistor M_{n1} not to completely turn OFF, consequently increasing the power dissipation of the cell. However, transistor M_{n1} can be completely turned OFF by increasing its threshold voltage even if it gate voltage is not 0V. The charge generated by the particle strike can be collected by nodes Q and $\overline{Q}$ while the cell is storing logic 0. In this case Q is storing logic 0 and $\overline{Q}$ and A are storing logic 1 and A will not collect charge as its drain and substrate are at the same voltage.

There may be an issue with with the node connected to the pass transistor that stays in high impedance state when the refreshing signal is OFF and it is vulnerable to the particle strike or to noise. It happens only when the data stored in the cell is logic 1. Firstly, this has a small impact on an FPGA cell because most of the time (i.e. 87%) it will be storing logic 0. Secondly, the capacitance at this node can be increased by techniques like presented in [19]. A particle strike has following effects on these nodes:

1) When the particle strikes at node Q, it produces a glitch because the gates of transistors M_{p1} and M_{n1}, (i.e., node A) stays steady since the feedback is disconnected by M_{pass}.
2) When the particle strikes at node $\overline{Q}$, it again produces a glitch because the gates of transistors M_{p2} and M_{n2} stays steady as the feedback is disconnected by M_{pass}.
3) Node A is not sensitive for 1 to 0 flip because PMOS transistor (drain of M_{pass} is only sensitive for 0 to 1 flip.

Overall the cell can't be flipped while storing zero and the transistor M_{pass} is OFF.

Figure 3 shows the flip of the standard SRAM cell. In this case, a particle strike flips nodes Q and $\overline{Q}$ whereas Figure 4 shows a particle strike only produces glitch. The glitch disappears and a cell restores its original value.

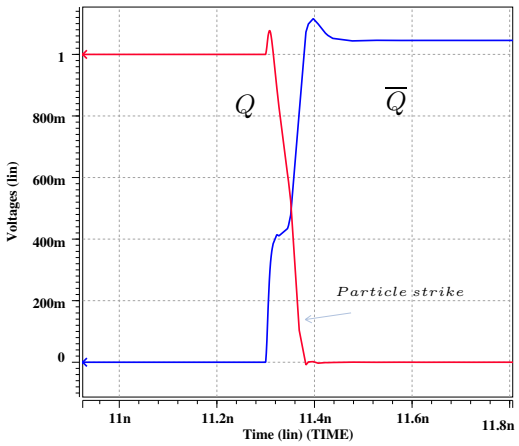

Fig. 3. A particle strike results in the flip of standard SRAM cell.

Similarly, when a cell is storing logic 1 the particle strike generated charge can be collected at all the three nodes but node Q can't be flipped. In this case node Q is storing 1 and nodes $\overline{Q}$ and A are storing 0. A particle strike has the following effects on these nodes:

1) A particle strike at node Q can't flip the cell instead it will generate a glitch.
2) A particle strike at node $\overline{Q}$ can only flip the cell if collected charge is sufficient to turn on M_{pass} transistor and increase the voltage level at A so the transistor M_{n1} turns on.
3) A particle strikes at node A can flip the cell if the collected charge is more than the charge stored at it.

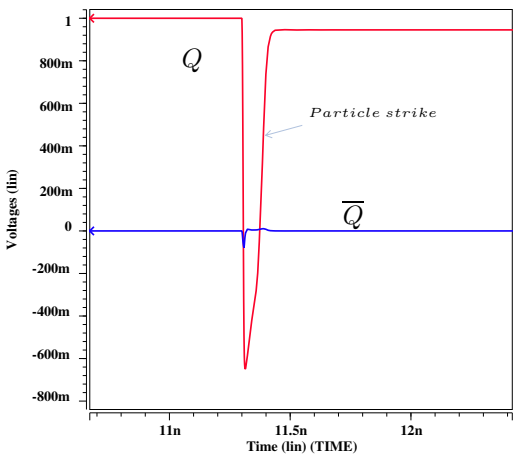

Fig. 4. A particle strike results in a glitch (not flip) in case of our new asymmetric SRAM cell.

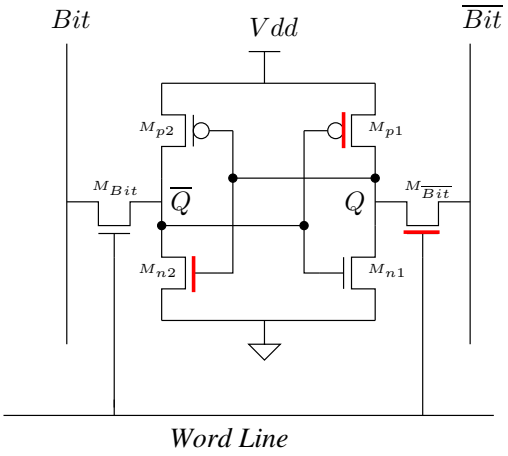

Fig. 5. Asymmetric cell used in [9] to increase soft error tolerance.

This node is very vulnerable to the particle strike as it is in high impedance state.

The routing bits of a FPGA are not required to change unless a reconfiguration is performed. It enables us to use refreshing signal which doesn't need to turn ON frequently to access the cell which otherwise would be in the case of data SRAM.

IV. Results

Q_{crit} of a cell is the minimum charge collected due to a particle strike which results in the cell flip. We designed three cells to determine and compare Q_{crit}. These three cells are: standard 6-transistor SRAM, asymmetric SRAM (ASRAM0) [9], and our new asymmetric cell RSRAM0 (Refreshing SRAM). Both cells, ASRAM0 and RSRAM0, are hard-0 cells. These cells were designed in 70nm process technology. The power supply voltage for this technology was used as 1.0v and Spice parameters were obtained from [20], [21]. The layout design rules were scaled to this technology according to MOSIS layout rules for 0.18μm technology.

For the comparisons purposes, we used transistor dimensions similar to given in [9]. Figure 5 shows ASRAM0 cell used in [9]. Thick lines at the gate of transistors M_{p1}, M_{n2}, and $M_{\overline{Bit}}$ represents changed threshold voltages (please refer [9] for more details). We used λ = 0.035μm for 70nm process technology. The length of every transistor in three cells (see Figure 1, Figure 2, and Figure 5) is used as 2λ. The width of access transistors, transistors M_{Bit} and $M_{\overline{Bit}}$, is considered as 21λ. The width of remaining transistors are as M_{p1} = M_{p2} = 35λ and M_{n1} = M_{n2} = 65λ. The threshold voltages of transistors of ASRAM0 are considered similar to provided in [9].

In Spice simulations of CMOS circuits, a particle strike is modeled by injecting a current pulse at the sensitive node. This pulse has rapid rise time and gradual fall time. The shape of the pulse can be approximated by the following equation described in [22].

$$I(t) = \frac{2Q}{\sqrt{\pi}} \times \sqrt{\frac{t}{T}} \times e^{\frac{-t}{T}} \quad (1)$$

Where Q is the charge collected due to the particle strike and T is the process technology constant. We used T = 16ps for 70nm as discussed in [23]. In order to determine Q_{crit} of a cell node, we performed Spice simulations by injecting current pulses of equation (1) for various values of Q, between the drain and substrate of the OFF transistor. The minimum values of Q which results in the cell flip is considered as Q_{crit} of that node. Table I shows the Q_{crit} of every node of three cells for different types of flips i.e when its storing 0 and 1. The first column shows cell node names, the second column shows type of flip at the node. A node can have either 1 to 0 flip or 0 to 1 flip. Third, fourth, and fifth columns show Q_{crit} of nodes of three different cells. The Q_{crit} of ASRAM0 for 0 to 1 flip at node Q and 1 to 0 flip at node $\overline{Q}$ is higher than regular SRAM. The Q_{crit} of node Q for 0 to 1 flip of our cell, RSRAM0, is ∞. In this case, the particle strike at Q only generates a glitch and the cell restores its original value. The Q_{crit} node $\overline{Q}$ for 1 to 0 flip is also ∞. Node A is not present in SRAM and ASRAM0 cells so Q_{crit} for node A is not applicable (NA). Node A is not applicable for flip (NAF) when it is storing logic 1. Thus, RSRAM0 can't be flipped by a particle strike if it is storing 0 and refreshing signal is OFF.

The failure rate of a cell due to particle strikes also known as Soft Error Rate (SER) decreases exponentially with increasing Q_{crit} of cell nodes. The units of SER are Failure in Time (FIT). One FIT is one failure in one billion hours. Equation 2 is generally used to calculate the FIT of a memory cell.

$$SER \propto N_{flux} \times A_{node} \times exp^{\frac{-Q_{crit}}{Q_s}} \quad (2)$$

where N_{flux} is the intensity of the Neutron flux, A_{node} is the area the node and Q_s is the charge collection efficiency. We used Q_s = 12fC [9]. Table II show comparisons of FIT

Node	Flip	Q_{crit} (fC)		
		SRAM	ASRAM0	RSRAM0
Q	0→1	57	72	∞
$\overline{Q}$	1→0	23	28	∞
A	1→0	NA	NA	NAF
Q	1→0	23	15	∞
$\overline{Q}$	0→1	57	37	110
A	0→1	NA	NA	5

TABLE I

COMPARISONS OF Q_{crit} FOR THREE DIFFERENT TYPES OF MEMORY CELLS

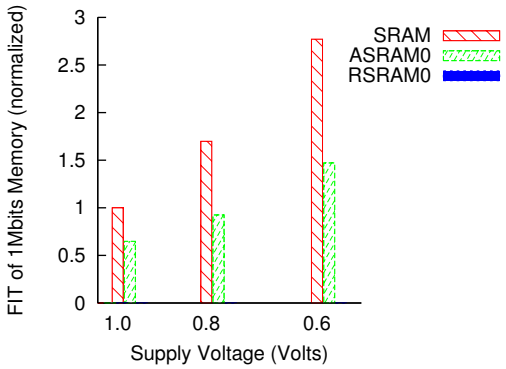

Fig. 6. FIT versus supply voltage scaling for 1 Mbits of memory using three different cells while storing 0. In this case RSRAM0 has 0 FIT for all the supply voltages

of one Mbits memory using three different types of cells while storing 0 and storing 1. The FIT of memory using RSRAM0 cell is 0 while all the cell of memory are storing 0 because it can't have 0 to 1 flip and for the same case the FIT of memory using ASRAM0 cell is much less than regular memory, SRAM. The FIT of ASRAM0 while storing 1 is the highest. The FIT of our cell, RSRAM0, is lower than SRAM in every case i.e. while storing 0 and 1.

	SRAM	ASRAM0	RSRAM0
Storing 0	1000	648.4	0
Storing 1	1000	2053	851.2

TABLE II

FIT OF ONE MBITS MEMORY USING THREE DIFFERENT TYPES OF CELLS

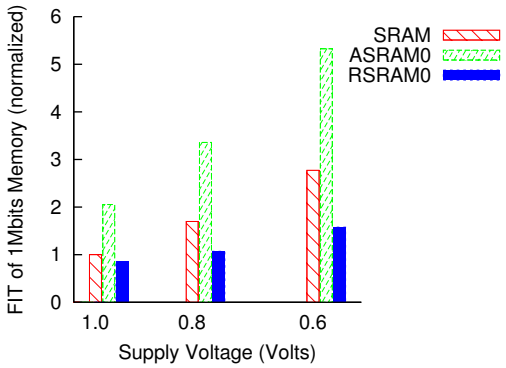

Fig. 7. FIT versus supply voltage scaling for 1 Mbits of memory using three different cells while storing 1.

Dynamic voltage scaling schemes are very popular to reduce the power dissipation by the memory [24]. However, by reducing the supply voltage (V_{dd}) increases the FIT rate of the memory. We have performed Spice analysis to calculate FIT of these cells for different supply voltages. The y-axis of Figure 6 shows the FIT of 1 Mbit memory while storing 0 using regular SRAM cell, ASRAM0, and RSRAM0 for three different values of V_{dd}. Note that FIT for RSRAM0 is not shown in this figure because it has 0 FIT. FIT values on the y-axis are normalized with respect to SRAM at 1.0V. The FIT of SRAM and ASRAM0 increases dramatically as compared to RSRAM0. Similarly, Figure 7 shows FIT of 1 Mbit memory while storing 1. Again in all cases, the memory using RSRAM0 cell yields lowest FIT. From Spice simulation, we found the refreshing rate of RSRAM0 less than 1 MHz with asymmetric duty cycle, meaning, the Ref signal of RSRAM0 is only turned ON for 1ns and remains OFF for rest of the cycle.

V. DISCUSSION

The idea of proposing new asymmetric cell to use in the configuration SRAM of FPGAs is to avoid electrical conflicts caused by radiation induced 0 to 1 flip in the cell. The 0 to 1 flip can in some cases lead to device destruction (a cell flip connecting two signals with different electrical states). At the same time this cell can be used at the reduced supply voltage to decrease the leakage power without significantly increase the FIT rate of the memory. However, reducing the supply voltage results in increasing FIT rate of normal memory cell. As shown in Figure 6 the FIT rate of the standard SRAM increases three times at 0.6V supply voltage compare to at 1.0V. In case of our cell for 0 to 1 flip, the FIT rate is 0 for various supply voltages. Figure 8 shows decreasing the supply voltage results in dramatic reduction in the leakage power of our cell. The y-axis shows normalized leakage power at 1.0V V_{dd}. Similarly, for 1 to 0 flip, our cell has less FIT than normal SRAM at various supply voltages.

Our proposed new cell is completely hardened for 0 to 1 flip. Other proposed schemes in literature only reduce the FIT of the cell [9], [11], [10] whereas our proposed cell has 0 FIT for 0 to 1 flip and much less FIT than standard SRAM cell for 1 to 0 flip. We remark that node A of our new cell is in high impedance state when transistor M_{pass} is OFF. However, node A will not collect charge generated by a particle strike when it is at logic 1 i.e. there can't be 1 to 0 flip at node A. The desired state of node A is logic 1 for our 0 to 1 hardened

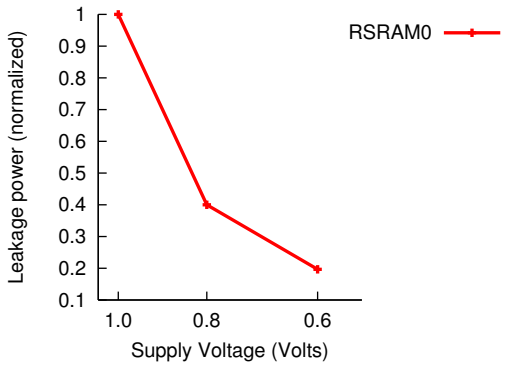

Fig. 8. Reduction in the leakage power with scaling down the supply voltage.

cell thus eliminating the high impedance state vulnerability. In case of node A at high impedance logic 0 state, the critical charge of A is still high as threshold voltage of transistor M_{n1} is increased. Moreover, increasing the threshold voltage of M_{n1} reduces the leakage current through it, consequently decreasing the leakage power of the cell.

We have performed Spice based analysis for the stability of the cell. We found it working for various supply voltages and temperatures. The pass transistor M_{pass} on the feedback line acts as resistor when it is ON which can increase the data write time to the cell. However, SRAM used for the routing bits is only written at the time of reconfiguration (not frequently) thus increasing the data write time will have insignificant affect on the performance of the FPGA.

Using M_{pass} and refreshing signal in our cell will increase the area overhead. For a minimum size cell the expected area overhead is less than 15% in terms of unit transistors. The refreshing signal can be generated on-chip by using available on-chip clock signal in modern FPGAs. The routing of the refreshing signal can be parallel to the bit-lines.

Using our cell for the configuration SRAM of FPGA will result in much lower FIT and leakage power than standard SRAM cell which is not doable with other existing schemes.

VI. Conclusion

We proposed a new asymmetric cell to increase the soft error tolerance of SRAM used in the configuration of FPGA. Our new cell has advantage of using at decreased supply voltage to reduce the leakage power without significantly increasing the FIT rate of configuration memory of FPGAs. The cell can be designed to be hard-0, difficult to flip from 0 to 1 or hard-1, difficult to flip from 1 to 0. Spice simulation results show that our new cell has 0 failure rate for 0 to 1 flip and lowest failure rate for 1 to 0 flip as compared to the standard SRAM cell and asymmetric cell, ASRAM0, used in [9]. We verified the functionality and stability of the cell at various supply voltages and temperatures.

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