Statistical simulation of high-frequency bipolar circuits

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Abstract:

This paper describes a physics-based methodology for computationally efficient statistical modeling of high-frequency bipolar transistors along with its practical implementation into a production process design kit. Applications to statistical modeling, circuit simulation, and yield optimization are demonstrated for an opamp circuit. Experimental results are shown that verify the methodology.

1 Introduction

Variations in processing conditions during wafer fabrication cause unavoidable manufacturing tolerances in a production process. The random nature of such tolerances needs to be captured by proper statistical modeling and simulation methods during the design process in order to avoid costly re-spins, considering today's skyrocketing mask cost. For digital circuits with the delay time as critical Figure of Merit (FoM), often fairly simple "worst-case" or "corner" modeling methods can be used to describe process variations. This is not possible though for analog high-frequency (h.f.) circuits in which a *variety* of FoMs, such as bandwidth, noise figure, conversion gain etc., has to be optimized *simultaneously*.

Since corner methods do not need any additional simulator capability and, in addition, little attention has been paid at all to *statistical modeling and simulation of **h.f.*** circuits, most design tools today still do not offer a suitable infrastructure for statistical simulation and modeling of analog h.f. circuits. The resulting issues and consequences have been discussed in [1]. There, various existing methods were compared and a suitable approach, based on physics-based compact modeling, was proposed for solving the problem. Most recently, this approach has been (to a large extent) implemented into a production process design kit (PDK) and has been used for circuit yield optimization.

This paper is organized as follows. Chapter 2 gives an overview on the statistical modeling and simulation approach. Chapter 3 describes the relation between compact model parameters and statistical fab data. Chapter 4 shows selected statistical modeling results for the process employed which are the basis for the statistical circuit simulation. Then, in Chapter 5 an opamp circuit is used as demonstration vehicle for simulation-based yield optimization.

2 Statistical modeling methodology

The goal of statistical modeling and simulation is to "predict" *circuit* performance parameters (and yield) prior to production based on the variation of *manufacturing conditions*, such as implant dose, anneal temperature, oxide growth etc.. The statistical variations of the latter are generally not available in contrast to statistical electrical measurements on special so-called process control monitor (PCM) structures. Hence, PCM data are used as input for statistical modeling and simulation.

PCM measurements can be related by simple equations to *PCM parameters*, $\boldsymbol{p}$[1)], such as sheet and contact resistances as well as capacitances per unit area or length. Compared to compact model parameters, $\boldsymbol{m}$, PCM parameters are less correlated. However, for practical purposes their correlation is still too large - at least for transistors - so that they need to be transformed to technology parameters (TPs), $\boldsymbol{t}$, such as average doping concentration and region widths. In a physics-based compact model such as HICUM/L2 [2] the model parameters can be directly expressed as function of $\boldsymbol{t}$ (and partially also $\boldsymbol{p}$). More details of this transformation are described in Section 3.

The basic methodology of a physics-based statistical modeling and simulation strategy is sketched in Fig. 1. Parameter extraction is performed once at the beginning of process development for "typical" devices, resulting in the model parameter vector $\mathbf{m}_T$. Once sufficient PCM data are available, $\mathbf{m}_T$ is shifted to the nominal parameter vector $\mathbf{m}_N$ by employing the properties of a physics-based compact model (cf. Section 3). In contrast to this predictive mode, which is based on a single shift vector $\Delta\mathbf{p} = \mathbf{p}_N - \mathbf{p}_T$ and its conversion to a specific $\Delta\mathbf{t}$, statistical simulation requires random vectors $\mathbf{t}$, from which then randomly skewed sets $\boldsymbol{m}^*$ are calculated. This is accomplished by transforming the variance of the measured PCMs, σ_p^2, to the variance of the TPs, σ_t^2, which determines the random variation of $\mathbf{t}$. In Fig. 1 a Design of Experiment (DoE) set-up combined with a Response Surface Method (RSM) [3] is shown at the center of the statistical simulation procedure in order to significantly reduce the computational effort in contrast to the often used Monte-Carlo (MC) method.

Fig. 1 indicates on the right the boundary between the responsibility of the foundry (for providing the appropriate statistical model information) and of the PDK set-up (for providing the proper statistical simulation capability). Obviously, the calculation of skewed model parameters as a function of random TP vectors needs to be integrated in the design system. This decouples modeling from design tasks and also, in contrast to corner models, enables circuit designers to perform "true" statistical simulations tailored toward the FoMs of each circuit specifically. Presently, all available design systems lack this capability due to missing "statistical" model equations. Two options exist to realize the desired feature. The most simple approach is to integrate TRADICA [4] with its already existing complete set of statistical model equations as a module into the design system. A corresponding prototype has already been created in cooperation with Cadence [5]. The other option is to code the physics-based statistical model equations in a simulator-specific description language (or possibly in Verilog-A). Since

1) Bold-faced letters indicate vectors.

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this task is quite elaborate (including testing and considering the large variety of contact configurations for bipolar transistors), and since it also reveals modeling and fab IP to potential competitors (for further discussion of the drawbacks of this approach see [1]), a different approach was pursued in this paper.

TRADICA uses physical geometry-independent parameters (such as sheet resistances, area and perimeter specific capacitances) and design rules to generate compact model parameters for a given layout. For bipolar transistors, the emitter dimensions and contact arrangement are variables. The above mentioned physical and process related input data also enable an efficient generation of statistical models. Using TRADICA, a polynomial representation $\mathbf{m}(\mathbf{t})$ was generated from the existing physics-based statistical model equations, the available nominal model parameters, and information on σ_t. This and related possible issues are discussed in more detail in Section 3.

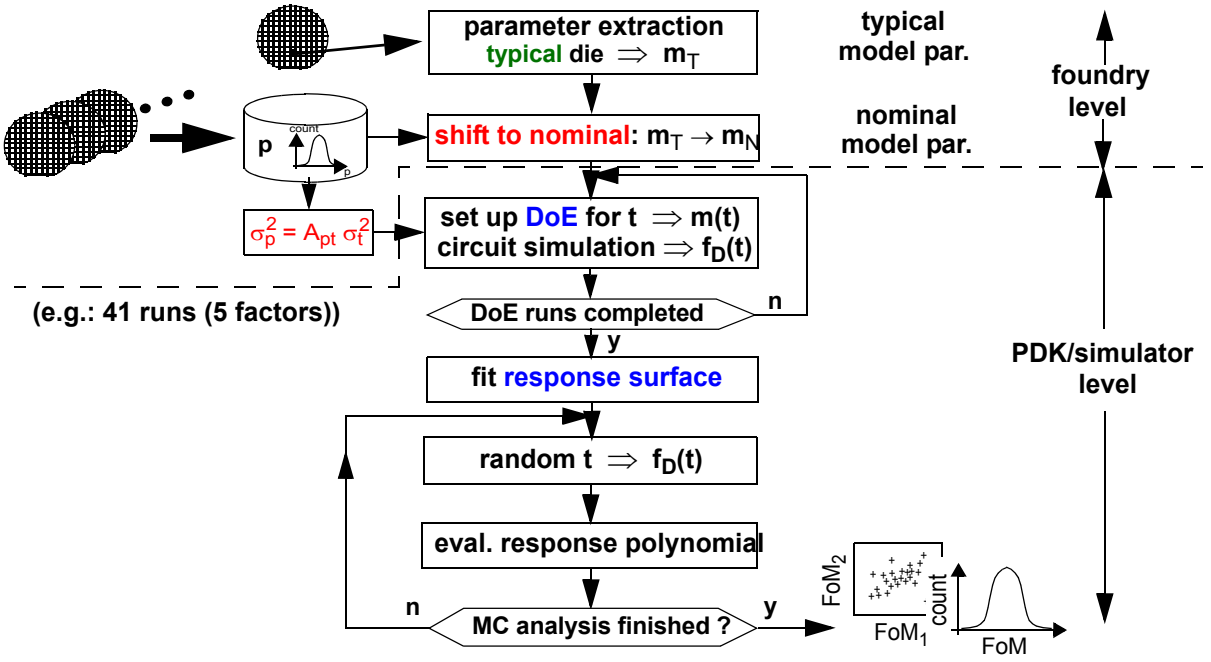

Fig. 1: PCM and compact model based statistical modeling and simulation flow (schematic).

3 Relation between compact models and PCMs

The model parameter set ***m*** of physics-based geometry-scalable compact models depends naturally on layout dimensions, ***d***, and technology specific electrical parameters, ***s***. The latter contain already many PCM parameters ***p*** as a subset and additionally, e.g., specific parameters associated with the selected compact model. As a consequence, certain model parameters are directly given by elements of ***p***, as for instance the zero-bias internal base resistance,

$$r_{Bi0} = r_{SBi0} g_i \,, \qquad (1)$$

with r_{SBi0} as zero-bias sheet resistance and g_i as a geometry function that depends on emitter width b_{E0} and length l_{E0} [6][6].

However, parameters describing, e.g., currents, minority charge and a variety of other effects associated mainly with the intrinsic transistor action often depend not directly on ***p***, but only implicitly through nonlinear relations on ***t*** (such as doping concentration, mole fraction or region thickness, and independent layout dimensions). This dependence is also the cause for the correlation between model parameters. Hence, it is necessary to develop equations relating ***m*** and ***p*** to ***t***. Since ***p*** and its variation $\Delta\boldsymbol{p}$ are known from in-line PCM measurements, the TPs have to be obtained from ***p***. For statistical simulation it is sufficient to just relate TP *variations* $\Delta\boldsymbol{t}$ to $\Delta\boldsymbol{p}$. Table 1 gives an overview on the dependence between ***p*** and ***t***. The Table also reveals that the PCM parameters are not uncorrelated.

p ↓ \ ***t*** →	N_{Bi}	w_B	N_{Ci}	w_C
$\overline{C}_{jEi0}$	xxx	-	-	-
r_{SBi0}	xxx	xx	x	-
$\overline{C}_{jCi0}$	(x)	-	xxx	-
$\overline{C}_{jC,PT}$	-	-	-	xxx

Table 1: Correlation table showing the dependence of TPs on PCM parameters for the *intrinsic* transistor (with a conventional BE doping profile); it is assumed that $\overline{C}_{jCi0}$ is not determined by collector punch-through. The number of crosses indicates the correlation intensity between a PCM parameter and a TP. (Geometry dependence will cause additional correlation.)

Generally, it is preferred to express the changes of ***t*** as ratios *r* of skewed to nominal value, since absolute TP values are usually unavailable. For instance,

$$r_{NBi} = \frac{N_{Bi}^*}{N_{Bi}} = \frac{N_{Bi} + \Delta N_{Bi}}{N_{Bi}} \qquad (2)$$

is the ratio of the changed (index '*') to the nominal base doping concentration. Similar definitions hold for the internal collector doping concentration (r_{NCi}) and width (r_{wC}) as well as for the base width (r_{wB}). The $\Delta\boldsymbol{p}$ variables can also be defined as relative deviations (with normalized standard deviations as input).

In summary, the generation of a complete set of skewed model parameters, ***m****, from measured $\Delta\boldsymbol{p}$ and a given nominal set ***m***

consists of three steps: First, calculate $\Delta\boldsymbol{t}$ from measured $\Delta\boldsymbol{p}$, then $\Delta\boldsymbol{s}$ and $\Delta\boldsymbol{d}$ from ($\Delta\boldsymbol{p}$,$\Delta\boldsymbol{t}$), and finally $\Delta\boldsymbol{m}$ from ($\Delta\boldsymbol{s}$,$\Delta\boldsymbol{d}$,$\Delta\boldsymbol{p}$). The equations for the last step are already available for geometry scalable models (e.g. [4]) and will not be discussed further here. The equations for the first two calculation steps are illustrated below, using HICUM/L2 [2] as a vehicle.

An educational example is the dependence of $\boldsymbol{m}$ on TPs such as base doping N_{Bi} and width w_B. HICUM parameters that depend on these TPs are, e.g., those of the internal BE depletion capacitance (C_{jEi0}, V_{DEi}), the transfer saturation current (I_S), the zero-bias hole charge (Q_{p0}), and the low-current transit time (τ_0). Their skewed values influence characteristics such as the collector current and transit frequency. First, physics-based relations are established for the ratio of the skewed to nominal internal base sheet resistance and area specific internal BE depletion capacitance, respectively:

$$\frac{r^*_{SBi0}}{r_{SBi0}} \cong \frac{1}{r_{NBi}^{1\angle a_{\mu pB}} r_{wB}}, \tag{3}$$

$$\frac{\overline{C}^*_{jEi0}}{\overline{C}_{jEi0}} = r_{NBi}^{1/z_{Ei}} \left(\frac{V^*_{DEi}}{V_{DEi}}\right)^{\angle 1/z_{Ei}}, \tag{4}$$

$$V^*_{DEi} = V_{DEi} + k_D\left[V_T\left(1\angle\frac{a_{vni}}{2}\right)\ln(r_{NBi})\right]. \tag{5}$$

Here, $a_{\mu pB}$, a_{vni}, k_D are parameters that are related to the doping dependence of the mobility and bandgap, using expressions typically found in device simulators (e.g. [8]) and evaluated in doping regions of interest; z_{Ei} is the nominal depletion capacitance grading coefficient.

Using above equations the two unknown TPs r_{NBi} and r_{wB} can be calculated iteratively from the two PCM ratios

$$\frac{r^*_{SBi0}}{r_{SBi0}} = 1 + \delta r_{SBi0}, \tag{6}$$

$$\frac{\overline{C}^*_{jEi0}}{\overline{C}_{jEi0}} = 1 + \delta c_{jEi0}. \tag{7}$$

Here, the δr_{SBi0} and δc_{jEi0} are the actually measured relative change of the skewed internal base sheet resistance and area specific internal BE depletion capacitance. Once the TPs are known, including the emitter width ratio r_{bE} (assuming a sufficiently long transistor for this example), the correlated model parameters can be calculated as

$$\frac{I^*_S}{I_S} = \frac{r_{\mu nB} r_{NBi}^{(a_{vni}\angle 1)}}{r_{wB}} r_{bE}, \tag{8}$$

$$Q^*_{p0}/Q_{p0} \cong r_{NBi} r_{wB} r_{bE}, \tag{9}$$

$$\frac{\tau^*_{0,b}}{\tau_{0,b}} \approx \frac{r^2_{wB}}{r_{\mu nB}}. \tag{10}$$

The latter is only the *base* portion of the low-current transit time, and $r_{\mu nB}$ ($=\mu_{nB}(N^*_{Bi})/\mu_{nB}(N_{Bi})$) is calculated directly from suitable approximations of the standard mobility expression. In a similar way, parameters that depend on the internal collector doping are calculated once the doping change has been determined from the PCM of the collector-base depletion capacitance. For instance, transit time parameter ratios read [7]

$$\frac{\tau^*_{Bfvl}}{\tau_{Bfvl}} = \frac{r_{wB} r_{wCi}}{r_{\mu nCi}\sqrt{(V^*_{DCi}/V_{DCi}) r_{NCi}}}, \quad \frac{\tau^*_{pCS}}{\tau_{pCS}} = \frac{r^2_{wCi}}{r_{\mu nCi}}. \tag{11}$$

Above equations clearly show the model parameter correlations (even without geometry dependence), and also the often nonlinear dependence on $\boldsymbol{t}$ (and $\boldsymbol{p}$). Other skewed HICUM parameters can be expressed in a similar form, using the TPs listed in Table 1. For the specific electrical parameters of the external transistor mostly simple direct relations are valid which complete the desired skewed model parameter set $\boldsymbol{m}^*$.

Fig. 2 visualizes the impact of the correlations for the peak transit frequency $f_{T,peak}$ of a bipolar transistor. The distribution on the left-hand-side results from a statistical variation of separate single HICUM model parameters (listed on top of the figure). If the correlation is taken into account, the result on the right-hand-side is obtained, which has been verified through device simulation.

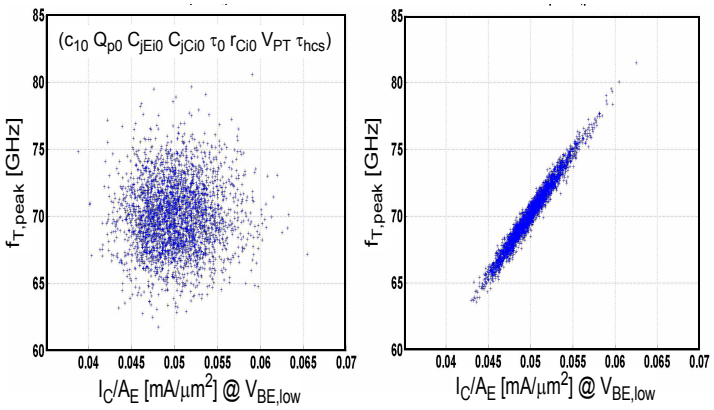

Fig. 2: Comparison between MC model parameter variation (left) and MC TP variation including correlation (right) for peak f_T.

The discussion so far was based on a $\Delta\boldsymbol{p}$ vector that is measured on a particular die, from which the corresponding $\Delta\boldsymbol{t}$ vector (and $\boldsymbol{m}^*$) can be calculated. In order to enable statistical simulation, the measured $\Delta\boldsymbol{p}$ vector would be required for each die, which is practically unfeasible. In this case, $\Delta\boldsymbol{p}$ represents the vector of standard deviations, i.e. $\Delta\boldsymbol{p} = \sigma_p$. Hence, the task is to determine the TP standard deviation vector σ_t from σ_p. Assuming that the tolerance ranges for statistical modeling are fairly small, the "propagation of variances" approach can be used, which results in a linear equation system relating the PCM variances to the TP variances,

$$\sigma^2_p = A_{pt}\sigma^2_t. \tag{12}$$

The elements of the matrix A_{pt} correspond to the square of the derivatives of the PCMs with respect to the TPs. These derivatives are taken at the nominal values, using the analytical equations (e.g. (3), (4)) presented earlier. This method is also referred to as backward propagation of variances (BPV) [9], where it was applied for the d.c. case only and with $\Delta\boldsymbol{p}$ (instead of $\Delta\boldsymbol{t}$) as basic variable calculated from the variance of measured *electrical* parameters.

Once σ_t is known, statistical model parameters can be generated. As mentioned before, a quick ***first-order approach*** was implemented into the design system in which the nonlinear relation $\Delta\boldsymbol{m}(\Delta\boldsymbol{t})$ is approximated by simple 2nd-order polynomials that are generated by TRADICA. Fig. 3 shows an example of a statistical model card for HICUM/L2. The variables b_e0 and

l_e0 are the nominal emitter width and length, respectively; r_xxx_l and a_xxx_l are the *local* relative and absolute variation, respectively, of a TP and are used for simulating matching; r_xxx and a_xxx are the total relative and absolute variation, respectively, consisting of the corresponding global and local variation. The model parameters then equal their nominal value plus a sum of deviations calculated from the total variation of each TP. In order to minimize the number of terms TRADICA automatically drops insignificant contributions. Based on a complete process-scalable parameter set for HICUM/L2, TRADICA can generate similar model cards also for the SPICE Gummel-Poon model and the new HICUM/L0 model [10][11].

From the previously discussed relations $\Delta m(\Delta t)$ it is obvious that this approach has accuracy limitations for larger process variations since a polynomial cannot represent all relations accurately enough in case of significant nonlinearity.

```
* Tr A  AE0=1*0.30*2.0(1); NB=2; NC=1(SIDE), lv; T=300;
* HICUM/Level2    v2.2                      TRADICA B5.2
.SUBCKT N030201S02_01   c   b   e   s
parameters
 + b_e0 =0.300E-06  l_e0 =0.200E-05
 + r_nbei_l = r_nbei_rm_lv*r_nbei_sm_lv/sqrt(b_e0*l_e0)
 + r_nbei   = r_nbei_g_lv+r_nbei_l
 + r_nci_l = r_nci_rm_lv*r_nci_sm_lv/sqrt(b_e0*l_e0)
 + r_nci    = r_nci_g_lv+r_nci_l
 + a_be0_l = a_be0_rm_lv*a_be0_sm_lv/sqrt(l_e0)
 + a_be0    = a_be0_g_lv+a_be0_l
 + a_wc_l = a_wc_rm_lv*a_wc_sm_lv/sqrt(b_e0*l_e0)
 + a_wc     = a_wc_g_lv+a_wc_l
 + a_le0_l = a_le0_rm_lv*a_le0_sm_lv/sqrt(b_e0)
 + a_le0    = a_le0_g_lv+a_le0_l
 :
Q     c   b   e   s  MOD
.model MOD  NPN level=9  TNOM= 26.85  version=2.2
 + c10   = 6.544E-33
           + 2.148E-33*r_nbei + 6.506E-27*a_le0
           + 3.811E-26*a_be0 + 5.547E-20*a_be0*a_be0
 + qp0   = 8.449E-15
           + 8.449E-15*r_nbei + 2.460E-08*a_be0
           + 4.200E-09*a_le0
 + cjei0 = 2.464E-15
           + 1.190E-15*r_nbei + 7.175E-09*a_be0
           + 1.225E-09*a_le0
 :
 + t0 = 6.523E-12
        - 1.546E-12*r_nci + 1.065E-12*r_nci*r_nci
        - 6.394E-06* a_be0
 :
 + rci0 = 3.754E+02
          - 3.380E+02*r_nci + 3.413E+02*r_nci*r_nci
          - 5.965E+08* a_be0 + 3.474E+08* a_wc
          - 5.252E+14* a_wc * a_wc -  1.563E+08* a_le0
 :
 + rbi0 = 1.282E+02
          - 8.519E+01*r_nbei + 7.095E+01*r_nbei*r_nbei
          + 3.259E+08*a_be0 - 5.568E+07*a_le0
```

Fig. 3: Excerpt of a statistical model card for HICUM/L2 generated by TRADICA.

4 Statistical models: experimental results

The methodology described above has been applied first to a silicon bipolar production process targeted towards high-speed industrial and consumer applications. Process features include complementary NPN and vertical PNP (VPNP) BJTs with peak transit frequencies of 33 GHz and 17 GHz for the NPN, and 12 GHz for the VPNP.

Information on process variations was obtained from PCM data. Table 2 contains a list of the most relevant bipolar transistor related PCM structures [1]. According to the last column usually only a single data point per measurement is taken. Statistical data for I_C *and* I_B provide information on variations of b_{E0} [9]. Statistical S-parameter measurements were made for transistor TNHS.

Name	Structure	PCM data / parameter
TWHV	wide high-voltage trans.: multi-finger with largest allowed emitter window width b_{E0} (or large area transistor)	$I_{x,I,HV} = I_x(V_{BE}>0)$, x={C, BE} $C_{jEi0,HV} = C_{jEi}(V_{BE}=0)$ $C_{jCi0,HV} = C_{jCi}(V_{BC}=0)$ $C_{jCPT,HV} = C_{jC}(V_{BC}>V_{PT})$ $C_{jSb0} = C_{jS}(V_{SC}=0)$
TNHS	narrow high-speed trans. with $b_{E0}=b_{E0,min}<< l_{E0}$ a) multi-finger for CV b) standard layout for S parameters	$I_{x,HS} = I_x(V_{BE}>0)$, x={C, BE} $C_{jE0,HS} = C_{jE}(V_{BE}=0)$ $C_{jC0,HS} = C_{jC}(V_{BC}=0)$
RBI	transistor tetrode [12] [13] with standard b_{E0}	$r_{SBi0} = r_{SBi}(V_{BE}=V_{BC}=0)$
RBLNK	"tetrode" with $b_{E0} = 0$	r_{Sl} , r_x
RCOL	3-contact chain, 2:1 ratio	r_{Sbl} , r_{Cc}
RBCON	3-contact chain, 2:1 ratio	r_{Bc} , r_{Ssil},

Table 2: Most important bipolar transistor PCMs and related data or parameters. Some structures can be used for other devices, too. Currents are measured at V_{BC} = 0V. RBLNK, RBCON, RCOL indicate base link, base contact and external collector resistance related structures.

Before applying the statistical modeling methodology to circuit design, the parameters for modeling the statistical variations (i.e. the coefficients in front of the TPs in Fig. 3) have to be extracted, and the resulting complete statistical models have to be verified. The method employed here is to mimic the PCM measurement conditions as close as possible by performing a *statistical simulation* of the PCM measurements using the models with the same size as the PCM structures and the same bias conditions. Furthermore, the same data reduction was applied before comparing the simulated distributions to the measured ones.

Figs. 4 and Fig. 5 show as examples comparisons of PCM measurements and corresponding simulations of the large area base-emitter depletion capacitance (corresponds to $C_{jEi0,HV}$ in Table 2) and the base-emitter offset voltage of a VPNP pair. In these results outlying data points were removed from the measurements. In spite of this filtering process there were still nearly 10k usable device measurements. More results can be found in [14].

All simulations have been done using HICUM/L2 in SPECTRE. Note that in Fig. 4 simulated capacitances have been corrected to take into account the parasitic capacitance of the parametric test system, since this capacitance is not included in the model parameter set. This correction leads to the correct mean value, but has no impact on the shape of the distribution. The latter, as can be observed in Fig. 4, is not Gaussian but has to be approximated by a Gaussian due to the assumptions in the modeling methodology in order to make it reasonably simple. As the circuit results later will show, this approximation has little impact in practical applications.

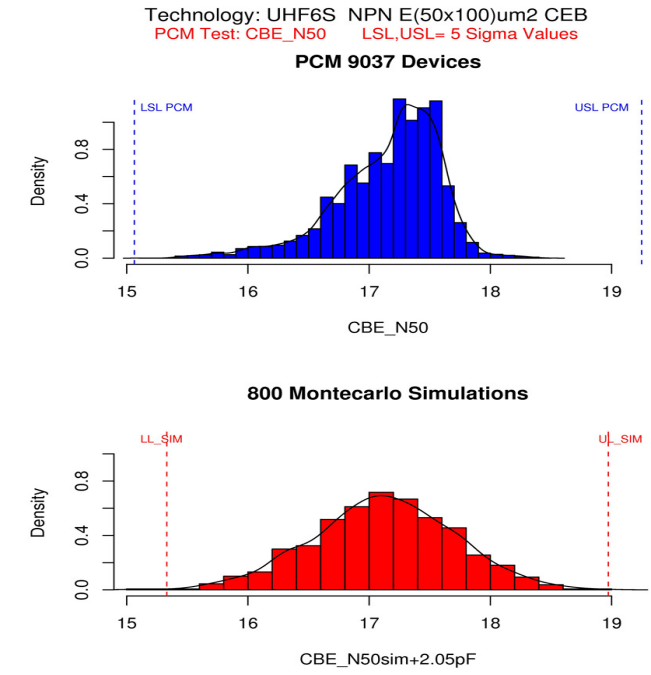

Fig. 4: Normalized frequency of occurrence of the large area NPN zero-bias base emitter capacitance: PCM measurements (top) and simulation results (bottom).

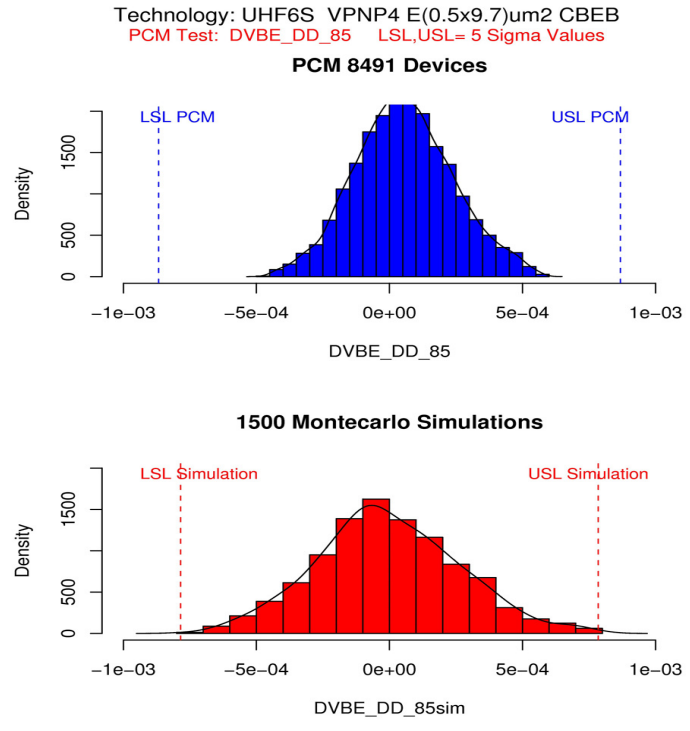

Fig. 5: Frequency of occurrence of the offset voltage of the vertical PNP: PCM measurements (top) and simulation results (bottom).

5 Statistical circuit simulation results

A simple operational amplifier is taken as demonstrator to show the application of statistical models in practical circuit design. The first step was to compare simulation and measurement for an already fabricated amplifier circuit (high gain, multistage structure). Here, the DC offset is evaluated. The measurement results are derived from wafer probing of about 2000 samples, and the corresponding distribution is shown in Fig. 6.

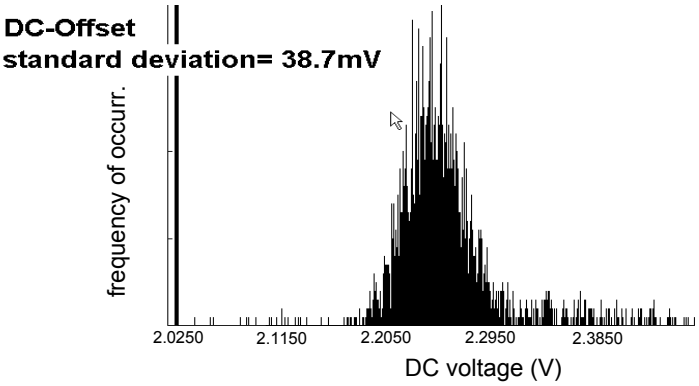

Fig. 6: DC offset distribution from wafer probing.

Next, the circuit was simulated with the verified statistical models. As Fig. 7 demonstrates, the combined process and mismatch analysis is capable of predicting the DC offset with an accuracy of around 20%. Of particular importance is that both measurement and simulation show a non symmetrical distribution with a tail toward higher offsets. As a consequence, the method is regarded as sufficiently reliable for optimizing other circuits with respect to process variability.

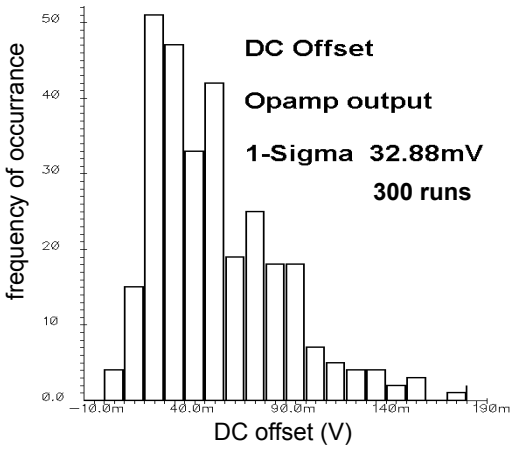

Fig. 7: DC offset distribution from statistical circuit simulation.

An example is shown next for an already existing circuit that had not yet been fabricated. In total, 1000 Monte-Carlo runs with mismatch and process variations were used to obtain an estimate of the DC offset standard deviation. An additional correlation analysis of these data helped to identify those technology parameters that have the highest impact on the DC offset. As it turned out in this example, the doping of the internal base appeared as the most important technology parameter. Fig. 8 visualizes the dependence of the DC offset voltage distribution as a function of the corresponding TP, r_{NBi}.

Based on this knowledge, it is now possible to improve the circuit by adequate measures such as adding base current compensation, cascode stage, and output buffer. Along with adding the related blocks, also a mismatch analysis was performed to optimize the area factor of critical components. The result in Fig. 9 shows a significantly reduced standard deviation.

First experimental verification of the statistical modeling methodology became recently available for an array of transimpedance amplifiers (TIAs) with integrated gain switching. The corresponding results are shown in Table 3.

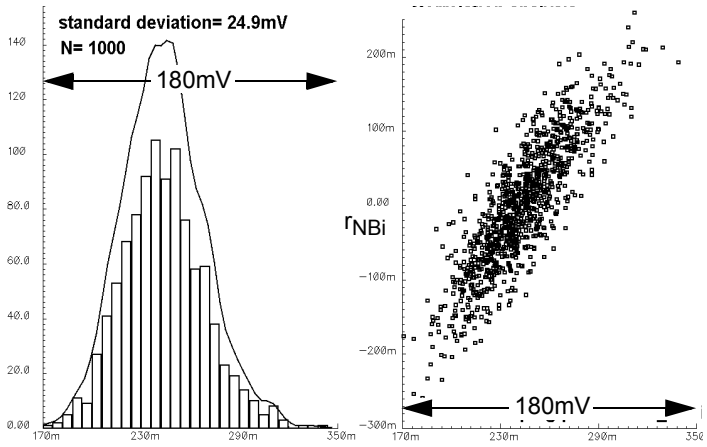

Fig. 8: Result of the Monte-Carlo analysis: DC offset standard deviation and its correlation with base doping (r_{NBi} = r_n_bei in Fig. 3).

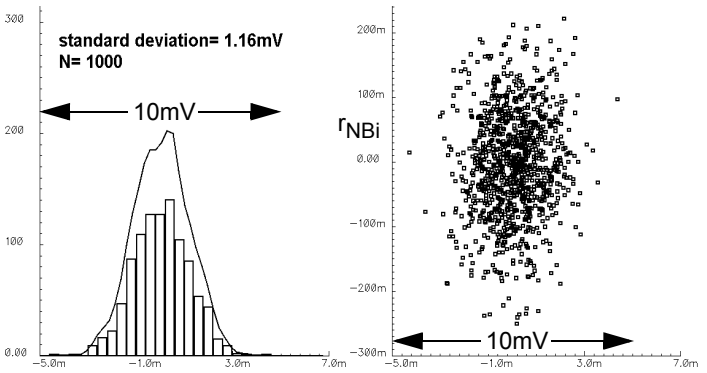

Fig. 9: Monte-Carlo analysis after circuit optimization: the standard deviation of DC offset has dramatically decreased and shows negligible correlation with base doping (r_{NBi}).

rel. gain	sim σ (mV)	meas σ (mV)	diff (mV)
TIA1			
40	15.16	20.59	5.43
13.3	16.82	20.60	3.78
3	19.36	23.90	4.54
1	14.85	14.51	-0.33
TIA2			
160	31.76	37.66	5.90
53.2	35.79	47.26	11.48
12	40.11	54.26	14.15
4	32.90	34.99	2.09

Table 3: DC output variation in test mode. Here the TIAs are biased by an on-chip generated DC current resulting in a nominal output voltage of 500mV at TIA1 and 1000mV at TIA2

6 Conclusions

Simulation-based methods for accurately predicting statistical circuit behavior and yield are becoming increasingly important. In this paper, a *practically feasible* approach for statistical simulation of analog/h.f. circuits is described, that is based on physics-based compact modeling. The approach not only facilitates an extremely fast *prediction* of consistent compact bipolar transistor model parameter sets as a function of process variations, but is also quite accurate as was demonstrated by a comparison to experimental fab data.

The methodology has been implemented in a process design kit. First applications to an Opamp and TIA show good agreement between statistical circuit simulation and measurement of the offset voltage distribution. As a consequence, the method is suited for identifying the main technology parameters responsible for process related circuit parameter spread and for reducing their variance in by circuit design measures, allowing a cost efficient design for yield.

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