Sensitivity Analysis for Fault-analysis and Tolerance in RF Front-end Circuitry

Tejasvi Das and P.R. Mukund
Dept. of Electrical Engineering
Rochester Institute of Technology, Rochester NY 14623
Email: tad4807@rit.edu

Abstract

RFIC reliability is fast becoming a major bottleneck in the yield and performance of modern IC systems, as process complexity and levels of integration continually increase. Due to high frequencies involved, testing these chips is both complicated and expensive. While the areas of Automated testing and Self-test have received significant attention over the past few years, no formal framework of fault-models or sensitivity-models exists in the RF domain. This paper describes a Sensitivity Analysis methodology as a first step towards such a framework. It is applied towards a Low Noise Amplifier, and a case-study application is discussed by using design and experimental results of an adaptive LNA designed in the IBM6RF 0.25 µm CMOS process.

1 Introduction

The rapidly escalating levels of integration in the CMOS IC industry have given rise to significantly complex RF front-ends, tightly integrated with digital, mixed-signal and base band Analog circuitry on a single silicon die. In this nanometer regime, fabrication complexity exponentially increases with every transition to a new technology node, inevitably accompanied by a larger number of process faults, higher process variations and passive tolerances. With higher frequencies of operation, the RF front-end exhibits heightened sensitivity to package parasitics, mutual-coupling, stray inductances, etc. Consequently it is difficult to incorporate these anomalies in the design process since their causes are uncorrelated; these issues continue to increase the gap between simulation models and performance of the RFIC in silicon, resulting in several design iterations, higher test costs and lower yield.

The problem is exacerbated by the fact that in RF circuits, process variations and catastrophic process faults are only part of the list of probable causes for failure or performance degradation. With the drive towards greater levels of integration, many of the passives used in RF circuits are implemented on-chip. The quality factor of these passives is not very predictable and is significantly influenced by slight variations in metal layer thickness, thickness of dielectric between the metal layers etc. Another major factor affecting reliability of RF circuits is the wide tolerance in the package parasitics. These factors will introduce soft faults in the RF circuit by degrading its performance beyond the required specification window. Due to these reasons, RF front-end reliability has become an issue of growing concern.

With testing these RF circuits being both a complicated and expensive exercise [1], self-test of RF circuits has received considerable attention in recent times [2] [3] [4]. The testing domain, however, suffers from a serious lack of availability of formal fault and sensitivity models. The lack of such models lead to sub-optimal test and fault-tolerance solutions: with prior knowledge of the range and extent of performance degradation caused by process variations and faults, test and self-correction algorithms and techniques can be optimized.

This paper describes a Sensitivity analysis methodology for RF front-end circuits and implements it on the popular cascode LNA topology. The analysis maps the impact of process variations and soft-faults on to performance specifications of the circuit. By quantifying these dependencies, performance degradation patterns and ranges are identified. Self-Test solutions can be optimized by focussing on these specific patterns and ranges. The paper also discusses the application of this analysis towards self-calibration methods (we have successfully demonstrated self-calibration of RF circuits in [5] [6]).

The rest of the paper is organized as follows. Section 2 describes the generic methodology of Sensitivity Analysis and Section 3 discusses the implementation of the methodology on a cascode LNA. Section 4 describes the application and results of the Analysis for self-calibration and Section 5 summarizes the work.

2 Methodology for Sensitivity Analysis

The Sensitivity Analysis (hereafter abbreviated to SA) studies the mapping of all circuit parameter variations onto performance specifications of the circuit. This analysis provides a quantitative insight into the performance deviations caused due to process variations and soft faults. The SA further addresses the following issues:

a. Sensitivity of each parameter with respect to each circuit specification
b. Quantified impact and dependence of each parameter with respect to all circuit specifications
c. Quantified deviation from ideal performance specifications for variations and soft-faults in each circuit component

For self-calibration approaches that dynamically sense performance and modify circuit parameters, it provides an early-design framework (described in greater detail in section 4). The analysis is expected to provide inputs to early (pre-simulation) stages of the design cycle, and cannot rely upon several time-intensive simulations – especially since multiple iterations are to be expected, and it is impractical to

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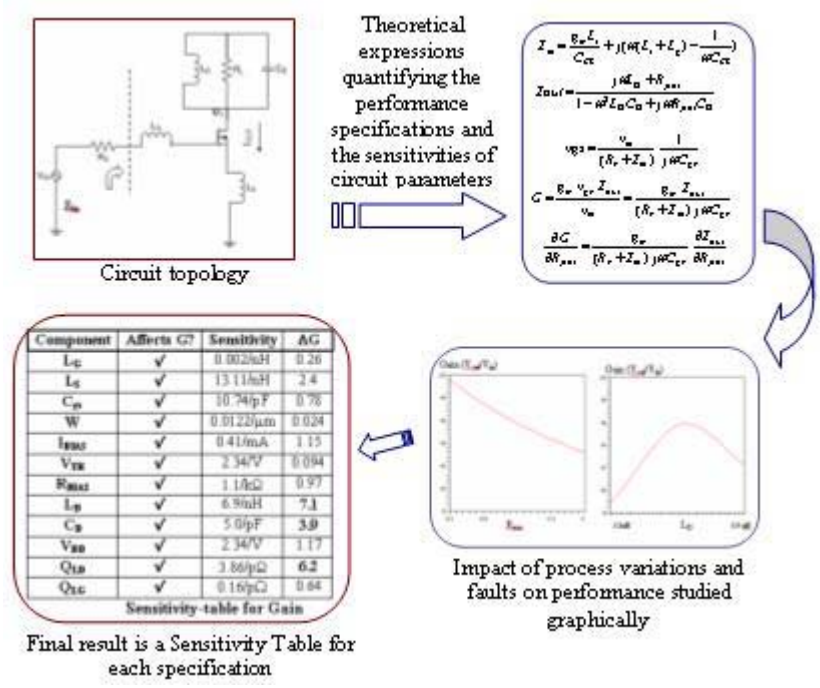


Fig. 1. The Sensitivity Analysis Flow

necessitate simulation cycles for each SA cycle. The ideal solution for such a scenario is to develop a theoretical, 'no-simulation required', generic process (as has been developed for this work) that can be re-used for different designs and iterations, across process technologies and different applications.

This analysis also finds utility as an early-design aid for designs of circuit topologies. It provides the designer with useful insight by quantifying parameter-performance dependencies, trends and trade-offs involved in meeting the application specifications. The process involved in this analysis is shown in Fig. 1. For a given circuit topology, the performance specifications and circuit parameters are identified. The analytical equations governing these specifications are developed, and their sensitivity about their value is computed. For a given design and process, the values of the design components, tolerances and range of maximum deviation are used as inputs, and the degradation in performance specifications are graphically studied (Fig 1(c)). The final result is a Sensitivity Table for each performance specification, as shown in Fig. 1(d). This table identifies all parameters that impact each specification, the sensitivity of the parameter (short-range), and the maximum possible deviation in the specification due to each component (long range). These tables fast to compute and require no simulation support. The math computations use Maple ® software, and the tables lend themselves very easily for multiple iterations – the user has to simply re-input the new design variables and values are re-computed.

3 Sensitivity Analysis for LNA

This section develops sensitivity tables for a LNA. For the numerical analysis, a 1.9 GHz cascode LNA is designed in the IBM6RF 0.25 µm CMOS process, as shown in Fig.2. All tolerance and process variation data have been extracted from the PDK. The analysis is not specific to this design: it can be re-used for any generic design and process.

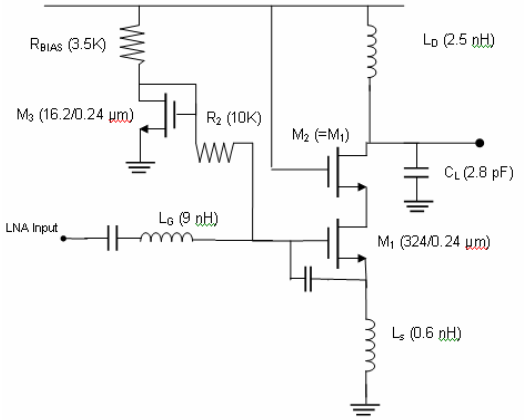


Fig. 2 Cascode LNA used in this work

3.1 Gain

The gain analysis in this section uses voltage gain compared to power gain; the power gain depends on the terminating impedance of the LNA, which is dependent on the circuit/termination that follows the LNA. Since this termination is both application and architecture specific, voltage gain has been considered. With the output load impedance denoted by Z_{out}, we arrive at the following equations:

The input impedance Z_{in} is given by [7]:

$$Z_{in} = \frac{g_m L_s}{C_{GS}} + j\left(\omega(L_s + L_g) - \frac{1}{\omega C_{GS}}\right)$$

The output impedance Z_{out} is given by (assuming the output impedance of M2 can be neglected):

$$Z_{out} = \frac{j\omega L_D + R_{par}}{1 - \omega^2 L_D C_D + j\omega R_{par} C_D}$$

where R_{par} is the series parasitic resistance of L_D.

The gate-source voltage v_{gs} is given by:

$$v_{gs} = \frac{v_{in}}{(R_s + Z_{in})}\left(\frac{1}{j\omega C_{gs}}\right)$$

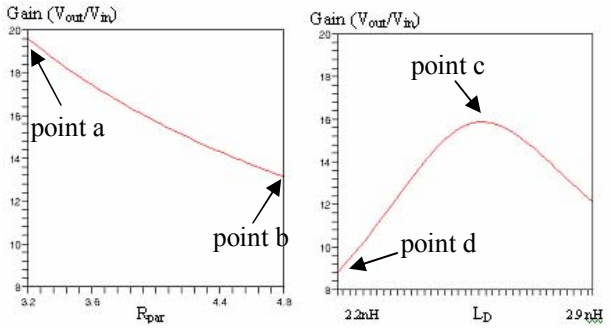
The voltage gain G is given by:

$$G = \frac{g_m v_{gs} Z_{out}}{v_{in}} = \frac{g_m Z_{out}}{(R_s + Z_{in}) j\omega C_{gs}} \quad (1)$$

The short-range sensitivity of G to R_{par} is given by

$$\frac{\partial G}{\partial R_{par}} = \frac{g_m}{(R_s + Z_{in}) j\omega C_{gs}}\left(\frac{\partial Z_{out}}{\partial R_{par}}\right) \quad (2)$$

The sensitivity equations to all other parameters are not mentioned due to space constraints. They can be calculated from the above equations, as shown in Eqn.2. For a tolerance of 30% in inductor value and 25% in Q-factor, the behavior of gain for the 1.9 GHz LNA due to these tolerances is shown in Fig. 3.



(a) **(b)**

Fig. 3 Deviation in Gain of LNA when (a) Q-factor of L_D changes by 25% (due to soft-fault or variation) and (b) when L_D varies by 30%

The graphical representation provides both a qualitative and quantitative insight into the impact of parameter variations on gain. To compute the maximum possible deviation in gain, the following techniques are used:

a. If the sensitivity curve is linear and monotonic, then the maximum deviation is simply given by (sensitivity*tolerance)
b. If the sensitivity curve is non-linear (as in Fig. 3(a)), then the max. deviation is found as the difference in values between point (a) and point (b) in Fig. 3(a).
c. If the sensitivity curve is not monotonic as in Fig. 3(b), then the local minima or the maxima is computed (point c, by evaluating the first partial differential), and the max. deviation is found as the difference in values between point (c) and point (d) in Fig. 3(b)

Following this process for all the parameters for the circuit in Fig 2, the Sensitivity table of Table 1 is computed. The table identifies the major contributors to gain degradation; gain is highly sensitive to the Q-factor of L_D, tolerance in L_D and C_D. Further, it quantifies these sensitivities, and numerically defines the maximum degradation in gain for the given design and process. Since it is a stand-alone process requiring no simulation support, iterations are ultra-fast and simple – the new design values and tolerance/variations are provided as inputs, and the graphs and tables are re-computed and displayed.

Component	Sensitivity	Max. ΔG
L_G	0.002/nH	0.26
L_S	13.11/nH	2.4
C_{gs}	10.74/pF	0.78
W	0.0122/μm	0.146
I_{BIAS}	0.41/mA	1.15
V_{TH}	2.34/V	0.094
R_{BIAS}	1.1/kΩ	0.97
L_D	6.9/nH	**7.1**
C_D	5.0/pF	**3.9**
V_{DD}	2.34/V	1.17
Q_{LD}	3.86/pΩ[1]	**6.2**
Q_{LG}	0.16/pΩ	0.64

Table 1. Sensitivity table for gain

3.2 Input-match frequency

The input match frequency of the LNA is given by [7]:

$$f_{in} = \frac{1}{2\pi\sqrt{(L_G + L_S)C_{gs}}} \quad \text{, where} \quad C_{gs} = \frac{2}{3}.W.L.C_{ox}$$

The input match frequency is dependent on L_G, L_S, C_{gs}, and W/L of the input transistor. For the 1.9 GHz LNA used in this work, variation of f_{in} for variation in these component values is shown in Fig.4. The sensitivity of L_G to S_{11} frequency (f_{in}) is given by:

$$\frac{\partial f_{in}}{\partial L_G} = -\frac{C_{gs}}{4\pi[(L_G + L_S)C_{gs}]^{3/2}}$$

and for the design values of the LNA, this equates to 9.902E16, or 0.099 GHz/nH. The total possible deviation in S_{11} frequency due to variations in L_G (ΔL_G is the tolerance of the gate coil is given by (since it is linear and monotonic):

$$\frac{\partial f_{in}}{\partial L_G} * \Delta L_G = 9.902E16 * 2.7nH = 0.27GHz$$

Following a similar process for L_G, C_{GS} and W, the sensitivity-table of S_{11} frequency (Table 2) is constructed. The deviation for all cases is monotonic and almost linear. It is also clearly seen that the deviation is greatest for variations in L_G. Further, since L_G has little or no impact on other specifications (as is seen in the following sections). All the equations have not been explicitly listed in this paper due to their complexity. They can, however, be readily derived from the equations mentioned in this paper.

[1] parasitic ohm

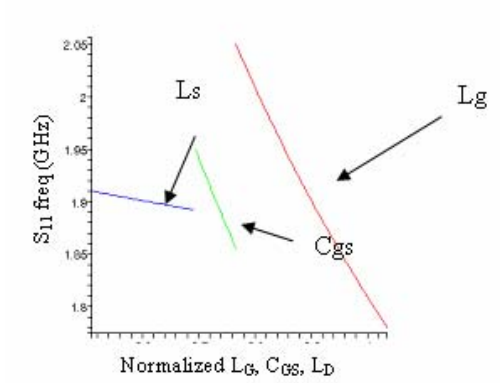


Fig. 4 Variation in S_{11} frequency (in GHz) for L_S, L_G and C_{GS} tolerances

Components	Sensitivity	Δ freq (GHz)
L_G	0.99/nH	**0.27**
L_S	0.1/nH	0.018
C_{GS}	1.3/pF	0.095
W	0.005/μm	0.06

Table 2 Sensitivity-table for S_{11} frequency

The actual variation considered for each component is based on the tolerances and variations specified by the technology process being used. For example, the variation/tolerance of a bond-wire is much higher (up to 40%) compared to an on-chip coil (up to 30%). Hence the variation considered for the gate coil will depend on the choice of coil used.

3.3 Input Impedance

The magnitude of input impedance Z_{IN} is given by:

$$|Z_{IN}| = \sqrt{\left(\frac{g_m L_S}{C_{gs}}\right)^2 + \left(\omega(L_S + L_G) - \frac{1}{\omega C_{gs}}\right)^2}$$

The sensitivity of L_S on input impedance is given by:

$$\frac{\partial|Z_{IN}|}{\partial L_S} = \frac{\frac{2{g_m}^2 L_S}{{C_{gs}}^2} + 2\left(\omega(L_S + L_G) - \frac{1}{\omega . C_{gs}}\right)\omega}{2.\sqrt{\left(\frac{g_m L_S}{C_{gs}}\right)^2 + \left(\omega(L_S + L_G) - \frac{1}{\omega C_{gs}}\right)^2}}$$

and for the design values used, it is evaluated at 8.335E10 (ohms per henry). Following a similar procedure for all other dependent components (as discussed in the previous sections), we arrive at Table 3.

Components	Sensitivity	Δ Z_{11} (Ω)
L_G	0.358/nH	2.6
L_S	83/nH	**14.9**
C_{gs}	69.5/pF	5.1
W	0.077/μm	0.924
I_{BIAS}	2.6/mA	7.28
V_{TH}	14.9/V	0.6
R_{BIAS}	7.1/kΩ	**6.25**
V_{DD}	14.9/V	**7.45**
Q_{LG}	1/pΩ	4

Table 3 Sensitivity-table for input-impedance of LNA

3.4 Noise Figure

The Noise Factor (NF) is given by [7]:

$$NF = 1 + \frac{\omega_0 \gamma g_{d0}(1 - 2c\chi_d + (4Q^2 + 1)\chi_d{}^2)}{2.\omega_t g_{m.} Q}$$

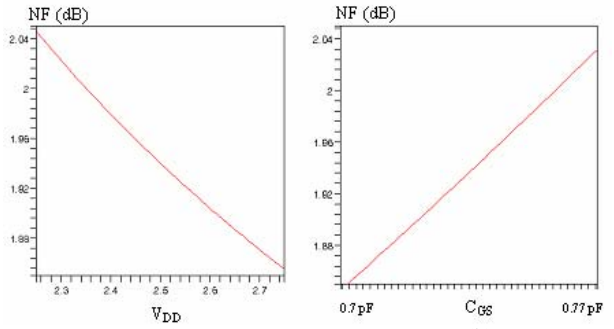
where $\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}}$, $\omega_t = \frac{g_m}{C_{gs}}$

$Q = \frac{\sqrt{L_g + L_s}}{2R_s\sqrt{C_{gs}}}$ and $\chi_d = \frac{g_m}{g_{d0}}\sqrt{\frac{\delta}{5\gamma}}$

g_{d0} is the device transconductance when the drain-source voltage is zero, i.e, in the triode region of operation. It is modeled as

$$g_{d0} = K\frac{W}{L}(V_{gs} - V_{th})$$

where K is a constant extracted from simulation. γ is the empirically derived excess noise factor, and its value ranges between 2-3 for short-channel processes, and δ is typically valued at 2γ. c is the correlation factor between the transistor gate and drain noise. Using the above equations, the sensitivity of each component is evaluated as before and tabulated in Table 3.4. The nominal noise figure value for this design was 1.94 dB.



(a) (b)

Fig. 5 Impact on NF when (a) V_{DD} is varied by +/-10% and (b) C_{GS} is varied by 10%

Fig. 5 shows the degradation on NF for two parameters that NF is most sensitive to: V_{DD} and C_{GS}. Similar to previous sections, table 4 is generated.

Component	Sensitivity	ΔNF(dB)
L_G	0.001/nH	0.017
L_S	0.5/nH	0.09
C_{gs}	2.5/pF	**0.18**
W	0.004/μm	0.048
I_{BIAS}	0.066/mA	**0.185**
V_{TH}	0.38/V	0.015
R_{BIAS}	0.18/kΩ	**0.16**
V_{DD}	0.38/V	**0.19**
Q_{LG}	0.006/pΩ	0.024

Table 4. Sensitivity table for Noise Figure

The analysis identifies that the parameters most sensitive to NF are C_{GS}, V_{DD} and bias current. In the particular design case, NF suffers by almost 10% for a 20% variation in bias current of supply voltage.

3.5 Linearity

Intercept-point and 1-dB compression point are the two accepted metrics to quantify linearity of RF circuits. This section discusses the sensitivity of the input-referred intercept point (IIP3) of the third harmonic for the cascode LNA. The IIP is quantified by the three-point method [7], as it is computationally more efficient compared to the power-series expansion method [9]. In this method, there is no necessity of computing double and triple derivatives in this approach. IIP3 is thus given by:

$$\text{IIP3} = \frac{4V^2}{Q^2 R_S}\left(\frac{g_m(0)}{g_m(V)+g_m(-V)-2g_m(0)}\right)$$

where $g_m(F)$ is a function of the input amplitude[2], R_S is the source resistance, V is a DC bias increment, and Q is the input stage Q-factor given by:

$$Q = \frac{1}{(R_S + |Z_{in}|)\omega C_{gs}}$$ .The transconductance $\left(\frac{\partial I_d}{\partial V_{gs}}\right)$ is calculated from the following current equation [10]:

$$I_d = \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}\frac{(V_{gs}-V_t)^2}{1+\theta(V_{gs}-V_t)}$$

where θ is known as the mobility degradation factor. θ is empirically extracted for a given process; for the IBM 0.25 µm process, it was extracted to a value of 2.5.

Following a similar process to earlier sections, the Sensitivity table 5 is computed.

Component	Sensitivity	ΔIIP3 (dBm)
L_G	0.002/nH	0.19
L_S	7.24/nH	1.3
C_{gs}	5.92/pF	0.43
W	0.013/µm	0.156
I_{BIAS}	0.59/mA	**1.65**
V_{TH}	55.34/V	**2.21**
R_{BIAS}	1.76/KΩ	**1.55**
V_{DD}	3.28/V	**1.64**

Table 5. Sensitivity table for IIP3

4 Applications and results

This analysis forms the basis for a formal fault-model paradigm in the RF front-end domain. By quantifying dependencies and performance degradation patterns, it can be used for optimal design of self-test and fault-tolerant systems. We have previously demonstrated successful on-chip self-calibration of LNAs in [5] [6].

The digital nature of self-calibration developed in [5] [6] is briefly summarized thus: LNA performance is sensed on-chip using novel sensors and algorithms, and downconverted to DC. The DC signals are analyzed using low-overhead circuitry, and performance specifications are quantified. This information is then used to digitally modify circuit parameters, and realign circuit performance to its desired value. For example, the circuit adaptability used in [5] uses a digitally tapped inductor to dynamically change gate inductor values, and correct the input-match frequency. The SA offers guidelines on the following issues:

a. The expected range of performance degradation for which the circuit should successfully test and/or calibrate itself.
b. The pattern of performance degradation identifies critical components that affect the specification, and their impact on other specifications
c. Most suitable component to be dynamically modified for each specification
d. Impact of this modification for the rest of the circuit specifications and compensation in the case of negative effects, if any
e. If the circuit component is modified in discrete steps, then the spacing between these steps has to be determined
f. Number of such steps to be programmed into the design

As a case study, this process is described for input-match frequency calibration in the next subsection

4.1 Input-match diagnosis and calibration

Fig. 5 shows the chip-micrograph of a 1.9 GHz LNA (IBM 6RF 0.25 µm process) with adaptive S_{11} behavior, and Fig.6 shows the four different S_{11} curves.

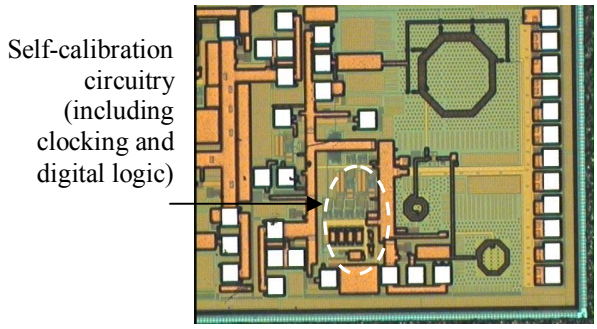


Fig. 5 Chip micrograph of a 1.9 GHz LNA

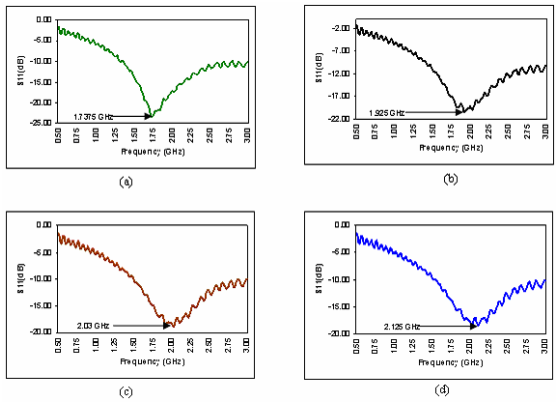


Fig. 6 Four S_{11} curves for the adaptive LNA

[2] The incremental gain is computed at three different input amplitudes, with 0 being the reference and +V and –V being the other two voltages. For this work, V is 50 mV.

To design this system, the first step was to identify the expected degradation in S11 frequency for the given process had to ascertained using Sensitivity Table 2 (0.27 GHz for the particular example). It then follows that testing/sensing mechanism must be designed to detect frequency changes in the range of 0.27 GHz.

Following this step, application requirements dictates the range over which S_{11} is made adaptive (0.5 GHz in this work). Due to the digital nature of calibration, the spacing of the steps and number of steps has to be ascertained. This design chose steps of 0.1 GHz (S_{11} frequency). The SA aids in choosing the gate inductor values to provide steps of 0.1 GHz. Using Table 2 and Fig.4, the four gate- inductor values (Table 6) were designed by tapping the outer turn of the coil and connecting them to switches (Fig. 7).

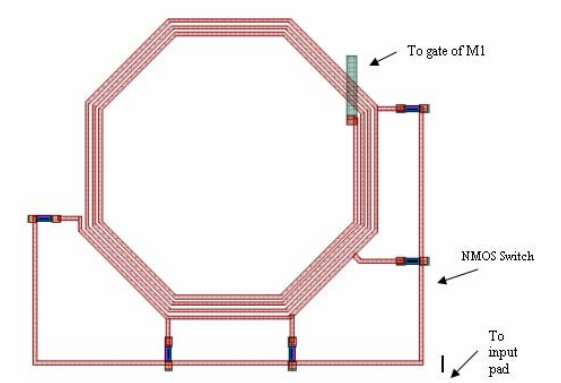


Fig. 7 The tapped gate coil

Tap no.	L_G value	Simulated S_{11} freq	Digital word input	Measured S_{11} freq
1	7.4 nH	1.7 GHz	00	1.73 GHz
2	9 nH	1.91 GHz	01	1.925 GHz
3	10 nH	2.0 GHz	10	2.03 GHz
4	11 nH	2.11 GHz	11	2.125 GHz

Table 6. The tapped coil values derived from SA, and validation with measured results

Further, it is verified that the impact of modifying L_G will not significantly impact input-impedance magnitude. With Table 3 depicting a sensitivity of 0.35 GHz per nH of L_G, varying L_G by approximately 4 nH nH will not impact S11 magnitude by more than 2 dB. This is also verified in the measured results of Fig. 7, where all S11 curves are less than -18 dB, and within 2 dB of each other. The SA also clearly indicates that variations in L_G have minimal impact on other specifications, thus making it the ideal candidate for calibrating S_{11}. The use of NMOS switches in Fig. 7 degrades the Q-factor of L_G, and this trade-off is also inferred from SA table 4 (The insertion loss of the switch degrades Q_{LG}, thus impacting NF).

We have demonstrated such a self-calibration methodology for output-match and gain also [8]. The SA developed in this paper forms the basic set of guidelines for achieving fault-tolerance using self-calibration.

5 Conclusions

RF reliability is an issue of growing concern in an RFIC world of increasing complexity, process variations and massive integration. While testing of such ICs has received considerable attention, the RF domain still lacks formal fault-modeling and sensitivity analysis approaches. This paper describes a Sensitivity Analysis methodology, and its application to a Low Noise Amplifier. The methodology quantifies performance degradation, inter-dependencies between parameters, and maps all dependent parameters onto specific performance specifications. Such an analysis can lead to optimal self-test solutions and fault-tolerance approaches, and a case-study of one such application has been described.

The Sensitivity Analysis itself is a stand-alone, simulation-free technique that lends itself well to multiple iterations and is ultra-fast. It can be re-used for any process and design by providing the new design and process information. The Sensitivity Tables and graphical plots are re-calculated and displayed. It provides the user with an early-design set of guidelines towards optimal design, test and fault-tolerance.

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