Double-Via-Driven Standard Cell Library Design

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Abstract

Double-via placement is important for increasing chip manufacturing yield. Commercial tools and recent work have done a great job for it. However, they are found with a limited capability of placing more double vias (called via1) between metal 1 and metal 2. Such a limitation is caused by the way we design the standard cells and can not be resolved by developing better tools. This paper presents a double-via-driven standard cell library design approach to solving this problem. Compared to the results obtained using a commercial cell library, our library on average achieves 78% reduction in dead vias and 95% reduction in dead via1s at the expense of 11% increase in total via count. We achieve these results (almost) at no extra cost in total cell area and wire length.

1. Introduction

Via in a VLSI design has been one of the important sources that invite manufacturing defects and cause reliability problem during operation. With interconnect width kept shrinking and the introduction of copper metallization process, the probability of creating open vias or partially void vias increases considerably. To alleviate this problem, foundries encourage designers to use at least two vias to connect metal wires locating at two different layers as shown in Fig. 1 [1-5]. There are two ways to achieve this goal as shown in Fig, 2. One is to perform double-via (DV) placement during routing, whereas the other is to do it after routing. Placing double vias on-the-spot during routing is still in its inception. We call this approach DV-driven routing as shown on the left of Fig. 2. Side effects induced by DV-driven routing are still not well investigated. However, it is believed that this routing approach will exacerbate wiring congestion. The maze router designed by Xu et al. [6] is a DV-driven router. As to post-routing approach, a redundant via (RV) is inserted to a place adjacent to a via of our interest. The insertion must conform to layout design rules. Lee and Wang formulated the insertion problem as a problem of finding a maximum independent set in a graph [7]. Chen et al. proposed a faster approach to the same problem which is formulated as a bipartite graph matching problem [8]. The work in [9] and commercial tools such as [2,10] also provide such a capability to designers. To further increase RV insertion rate, Yao et al. in [11] designed an RV aware multilevel router that considers the cost of placing double vias during maze routing. Chen et al. in [8] presented an RV aware gridless multilevel router. The results obtained by an RV aware router are then fed into a post-routing RV insertion tool to complete the placement of double vias. The post-routing RV insertion rate with respect to the total number of vias in layout designs obtained by either an RV aware or a conventional router ranges from 70% to 98%.

Post-routing RV insertion is in the main stream of current practice, which might be assisted by an RV aware router. Although previous work has done a great job for RV insertion on one aspect or another, our own study finds that only 20%~50% of via1s get inserted with redundant via1s (connecting metal 1 wires to metal 2 wires). This finding is consistent with that presented in [7]. Since via1 is more critical than any other type of vias, it is desirable to have a higher via1 insertion rate. We have found that most of via1s, each of which is not accompanied by a redundant via1, occur at the IO pins of a cell. The main reasons for this have two.

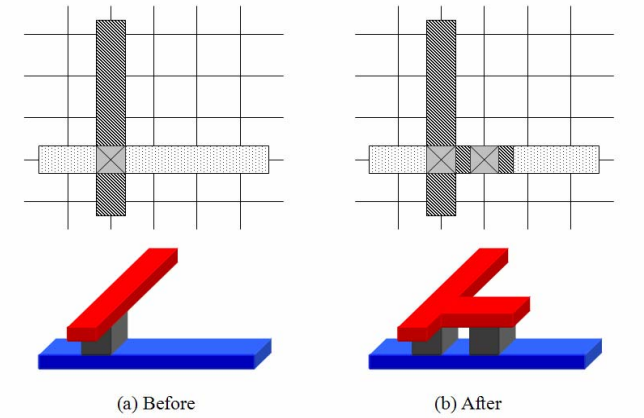

Fig.1: Redundant via insertion.

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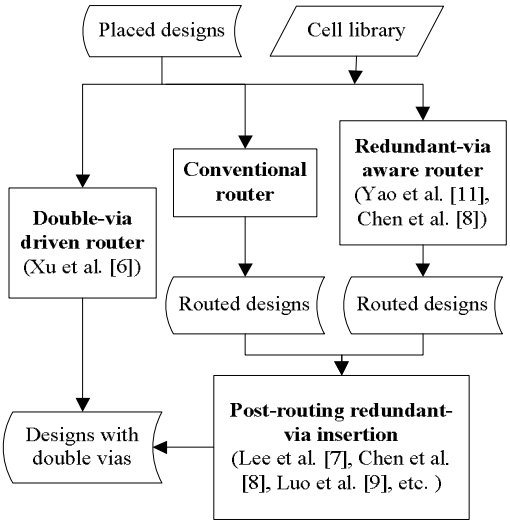

Fig. 2: Approaches to double-via placement.

- The pins of a standard cell are normally designed with metal 1. Adding a redundant via1 to a pin is often found impossible because the metal 2 areas above the pin have been covered by the wires of different nets.
- The standard cells are not designed for serving RV insertion. We have observed that metal 1 pins of some standard cells in a commercial cell library are not extendable to allow adding of an RV to a pin. Pin A in Fig. 3 illustrates such a situation.

We can tackle the first problem using a DV-driven or an RV aware router. However, there is no way to solve the second problem simply using a routing tool. Based on the above observations, the most likely way to improve via1 insertion rate is to redesign the standard cells in a cell library. In this paper we propose a DV-driven standard cell library design approach to achieving this goal. Two standard cell libraries DV1 and DV2 are designed. DV1 provides each pin with sufficient metal 1 area to hold at least two vias. It can be used along with a DV-driven router, a conventional router, or an RV aware router. The later two cases need a post-routing RV insertion tool to install a second via so that via1 duplication is not guaranteed. On the contrary, DV2 directly installs two via1s at each pin and promotes the pins to metal 2. Via1 duplication at each pin is thus guaranteed before routing. Hence, it is not necessary to make any change to a conventional router to support redundant via1 insertion. Various kinds of experiments using DV1, DV2, and combinations of DV1 and DV2 have been performed. Compared to the results obtained using a commercial cell library, DV1 does not render good results in reducing dead via count. One possibility is that the places for adding a redundant via1 to the cells in DV1 are more seriously occupied by other metal 2 wires. Hence, a DV-driven or an RV aware router needs to be employed to take advantage of DV1. For the circuits designed with DV2, dead via count is on average reduced by 78% and dead via1 count is on average reduced by 95% at the expense of 11% increase in total via count. When reduction in dead via count is translated into yield gain, DV2 indeed achieves better yield improvement than any other approaches, especially for the cases with large single-via failure rates. We achieve the above results (almost) at no extra cost in total cell area and total wire length. The best results are obtained when there are at least four or more metal layers. Besides, our approach is simple, practical, and effective.

The rest of this paper is organized as follows. Section 2 elaborates on why a DV-driven cell library is needed. Section 3 describes our DV-driven standard cell library design approach. Section 4 gives the experimental results. The last section draws some conclusions.

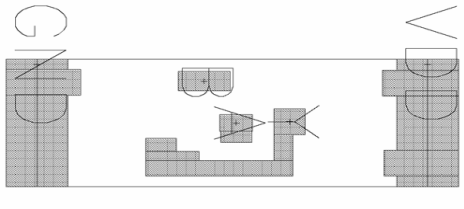

Fig. 3: Abstract view of a commercial NAND2 cell.

2. Why a DV-Driven Library?

Section 1 has revealed our motivation of conducting this research. However, upon surveying the available literature, one might deny the arguments we made in Section 1 if one does not pay attention to how the data in the literature are obtained. The data reported recently show that a post-routing RV insertion approach is capable of achieving near 100% insertion rate. If this is still true for the case where the circuits are designed with a commercial cell library, there is no reason for us to conduct this research. So let us see why we really need a DV-driven library. First, we summarize the experimental data presented in [7], [8], [9], and [11] in Table 1. The columns denoted by "Alive" give the average insertion rates with respect to the number of alive vias, whereas those denoted by "Total" give the insertion rate with respect to the total number of vias. An alive via is a single via where there exists at least a place to hold a redundant via around it. The row denoted by CV (RVA) means that the routed designs input to a post-routing RV insertion tool is generated by a conventional (RV aware) router. An entry denoted by NA means non-availability. Based on the data given in Table 1, we have the following observations:

- Post-routing redundant via insertion with respect to alive vias can hardly be done much better than what we have now.

- An RV aware router does help to increase the average insertion rate up to 2.2% at the expense of 1.8% increase in the total number of vias [8].
- The insertion rates with respect to the total number of vias are not consistent throughout the above four approaches, i.e., 94.8% in [8], 92.1% in [9], 97.9% in [11], and 70.1% in [7].

Method / Router	Chen et al. [8]		Yao et al. [11]	Luo et al. [9]	Lee et al. [7]	
	Alive	Total	(Total)	(Total)	Alive	Total
CV	NA	92.6	NA	92.1	99.6	70.1
RVA	98.6	94.8	97.9	NA	NA	NA

Tab. 1: Redundant via insertion rates (%).

The last bullet is the foremost interesting. Even though the insertion rate of 70.1% in [7] is achieved for the layout designs generated by a conventional router, the rate would not be considerably higher than 70.1% if the RV insertion were done for the layout designs generated by an RV aware router. This argument is made based on the observation presented in the second bullet. So, how could the situation in the third bullet happen? Our answer is that the insertion rate with respect to the total number of vias highly depends on the abstract views of the cells (gates) in a cell library. With a private communication to the authors in [7], we are told that a 0.18 um commercial cell library [12] has been used to describe the designs. It is found that the lower insertion rate reported in [7] is mainly caused by a considerable portion of dead via1s (in contrast to alive vias), which on average amounts to 26.4% with respect to the total number of vias. Our own study using the same commercial cell library justifies such a consequence. This places an upper bound on the RV insertion rate.

As for the work in [8] and [11], the higher insertion rate is also attributed to the libraries used to describe their benchmark circuits. Both [8] and [11] use the same set of benchmark circuits, each of which contains cell instances from a very simple library. For the ISCAS89 circuits, the library being used there consists of only three gates, a 2-input NAND, an inverter, and a flip-flop. The abstract views of these three gates are very simple. Each of their IO pins is simply a small square on metal 1 as shown in Fig. 4 except that nothing is found on metal 1 layer. The libraries used for the benchmark circuits other than the ISCAS89 circuits are also similar except that the macros contained in the library are much larger than basic logic gates. With such kind of libraries used in [8] and [11], it is basically no need to place a via1 on a pin because metal 1 pins are easily accessible using metal 1 wires. This is the reason why very high insertion rate can be achieved. However, a real circuit is seldom designed with this kind of cell library. As to the work presented in [9], libraries used for its benchmark circuits are not disclosed there.

On account of the above analysis, RV insertion rate for a circuit highly depends on the library used for describing the design. In a more realistic situation where a commercial cell library is used, a very high insertion rate is not achievable simply using better tools. This gives concrete evidence to the need of a DV-driven library for resolving the low insertion rate problem in via1s.

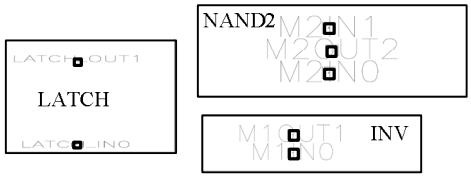

Fig. 4: Abstract views of some basic gates (only topologically but not geometrically correct).

3. DV-Driven Standard Cell Library

We design two standard cell libraries, DV1 and DV2. DV1 provides each pin with sufficient metal 1 area for accommodating at least two via1s. DV1 addresses the problem of insufficient metal 1 pin area. DV2 pre-installs two via1s at each pin of the cells. RV insertion at IO pins is thus guaranteed before routing. DV2 can resolve the problem about low insertion rate of via1s.

Here we design a small cell library, instead of a full-blown one. Our cell library contains 48 frequently used standard cells such as INV, NAND, NOR, XOR, AND, OR, AND-OR-INV, and DFF with different drive strengths and different number of input pins. These cells are designed with UMC 0.18μm process technology. For the purpose of making a fair comparison, each cell we design has the same dimension as that of its counterpart in a UMC 0.18μm standard cell library [12]. Power/ground bus width, layout grid, and vertical/horizontal pin grid are all set equal to that used in the UMC cell library. The transistors in a cell are tuned to produce the same timing characteristics as that of its counterpart.

We use a layout editor to handcraft the art work of each cell. We run DRC (design rule check) and LVS (layout versus schematic) to verify cell layouts. The post-layout HSPICE simulations are performed to see if the timing meets the specification. Once this is done, the abstract view of a cell layout is translated into a library exchange format (LEF) file. For the cells in DV1, only metal 1 of a pin is treated as ports. For the cells in DV2, both metal 1 and metal 2 of a pin are treated as the ports. Each pin in a cell is designed in such a way that it is placed in parallel with metal 2 routing tracks so that the adjacent metal 2 routing tracks will not be blocked by the pin. This is illustrated in Fig. 5. Fig. 6 shows a layout of D flip-flop and NAND2 in DV2, respectively. If we remove the metal 2 plates and the via1s on the pins of these two cells, these two cells become the cells in DV1.

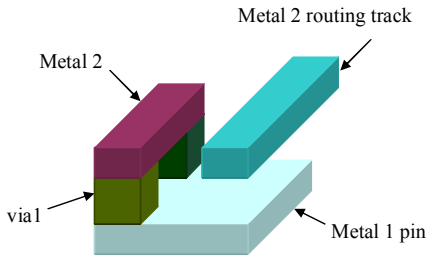

Fig. 5: Vias placement.

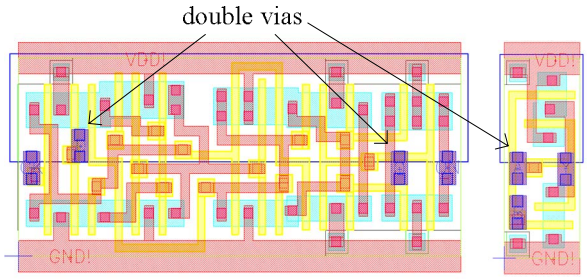

Fig. 6: Double vias on pins of DFF (left) and NAND2

A problem which is critically important for designing DV1 or DV2 is to align pins vertically with the routing tracks on metal 2 and horizontally with the routing tracks on metal 1. In the past, this is often a requirement for cell designs for the sake of improving routability. However, it is currently not enforced because almost all the contemporary routers can handle off-grid pin access very well. Let's see what will happen if the above requirement is not respected. First, when designing cells in DV1, we would end up with a situation that a metal 1 pin indeed has enough space to hold two vias, but in reality this does not occur. For example, given in Fig. 7 is part of the abstract view of a D flip-flop in a commercial cell library. Pin *Q* indeed has enough space to hold at least two via1s, but an RV can not be added to pin *Q* without causing a layout rule violation. The problem is that when a router drops the first via1 on pin *Q*, the via1 will be placed at the grid point formed by the metal 1 (horizontal) and metal 2 (vertical) routing tracks. As a consequence, a rule violation happens when we add an RV to pin *Q* after routing. This problem can be solved if a router drops the first via1 on *Q* at a location lower than where it is now, i.e., we can add an RV either to the left or to the right of the first via. However, a router is normally not designed to do so. Therefore, we design our DV1 cells in such a way that any pin aligns vertically with the routing tracks on metal 2 and horizontally with the routing tracks on metal 1. However, if a router has the capability of dropping an off-grid via1, such a rule can be removed. To achieve best via1 insertion effect, a router still needs to be modified to drop a via1 smartly at the place where a redundant via1 can be added later. Similarly, the above rule should also be respected when designing DV2 cells. Otherwise, each metal 2 pin would block one extra metal 2 routing track and thus may seriously impact the routability of a design.

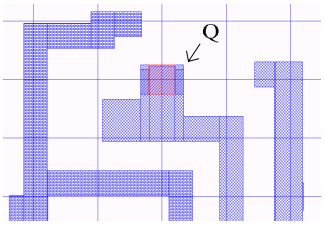

Fig. 7: Unable to place double vias on pin Q.

The cells designed in this way are not without their problems. First, a designer may find difficulties of placing a large enough metal 1 pin on the grid points for some cells. If this situation occurs, a cell designer can choose to increase the cell area or leave the pin as it is without cell size increase. The decision may depend on how often a cell is used in designs and on the relative magnitude of failure probabilities of a single via and double vias. The other noticeable problems may include the potential increases in total wire length, via counts, pin capacitance, the possibility of routing failure when routing resources are limited, etc. We will show the extent of some of these problems in our experiments. Note that the increase in pin capacitance can be offset by the decrease in via resistance.

4. Experimental Results

Here we perform some experiments to see whether the proposed cell library design approach can effectively increase RV insertion rate. Three standard cell libraries, DV1, DV2, and UMC018 (a commercial library) are tested. For simplicity, we call a synthesized design using *X* library an *X*-synthesized design. Three large ISCAS-89 circuits and two ITC-99 circuits are employed to test our libraries. A circuit synthesized by Design Compiler using UMC018 library is constrained to use only those cells, each of which has a counterpart in DV1 or DV2. We then use a commercial tool suite to perform placement and routing (not RV aware) and the program from [7] to perform post-routing RV insertion. Chip area of a benchmark circuit is kept the same no matter which cell library is used. The core utilization in each circuit is 90%. No spare cells are deployed. Each circuit is routed with three, four, and five metal layers, respectively.

In addition to using UMC018, DV1, and DV2, we also do other two types of experiments. Each needs a trial run to get a DV1-syntheized (DV2-synthesized) routed design. The first type is to replace a DV1 cell in a DV1-synthesized routed design by its counterpart in DV2

if all pins in the DV1 cell are connected to metal 2 wires directly by via1s. This approach is called DV12. The other type is to replace a DV2 cell in a DV2-synthesized routed design by its counterpart in DV1 if at least one of the pins in the DV2 cell is connected to metal 1 wire directly. This approach is called DV21. Table 2 shows our experimental results only for the case using 4 metal layers due to lack of space. The results given in Table 2 are somewhat better than that for the case using 3 metal layers and somewhat worse than that for the case using 5 metal layers. Each bracket in an entry contains a normalized number with respect to the result obtained using UMC018 library. We have the following observations (based on all the results obtained using 3, 4 and 5 metal layers). All comparisons are made with respect to the results obtained using UMC018 library.

- The dead via count is monotonically reduced with increasing number of DV2 cells in a circuit, whereas the total via count before RV insertion is monotonically increased with increasing number of DV2 cells in a circuit. For the circuits that use DV2, dead via count is reduced by 64%~84% (78% on average) and dead via1 count is on average reduced by 95% at the expense of 7%~18% (11% on average) increase in total via count. We can also clearly see the trade-off between total via count and dead via count.
- DV1 does not perform well in reducing dead via count but does help to reduce total via count by 2%~4% and via1 count by 1%~4.5% in a design. The reason for total via count reduction is possibly due to the improvement of metal 1 pin accessibility. However, the reduction in dead via1 (via) count is not consistent. In some cases, DV1 even incurs up to 20% (23%) more dead vias (via1s) than UMC018. We are still not totally clear why this happens. One possibility is that the places for adding a redundant via1 to the cells in DV1 are more seriously occupied by other metal 2 wires. Hence, a DV-driven or an RV aware router needs to be employed to take advantage of DV1.
- The insertion rate is on average increased from 66% with UMC018 library to 93% with DV2. The insertion rate achieved with DV2 is similar to those obtained by Chen [8] and Luo [9] (see Table 1).
- No routability degradation is observed. The total wire length is fluctuated within ±5%. Note that the above results are achieved at no extra cost in total cell area.

How good are the results we have obtained? It is somewhat difficult to answer this question. The problem is that we reduce dead via count at the expense of increasing total via count. Thus, it is interesting to see how much gain in via yield is achieved with our approach. To make yield calculation more realistic, we assume that single-via failure rate ranges from 5E-9 to 5E-6 [9] and the double-via failure rate is about 1/40 times the failure rate of a single via [4]. Assume Poisson yield model is used and the possibility of the opens or shorts on the metal overhangs for redundant vias is ignored. Figs. 8 and 9 show that DV2 indeed achieves better yield improvement than any other approaches, especially for the cases with large single-via failure rates. Two large ITC-99 circuits b17 and b18 are also tested (in many cases the program from [7] can not complete RV insertion for the large circuits). Fig. 10 also shows that the results for b17 and b18 are consistent with that given in Figs. 7 and 8.

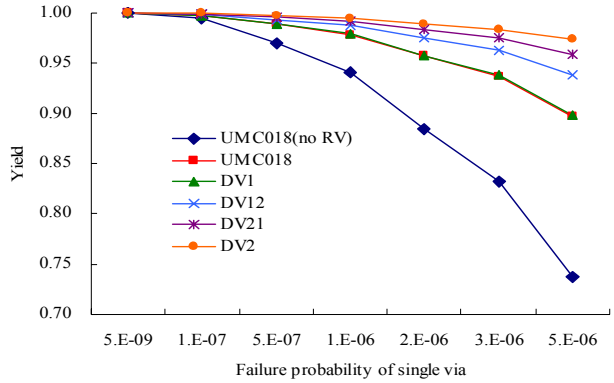

Fig. 8. Via yield improvement for s35932.

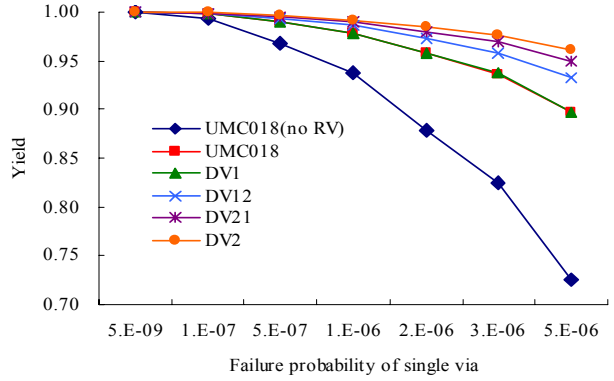

Fig. 9: Via yield improvement for b15.

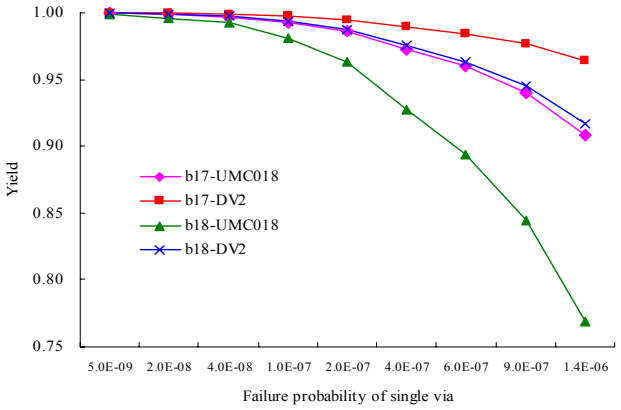

Fig. 10: Via yield improvement for b17 and b18.

5. Conclusions and Future Work

In this paper we propose a standard cell library design approach to addressing the problem of low RV insertion rate for via1s. We design two cell libraries, DV1 and DV2. DV2 achieves on average 78% reduction in dead via count and on average 95% reduction in dead via1 count at the expense of 11% increase in total via count. This is achieved (almost) at no extra cost in total cell area and total wire length. Despite of being unable to reduce dead via count with DV1, we are interested in designing a DV-driven or an RV aware router to take advantage of DV1 in the future. Moreover, we need to perform experiments for the designs with spare cells. We expect that DV2 will be more competitive in this situation.

Circuit	Library	Total via count		Via1 count		Dead via count		Dead via1 count		Insertion rate	Via1 insertion rate	Total wire length
	UMC018	61102	(1.00)	27388	(1.00)	20855	(1.00)	17537	(1.00)	0.66	0.36	(1.00)
	DV1	58976	(0.97)	26770	(0.98)	20492	(0.98)	17437	(0.99)	0.65	0.35	(0.99)
s35932	DV12	60490	(0.99)	27206	(0.99)	11414	(0.55)	8359	(0.48)	0.81	0.69	(1.01)
	DV21	62881	(1.03)	27568	(1.01)	7063	(0.34)	3839	(0.22)	0.89	0.86	(0.99)
	DV2	67462	(1.10)	29075	(1.06)	3833	(0.18)	412	(0.02)	0.94	0.99	(0.96)
	UMC018	55102	(1.00)	24476	(1.00)	19354	(1.00)	16343	(1.00)	0.65	0.33	(1.00)
	DV1	52758	(0.96)	24218	(0.99)	20426	(1.06)	17677	(1.08)	0.61	0.27	(0.98)
s38417	DV12	55269	(1.00)	24964	(1.02)	9295	(0.48)	6539	(0.40)	0.83	0.74	(0.98)
	DV21	56695	(1.03)	25138	(1.03)	6096	(0.31)	3264	(0.20)	0.89	0.87	(0.97)
	DV2	59781	(1.08)	26330	(1.08)	3179	(0.16)	380	(0.02)	0.95	0.99	(0.95)
	UMC018	62921	(1.00)	27356	(1.00)	21123	(1.00)	17827	(1.00)	0.66	0.35	(1.00)
	DV1	60559	(0.96)	26768	(0.98)	22572	(1.07)	19534	(1.10)	0.63	0.27	(1.01)
s38584	DV12	62873	(1.00)	27470	(1.00)	11478	(0.54)	8362	(0.47)	0.82	0.70	(1.02)
	DV21	64089	(1.02)	27643	(1.01)	7358	(0.35)	4278	(0.24)	0.89	0.85	(0.98)
	DV2	67409	(1.07)	29279	(1.07)	3983	(0.19)	910	(0.05)	0.94	0.97	(0.96)
	UMC018	64314	(1.00)	27066	(1.00)	20740	(1.00)	17500	(1.00)	0.68	0.35	(1.00)
	DV1	63055	(0.98)	26658	(0.98)	20565	(0.99)	17469	(1.00)	0.67	0.34	(1.00)
b15	DV12	66875	(1.04)	26948	(1.00)	12715	(0.61)	9548	(0.55)	0.81	0.65	(1.06)
	DV21	68515	(1.07)	26992	(1.00)	9068	(0.44)	5629	(0.32)	0.87	0.79	(1.02)
	DV2	72404	(1.13)	28273	(1.04)	6231	(0.30)	2191	(0.13)	0.91	0.92	(1.00)
	UMC018	73150	(1.00)	32569	(1.00)	21598	(1.00)	19140	(1.00)	0.70	0.41	(1.00)
	DV1	71180	(0.97)	31079	(0.95)	26003	(1.20)	23521	(1.23)	0.63	0.24	(0.97)
b14	DV12	74305	(1.02)	31325	(0.96)	11901	(0.55)	9681	(0.51)	0.84	0.69	(1.03)
	DV21	77216	(1.06)	31357	(0.96)	8000	(0.37)	5434	(0.28)	0.90	0.83	(1.02)
	DV2	82427	(1.13)	32971	(1.01)	4104	(0.19)	1048	(0.05)	0.95	0.97	(0.97)

Tab. 2: Effectiveness of redundant via insertion.

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