Reconfigurable System-on-Chip Data Processing Units for Space Imaging Instruments

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Abstract

Individual Data Processing Units (DPUs) are commonly used for operational control and specific data processing of scientific space instruments. To overcome the limitations of traditional rad-hard or fully commercial design approaches, a System-on-Chip (SoC) solution based on state-of-the-art FPGA is introduced. This design has been successfully demonstrated in space on Venus Express. From this, a reconfigurable DPU design for future advanced imaging sensors is derived using embedded processing cores. In addition, a SoC design variant is presented based on recently available FPGA technology with integrated hardwired processor, which is capable to support also high end payload applications.

1. Introduction

Data Processing Units (DPUs) are used as interface between the spacecraft and several instrument sensor electronics or heads, providing the operational control and specific data processing of scientific space instruments. These systems have to provide sufficient computing power, mission specific radiation tolerance, low consumption of power, volume and mass, and adequate reliability at moderate unit costs. For high-resolution, high-speed imaging instruments, especially acquisition sequence control and image processing (e.g. data compression) impose strong real-time requirements on the system design to handle the high sensor data rates in the order of up to some hundred Mbit/s for advanced sensors.

In principle three implementation approaches for data processing systems exist:

1. Traditional design based on rad-hard discrete components or Application-Specific Integrated Circuits (ASICs) of high quality level,
2. Commercial Off-The-Shelf (COTS) approach using integrated solutions,
3. Reconfigurable System-on-Chip (RSoC) solution with processor and special functions in radiation tolerant Field Programmable Gate Array (FPGA).

In this paper we will focus on the reconfigurable System-on-chip approach, which has been already successfully demonstrated in Space for the Venus Express Monitoring Camera VMC [1]. The three approaches are shortly compared with respect to the requirements above and the advantages for the RSoC approach are outlined. Based on the VMC DPU, a reconfigurable DPU design for future advanced imaging sensors is derived and the achieved design characteristics are outlined. In addition a second RSoC design variant is presented, based on recently available FPGA technology with integrated hardwired processor.

2. Design approaches

Independent of the approach, mission specific radiation tolerance and reliability have to be guaranteed by the design. Radiation effects can be classified in permanent (Total Ionizing Dose, TID, and Latch-Up, LU) and transient failures (Single Event Upset, SEU, Single Event Functional Interrupt, SEFI). Protection against both can be achieved by using parts build of special technology and/or by design provisions. This required protection is carefully considered for the different design approaches.

2.1. Traditional design

In the traditional design data sources (i.e. scientific space instruments) are equipped with stand-alone data processing units using radiation hardened (RH) parts. The present available rad-hard processors (e.g. ERC32, TSC21020 or AT697) offer low to medium processing performance and therefore are typically used for control and sequencing tasks, only. To handle high sensor data rates, DPUs need to include some dedicated hardware for offline (via intermediate data mass storage) or online processing (e.g. data compression ASIC). Such classical systems show clear disadvantages in resource allocation (low integration density and moderate performance). The state-of-the-art solution could be a complete SoC system implemented within a radiation hardened ASIC. But also this approach has the drawback of long development time

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and low adaptability to changing mission needs due to dedicated implementations with fixed dataflow paths and restriction to a simplified scheme, which needs to be frozen in an early project phase.

2.2. COTS approach

Commercial off-the-shelf available devices use standard processes and plastic encapsulation. This approach combines state-of-the-art performance with small outline lightweight packages and intrinsic high reliability of high volume production. Meanwhile it is agreed widely that plastic encapsulation and failure rates of COTS parts are acceptable or can be made acceptable by additional measures for the space environment. This allows for very compact DPU designs [2], [3]. But, the big disadvantage of using COTS parts is that every part has to be tested for radiation resistance (TID & SEU) and other environmental (e.g. temperature) performance. This needs a lot of preparatory work and due to the short availability time of commercial parts replacement types could have to be selected even after one mission.

2.3. Reconfigurable System-on-Chip solution

The availability of new radiation tolerant high density FPGA and processor technology enables new approaches to the instrument system architecture. An advanced SoC design integrates special functions (e.g. data compression or formatting/coding [4]) together with the processor system completely on a single or few high density FPGAs. Figure 1 depicts the general architecture of such an advanced DPU design. Scalable on-chip architectures for data handling systems use common modules, standardized interfaces, and modeling tools to customize to each new mission objectives. Such highly integrated designs have low resource requirements for both, power and mass, but moderate to high processing power capabilities, which is mandatory for significantly restricted resource budgets on e.g. interplanetary missions. The major requirements are flexibility, (re)programmability, modularity, and module re-use. The last point is very important, since developing and implementing systems of such complexity are only feasible and affordable if basic elements can be reused. This will become much more crucial in the future. The key parameters of the different approaches together with their advantages/disadvantages are summarized in Table 1 for comparison. Both, already operational DPUs and current designs are shown.

3. SoC DPU design variants

Field programmable gate arrays have the major advantage for space applications that the complete development and test cycle is kept within the developer in-house responsibility. This is cost effective for development and production of small series, like it is usually needed for space-borne applications. A dedicated MCM or ASIC is not useful for small volume production with different interfaces and application tasks for each instrument. Today large gate count FPGAs are available also for space applications with required qualification level and radiation tolerance, e.g. Xilinx XQR Virtex-I and Virtex-II series with gate counts of up to 6 million system gates. Low internal core voltages allow for high throughput and low power implementations of complex processing tasks. These Xilinx FPGAs are configured by means of a configuration RAM, which is as prone to single event upsets as the internal logic and memory cells (BlockRAM), but enables re-programmability of the complete or partial system during development or even in-flight. Using basic SEU mitigation by dedicated design measures (e.g. in operation functional testing of the device, configuration memory scrubbing, Triple Modular Redundancy, TMR) the expected SEU rates for a broad range of applications can be reduced to negligible or at least tolerable values [5], [6]. Zero effective upsets is not our objective, but to achieve the optimum availability for given system constraints (cost, performance, mass, etc.).

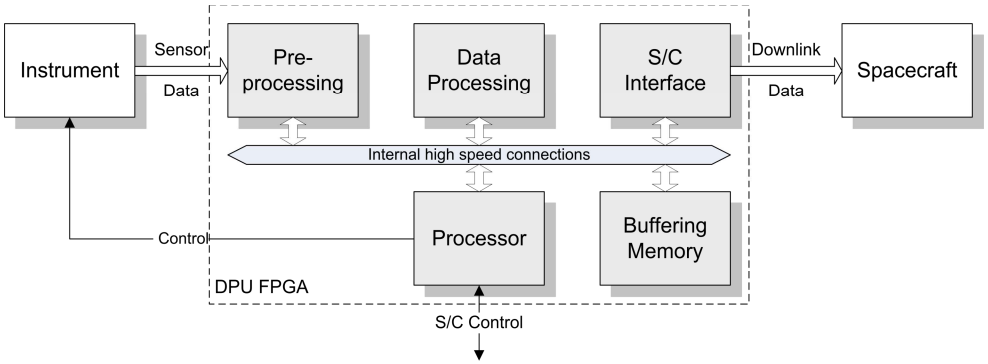

Figure 1: Advanced System-on-Chip DPU Architecture

Table 1: Key parameters of different approaches

Approach	Traditional	COTS	Reconfigurable SoC	Combined SoC
Operational DPUs	***Rosetta Rosina***	***µDPU***	***VEX VMC***	
Processor	TSC21020	DSP56302	LEON-2 in Virtex-I	
Volume excl. box [cm^3]	850	70	250	
Mass excl. box [g]	800	80	280	
Power consumption, secondary [W]	4 - 6	0.4 - 4	3.5	
Processing power [MIPS]	6 - 20	0 - 100	20	
Fast program memory	16 Mbit	6 Mbit	16 Mbit	
Science data memory	128 Mbit	1 Gbit	1 Gbit	
DPUs in development	***AT697 / ASIC***	***e.g. MSC8101***	***LEON-3 in Virtex-II***	***Virtex-II Pro / Virtex-4***
Power consumption, secondary [W]	2 - 4	1 - 4	2 - 4	1 - 4
Max. Processing power [MIPS]	86 / ~300	3000	~80	600
Permanent tolerance (TID, LU)	high	medium	high	medium
Transient tolerance (SEU, SEFI)	high	medium	medium	medium
Qualified reliability	high	medium	high	high
Component costs	high / very high	low	medium	medium
Development time	medium / long	medium	short	short
Flexibility	very low	low	high	high

3.1. Fully programmable approach

We have evaluated a flexible SoC style approach and identified functional blocks, which are well suited to be put together in a single highly integrated device:

- Processor incl. cache
- Application specific co-processors (e.g. for data compression)
- All peripheral interfaces (S/C and sensor side)
- Small FIFOs for interface decoupling
- All memory interfaces incl. error correction

The only devices not practical for integration are mass memories, which have a dedicated highly integrated structure and differ in size for each application.

This design was implemented in a first step for the micro Venus Express Monitoring Camera (VMC), using a "LEON-2" processor core, a SPARC V8 architecture compatible highly configurable VHDL model, in a radiation hardened Xilinx Virtex-I FPGA. Two FPGA devices had to be used for the complete system because of manufacturing reasons (avoid Ball Grid Array package, BGA). The FPGAs includes not only the processor itself, but all peripheral logic and interfaces to the different sensors and communication units:

- SDRAM controller including Direct Memory Access (DMA) burst controller for 16 Mbit/s image data transfer independent of processor
- Zero wait state memory error correction based on Reed-Solomon code with Single 8-bit Symbol Correcting (SSC, adjacent bits located in the same device form a symbol) capability for both, program SRAM and mass memory SDRAM. Cyclic background scrubbing of all cells is used to reduce the probability for non correctable multi-bit errors drastically.
- Boot PROM controller. If the program load from EEPROM fails, the DPU can be still commanded from S/C to upload new software
- Spacecraft RTU interface logic and FIFOs
- 1355 Spacewire interface controller and FIFOs
- Interfaces to internal subunits

The complete system in Figure 2 integrates also an internal camera image mass memory of 1 Gbit within a volume of 250 cm^3, a mass of 280 g and a power consumption of less than 3.5 W. The processor core in VHDL provides a computing power of 20 Million Instructions Per Second (MIPS). The real-time operating system RTEMS is used as basis for a complete instrument control and data processing system, implemented in a sophisticated on-board command language (OCL).

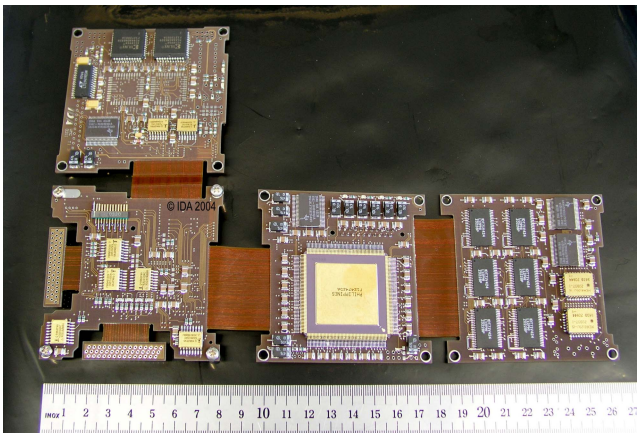

Fig. 2: Venus Express Monitoring Camera DPU

Partial hardware redundancy, reconfigurable subunits, majority voting, and graceful degradation of performance are implemented to get required reliability. For a timely protection of all FPGA areas and to eliminate SEU effects before they are accumulating, additional supervisor logic is implemented. A radiation hardened and TMR by design, one-time programmable Actel FPGA is used as supervisor circuit to achieve radiation tolerance. The implemented measures are

- configuration control of both Xilinx, including CRC/Sync error detection and main/redundant Xilinx PROM switching,
- continuous check of all critical Xilinx external signals to handle any SEU induced bus contention (possible permanent damage),
- latch-up switch control for SRAM and SDRAM,
- provision of 'SEU-hard' functions (e.g. power switching of subunits),
- register bank for critical system and software status protected by TMR,
- watch-dog triggered system reboot as the last resort to cover also SEFIs.

The calculated overall SEU rate of the design is in the order of a few errors per year for Galactic Cosmic Ray (GCR) Background, which is tolerable for a scientific instrument with an operating time of only some hours during a 24h orbit, so long term accumulation of errors is not a problem. Therefore no special measures to prevent accumulation of SEUs in Xilinx configuration have been implemented. VMC was successfully verified in space during Venus orbit insertion and routine science operations, which have been started mid. of May 2006. Since then, VMC DPU was switched on for an accumulated time of more than 1200 hours and is running very well. So far, only a few single errors in external RAM were detected and corrected during scrubbing. No indication of any SEU effect in the Xilinx devices has been observed up to now.

The major FPGA modules of the VMC processing system were enhanced and re-used with additional interfaces and improved system supervisor FPGA for the NASA DAWN Framing Camera. Especially the scrubbing (overwrite) of the FPGA configuration in short time intervals was enhanced to eliminate the long term accumulation of SEU effects. To decrease volume and mass further, stacked memory devices with 8-bit symbol error correction and latch-up protection are used for an internal camera image mass memory of 8 Gbit. The complete processor system has a volume of 600 cm^3, a mass of 520 g and a power consumption of less than 7 W. The increase compared to VMC is due to bulky MIL-Bus interface and Class S type parts requirements.

3.2. Embedded processing cores

For future missions, the Xilinx Virtex-II series is available as radiation hardened version (TID >200 krad, SEL LET >160 MeV-cm^2/mg) in a non-BGA package, providing up to 6 million configurable system gates. For comparison, VMC uses only about 800,000 system gates. This high gate count enables the integration of a standard programmable processor core together with dedicated online processing cores like data compression or on-board feature extraction into a single FPGA.

For a wavelet based online JPEG2000 compression, we have developed a hardware core using an image tile size of 128x128 pixels and running at 125 MHz, which performs a 5-level lossless discrete wavelet transform and Tier-1 encoding on the tile data. Using this in a highly parallel implementation on a 6M gates Virtex-II FPGA with a device utilization of 60 to 80 percent, an online data compression with data rate of up to 250 Mbit/s can be achieved. The JPEG2000 image compression standard provides important features, such as lossless and lossy compression, Region-of-Interest (ROI) coding, and progressive transmission by quality and resolution. It was selected as image compression standard for VMC and future missions, because it overcomes many disadvantages in traditional JPEG, such as the single resolution, single quality, no target bit-rate, no lossless capability, block artifacts, etc. Available commercial Intellectual Property (IP) cores for Xilinx FPGA are not suited for space instruments, because they are optimized only for commercial applications, e.g. the pixel resolution in lossless mode is not high enough (min. 14 bits required).

By using Virtex-II FPGA, an enhanced design compared to the VMC processor system can be implemented with a performance of up to 80 MIPS. An improved "LEON-3" processor core is integrated together with powerful dedicated real-time data processing and compression cores within a single chip, shown in Figure 3. An instrument DPU is planned to be implemented, which integrates also an internal mass memory of 8 Gbits within a volume of 250 cm^3, a mass of 250 g and a power consumption of less than 4 W.

In-flight re-programmability of the FPGA system is achieved by using additional Xilinx configuration EEPROM, programmable via the S/C interface implemented in the rad-hard Actel FPGA. To facilitate this, we have developed a design for remote configuration upload within the Actel FPGA. This core allows the reliable transmission of data by telecommand and programming of Xilinx EEPROMs via the IEEE 1149 JTAG boundary scan interface. The approach enables hardware IP-core reconfiguration, giving the same adaptability as for a software implementation. It offers a great amount of flexibility and is feasible for applications

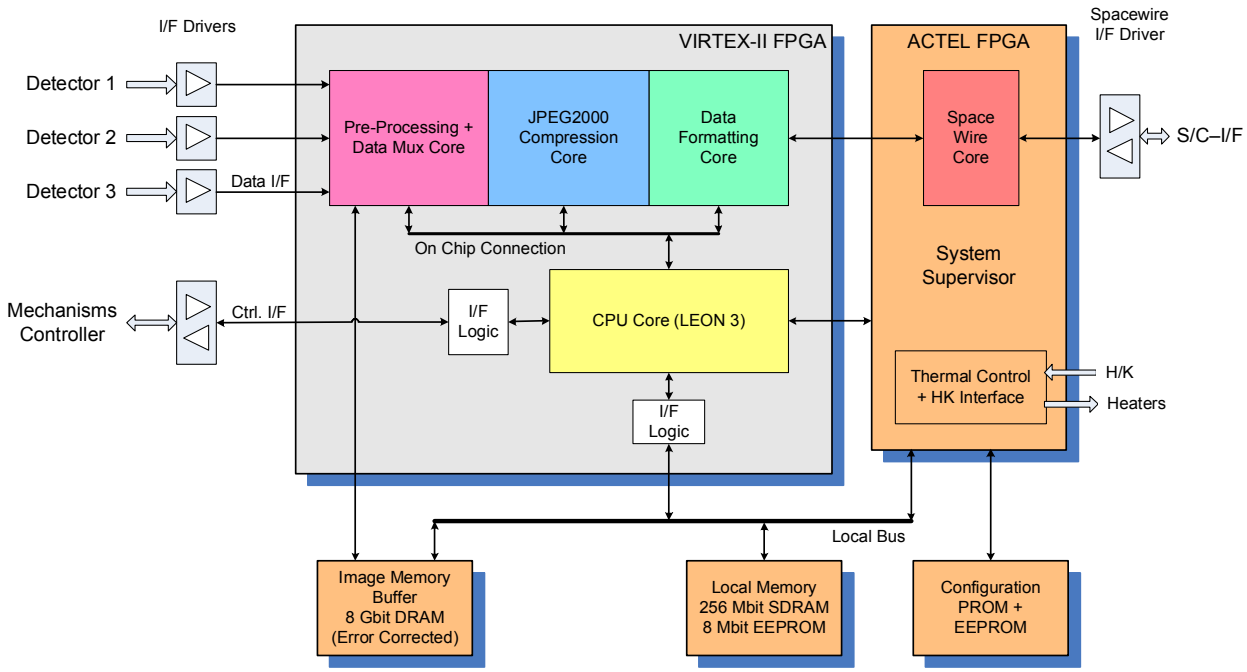

Figure 3: Reconfigurable SoC Design with Online Processing Cores

that need a moderate adjustable processing power of up to hundred MIPS. By means of a second identical FPGA processor system in master/monitor configuration, this approach can even be applied to critical applications where high availability is required.

3.3. Combined SoC approach

The implementation of a complete processor core in even the fastest FPGA available today offers a processing power not higher than about 100 MIPS and consumes more power than a comparable hard-wired processor. To overcome this, Xilinx introduced the Virtex-II Pro series of FPGA which offers a real SoC combination of hard-wired processor core together with fully programmable logic and embedded memory in one chip. According to Xilinx, this will be available also as radiation tolerant version. Two processor cores of a standard IBM PowerPC 405 with processing power of up to 600 MIPS are integrated in a single off-the-shelf programmable device and provide a great amount of flexibility for high performance applications. The standard processor is needed by every application and around this instrument specific processing cores and interfaces can be implemented.

We have done a survey of COTS available processors including the Virtex-II Pro to evaluate this design approach for high performance applications [7]. This shows that the Virtex-II Pro performs quite well compared to other state-of-the-art commercial processors and has the great advantage of fully configurable internal caches and interfaces to other application specific functional blocks.

To verify this, a prototype processor system was developed, based on a highly integrated system-on-chip implemented in a Virtex-II Pro FPGA. The FPGA includes two embedded PowerPC processor cores, interfaces to a JPEG2000 compression core, memory error correction and control, and all peripheral interface logic. Additionally to the standard RTU and Spacewire interfaces other state-of-the-art high speed CompactPCI, Firewire, Ethernet, SerialATA, and Xilinx RocketIO interfaces were implemented. The system is completely scalable in processing power and power consumption to meet the demands during different mission phases. Integrated in the DPU system a complete semiconductor mass memory is established. Both types of solid state memories, volatile and non-volatile, are used to store sensor data as well as operational sequences or on-board analysis results.

Again, a radiation hardened Actel FPGA is used as system supervisor to achieve required radiation tolerance. To overcome the potential SEU sensitivity of the processor cores, both cores operate in a synchronous lockstep configuration on the same data set and the outputs of both are continuously compared. In case of a SEU induced error detected by one of the comparators, the processor cores are reconfigured and re-synchronized to a known good state. Afterwards operation is resumed with some time delay, but without any data loss [8].

Verification of the system with special attention to the protection against and recovery from SEU errors is ongoing.

To verify the usability of the Virtex-II Pro for space radiation environment, we have performed Single Event Effects (SEE) radiation testing on a commercial device in the frame of an ESA study. Both, static and dynamic tests were conducted to verify the different areas of the device: Configuration bits, Block RAM, half latches, PowerPC processors, and peripheral interfaces (e.g. Rocket I/O).

4. Future research

The further step of development in radiation tolerance is to eliminate SEU effects already by Xilinx internal design provisions, which will be supported by built-in error correction for configuration and internal memory of the next generation Virtex-4 devices.

The flexibility of in-flight reconfiguration will enable new and unique features of space systems with mission adaptive hardware functions, e.g. upgrade of on-board algorithms or functionality adaptation according to mission results, as an interesting feature for deep space probes with long mission duration. Besides the technical implementation of the upload, we focus our research on adapted system architecture to further increase the flexibility of in-flight reconfiguration and easiness of usage. To allow partial replacement or addition of IP cores without complete re-implementation and re-qualification, standardized interfaces and implementation processes are mandatory. The next step is the integration of complete networks of dynamically reconfigurable modules together with a qualified communication system within one chip in a Network-on-Chip (NoC) design. This is supported by a design flow with hierarchical, modular and incremental methodologies by use of the newest Xilinx PlanAhead software.

5. Conclusion

The state-of-the-art FPGA based approach for implementation of complex payload data processing functions is a proven solution, currently typically used for single instrument systems, but capable to support also medium and high end payload applications. With Virtex-I and II series qualified and radiation tolerant devices exist. The Virtex-II Pro series provides even more capabilities in terms of interface flexibility, data rates and processing power, but is currently restricted to devices without radiation specification. These FPGA based systems combine the advantages of both classical approaches, the speed of a hardware accelerated implementation with the flexibility of a software programmed processor system.

6. References

[1] W.J. Markiewicz, H.U. Keller, D. Titov, R. Jaumann, H. Michalik, D. Crisp, L. Esposito, S.S. Limaye, S. Watanabe, N. Ignatiev, N. Thomas. VENUS Monitoring Camera for VENUS EXPRESS. *European Geosciences Union. 1st General Assembly Nice,* April 2004.

[2] B. Fiethe, H. Michalik, C. Dierker, B. Osterloh, F. Gliem, W.J. Markiewicz, D. Titov, H.U. Keller. Miniaturized Data Processing Unit for Space Instruments. *54th Int. Astronautical Congress,* September 2003.

[3] F. Gliem, B. Gerlach. DPUs based on COTS. *On-Board Payload Data Processing Workshop*, ESTEC, September 2001, 01-4.

[4] H. Michalik, S. Wolter, M. v.d. Wall, L. Hinsenkamp, B. Penné, R. Rathje. High-rate CCSDS formatter/encoder plus IDEA encryptor as a single chip solution. *Acta Astronautica, Volume 58, Issue 12,* June 2006.

[5] S. Habinc (compilation). Suitability of reprogrammable FPGAs in space applications. *FPGA-002-01, Report ESA contract No. 15102/01/NL/FM(SC) CCN-3,* September 2002

[6] C.C. Yui, G.M. Swift, C. Carmichael, R. Koga, J.S. George. SEU Mitigation Testing of Xilinx Virtex II FPGAs. *Radiation Effects Data Workshop, ISBN 0-7803-8127-0,* July 2003.

[7] M. Otto. Vergleich kommerzieller Prozessoren für Instrumentenrechner. *Student Thesis*, TU Braunschweig, 2003.

[8] H.H. Ng. PPC405 Lockstep System on ML310. *Xilinx Application Note 564,* October 2004.