Panel Discussion:
Life Begins at 65 - Unless You Are Mixed Signal?

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Abstract

The old school of analog designers, exemplified by pioneer Bob Pease, is becoming an extinct species. But the demand for analog/mixed-signal IP blocks has never been greater, especially at 65 nm and below. Can this demand be met by using externally designed 3rd party analog/mixed-signal IP? Or is the implementation of revolutionary changes to traditional work flows and analog design processes a suitable option? Which solutions that help in increasing design efficiency are currently on the table? In the future, which side of the table will analog designers of Bob Pease's generation sit: the IP provider or the chip company? Or are their skills redundant for the 65 nm analog design challenges?

1. The New Breed Of Analog Designer - What Your Professor Never Told You About The DSM Design (N. Nandra, J. Kunkel, Synopsys)

Today, many chips are being manufactured at 90 nm, and the ramp for 65 nm design starts has been more aggressive than expected. Following close behind is 45 nm, with early versions of design rules and process parameters already available today. The goal is to achieve improvements in digital speed, power, integration density, and ultimately lower cost, but the scaling of devices has led to some interesting challenges for the analog circuit designer. In reality, the analog designer must follow the technology roadmap for digital processes that add sources of variation that can severely limit the analog circuit performance. While this evolution in CMOS technology is very beneficial for digital, this is not the case for analog circuits.[1]

The goal of our panel discussion is to state that these challenges require a new breed of analog designer that can deal with the power dissipation constraints, due to the increased leakage, device variability and model accuracy, and design methodology/tools for reliability. The important challenges and solutions will be presented.

Excellent model-to-hardware correlation is needed and in some cases trade-offs in design flexibility for accuracy by constraining device geometries are made, and model characterization structures must match recommended geometries. Close co-operation between the semiconductor foundry and EDA tool vendor is crucial to designer productivity.

In the past the designer could work with a large strong inversion region and device equations were square law based, allowing hand analysis to calculate device sizes. Today, with channel lengths as low as 40 nm and with gate oxides in the region of 20 angstroms, the analog design challenges are related to the non-linear output conductance; and this, in combination with the lower voltage gain, puts limits in the linear range of circuits.[2] Gate-leakage (due to the tunneling current through the thin oxide) mismatch exceeds conventional matching tolerances.

Increasing area does not improve matching anymore, except if higher power consumption is accepted or if active cancellation techniques are used. Also, the bipolar-like current gain for longer channel lengths is an everyday reality for these designs.[3]

Another issue is the lower supply voltages. One potential solution is to use both thin- and thick-oxide transistors. For example I/O applications such as USB 2.0 that require 5 V tolerance can be achieved by using the thick oxide devices. With these high voltage

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requirements, electro-migration checks for potential short conditions must be made. This can occur on dense arrays of conducting thin-film metallic conductors, and over time, high current densities cause these conductors to fail causing metal separation. Also adequate metal widths and checks for metal / MOS / POLY / VIA / contacts should be available from the EDA tool.

The effects of shallow trench stress (STI), negative bias thermal instability (NBTI), well proximity, contact stress, and device reliability degradation make analog circuit design challenging at the 65 nm node. The impact of these and their solutions will be discussed.

STI is a fabrication method used to isolate active areas and can cause currents to be different from simulation, and it depends on transistor location.

NBTI degrades PMOS devices progressively over time, ultimately by an increase in the threshold voltage and reduction in mobility due to negative gate bias and/or higher temperatures usually around 100 ºC. The net effect is that the PMOS current drive is degraded over time, and this can induce timing failures in digital circuits. Matched devices, like current mirrors and differential pairs, which are asymmetrically stressed, will have an additional mismatch component, in addition to mismatch from processing variations, causing additional performance degradation to the system.

Hot carrier injection degrades the performance of NMOS devices in a similar way, but through a different physical mechanism from NBTI. Unlike NBTI, HCI is a function of the electric field across the channel (i.e., from drain to source), whereas NBTI degradation is a function of the field across the oxide.

Circuit layout must be able to accommodate well proximity effects.

References

[1] Analog IP Tutorial, Lefferts, Nandra SNUG 2007

[2] Analog Circuits in Ultra-Deep-Submicron CMOS, Nauta et al. JSSC January 2005

[3] Deep Submicron CMOS and the New Era of Creativity, in Analog Design. John A. McNeill, May 2006

2. Combine today's analog IP together with Product Realization Services (M. Vanzi, Accent)

Analog designers are facing increasing challenges. The "consumerization" of the electronics market has caused a never-ending push towards often conflicting objectives, such as power, performance, cost, and time-to-market, which are all heavily affecting the analog portion of a design. In turn, analog design is quickly becoming the bottleneck of any design of nontrivial complexity, no matter how much or how little of the design is actually analog.

Market objectives are often achieved by targeting smaller technologies and non-standard options, but the evolution of design technology and tools has not yet permitted analog design to undergo the paradigm shift that digital design has achieved in the past couple of decades.

These considerations make it inevitable to base the development of new products on proven IP blocks. Reuse in IDMs is often based on the optimization of derivatives, moving among different nodes of the same technology; however, fabless companies, which do not own technology-dependent blocks internally, have to turn to the outside market.

Unfortunately, the outside market does not always offer analog IP blocks that meet the needs of the fabless industry. Analog IP is often much trickier than soft IP; and what has been proven to work in one chip will not always work in the next one. Apart from classical issues, such as quality of specs and missing or incomplete views, more subtle misbehaviors are known to happen, such as previously inexperienced leakages.

In today's designs, whenever analog is involved, it is still very risky to vary from the classical practice of "two silicon runs before going into production." Until the day that we have a more structured approach to analog design, it appears inescapable to combine today's analog IP together with design services, thereby ensuring the informed integration of a "sub-design," not a black box, and to achieve a higher level of predictability.

3. The Quality and Capability of the Design Kit is the Key Issue (H.-J. Wassener, Atmel)

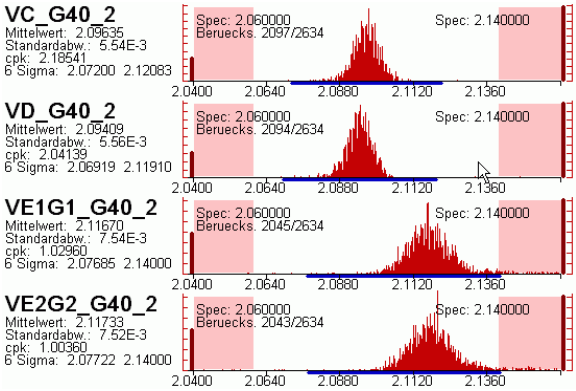
Is there life beyond 65? IP or not IP, is that the question? The answer depends on the boundary conditions and the experience, which is related to the kind of company one is working for. On the one hand there is the extreme lean company only designing IPs. On the other hand there is the classical semiconductor company with internal access to all skills needed to develop and produce ICs. This also includes developing new devices for a technology, modeling them, building design kits, having full access to possibly several wafer fabs, running wafer and final test, handling customer claims. Atmel RFA belongs to those classical companies, in former times known as Telefunken and TEMIC. Having access to all parts of a design flow it is possible to improve it, e.g. targeting better quality, optimum yield, reduced cost and faster development time.

One part of the question concerning structure size can be answered quite simply. For designs with a high content of digital blocks small structures with dimensions of 65 nm and below give a small chip size. But the drawback is the increase of cost for a mask set and the first wafer run. Assuming a first-time-right design it is only a simple calculation to find the suited technology for a given quantity of later produced parts.

The situation is more difficult if there is a larger content of analog or RF blocks. An analog design often can't use minimum structures due to RF performance and the HCI (hot carrier injection) problem reducing life time [1]. HCI occurs around a certain bias condition and can be avoided by increasing the channel length. So the down-sizing is limited especially in the case of automotive applications. Thus the actual minimum channel length for RF ICs is 130 nm.

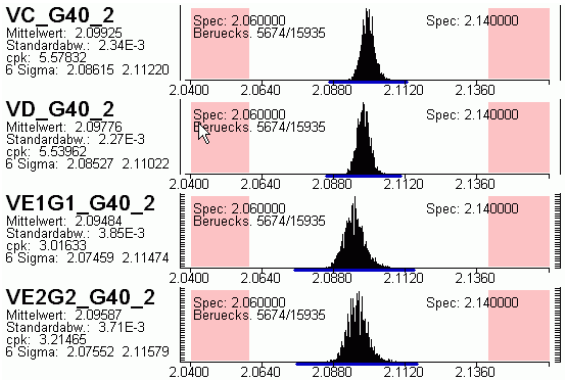
Two key targets from above, the fast development time and the first-time-right design are addressed in DETAILS [2]. The solution is that the designer is enabled to simulate exactly what later is the output of the wafer fab. This one the one hand includes that the model of a device really describes it's true behavior under all bias and voltage conditions. On the other hand all statistical effects of the fab including global and local (= mismatch) variations are known and included in the design kit.

The first step is successfully finished including devices of a bipolar technology. Two changes in parallel were necessary. One is replacing the old SGP (Simple Gummel Poon) bipolar model by an advanced and precise model, i.e. HICUM [3]. The second step is using the technology process parameters as the independent statistical input variables. This is in contradiction to the former and commonly used approach of directly taking the model parameters for that purpose, which produces simulation data garbage. This is also in contradiction to the former corner runs which describe a multi-dimensional design space which never will occur during production. Meanwhile the approach is verified, the loop is closed [4]. Two figures are attached to demonstrate this. The first one shows some test results from more than 2000 chips, designed without the aid of a statistical design kit. The standard deviation and the cpk are quite poor. Especially for the last 2 values many results are above the upper spec limit which would lead to a reduced production yield.



The second figure shows the result after optimizing the IC using the statistical design kit, thus performing a DFY (design for yield) plus DFM (design for manufacturing).

The values now are centered, standard deviation and cpk are improved.



The second step is just ongoing, is addressed to CMOS and only needs the first change, as the second change is still available in the design kit. Like the SGP the BSIM model is no longer up-to-date especially for analog and RF. It will be replaced by an enhanced EKV

3.0 model supporting the same feature set as the above mentioned full statistical and RF proven HICUM.

Coming back to the IP question there has to be differentiated between digital and RF, between using a complete IC IP or only blocks, and between using the same fab where the IP was proven or changing the fab and even the technology. If obviously no changes would be necessary for an IP, so using it as delivered, then the decision is easy. In all other cases we would have to modify the IPs and had to do this task first-time-right. In this case the decision is very difficult as long as there is no support by a fully statistical design kit as described above.

Recapitulating, the design bottleneck can't be simply solved by buying IPs from external companies as they suffer from the same bottleneck. Instead the root cause has to be fixed and this is a design kit and flow with insufficient model characterization. Introducing the technology process as root cause of statistical variations we can target reduced development cycles, mainly by avoiding redesigns. Only this approach will grant the quality of design which is necessary to reduce the failure rate towards 0 ppm.

References

[4] www.siliconfareast.com/hotcarriers.htm

[5] www.edacentrum.de/ekompass/projekte/details/

[6] Kraus, W. : PCM- and Physics-Based Statistical BJT Modeling Using HICUM and TRADICA, 6th HICUM Workshop, 2006

[7] Wassener, H.-J., Strobel, H.-J., Eichel, D., Schneider, W., Schröter, M., Wittkopf, H. :Use of a TRADICA based Statistical Design Kit in the Cadence Environment, Poster Session at Analog06

4. C-Level Design Entry and Statistical Averaging Techniques against Process Variations (R. Wittmann, Nokia)

The 65nm process node is available now for complex communication system design. It allows reaching new milestones for integrating digital signal processing units containing multi-processor sub-units. In traditional design methodologies the analog devices cannot follow the technology node scaling relevant for the digital circuit parts. One of the main threats for beyond 65nm process generations is the increasing influence of process parameter deviations on system performance and fabrication yield. Especially embedded RF- and AMS IP's in highly integrated communication systems suffer from the decreasing quality of the basic process devices and the increasing number of parasitic effects. The design gap within 65nm and beyond process technologies cannot be filled by external IP providers, as long as they are not able to address substantial design technology capabilities influencing performance, yield and reliability. The tradeoff between quality and cost puts a big question mark on the feasibility of future single chip system solutions offering a promising market success. On the other hand single chip solutions offer best power efficiency, which is relevant for high mobility. In that sense they stay extremely interesting.

New analog and RF EDA tools urgently have to offer a higher work efficiency to increase the work efficiency of the designers, who are using them. All monotonous tasks have to be automated and the urgently required innovation process of experienced designers has to be supported actively. Today the lack of productivity forces design engineers to reuse old staff in kind of panic mode, with too less time left for evaluating the new opportunities. A design engineer should again, like in the good old days, be able to spend more time on innovative engineering tasks than on fixing interface and design flow incompabilities and repeating again and again same design tasks by transferring same designs without new challenges across the process nodes.

On circuit design level new design options for 65nm and beyond exist and are waiting to be addressed. New design approaches as the Generic Engineering Model approach (GEM) allow increasing drastically design efficiency [1]. This approach allows describing the known full handcrafted design process independent from the actual process selection. All interactions (e.g. model entry, schematic entry, layout entry, testbench entry, simulator control) between a designer and a state-of-the art design platform can be described in a high-level description language. In contrast to existing approaches, GEM (Fig. 1) describes the design process itself, not the result of it. The database of a high performance analog IP has a complexity of tens to hundreds of megabytes. No reuse across process nodes is possible by only evaluating the database, since the design process stays invisible. In this approach the design result stays invisible until the model is executed in a selected process and the low level database is generated. The design process stays transparent and can be reproduced or improved in other process nodes or similar processes of other vendors. Same tools and process setups are used in traditional and the proposed GEM approach guaranteeing 100% database compatibility. Both approaches – handcrafted and GEM – are compatible to each other and can be mixed.

Experienced designers can continue to work in their trusted environment, but with improved efficiency.

Some design practices, which have in the past been skipped because of their inherent extreme high effort, may find their way back to the designers in presence of design automation. New opportunities exist on how device parameter deviations can be ruled efficiently for the coming process nodes for embedded analog and RF functions in order to achieve high yield and quality for

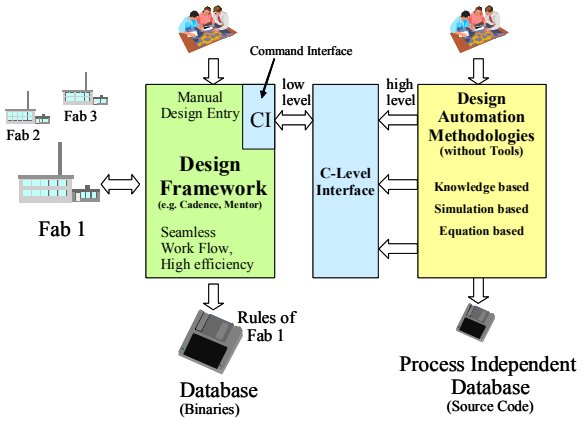


Figure 1: ***Generic Engineering Model (GEM) driven design versus handcrafted design.***

the system architecture. Some disruptive changes to traditional circuit/device design and modeling techniques are required in order to be able to address these opportunities. Example 1: It has been shown that the design principles of statistical averaging was able to keep 10 bit-linearity of a digital controlled analog potentiometer across the process nodes from 0.8µm down to 65nm in presence of increasing local parameter deviations and the adopted digital downscaling factor. It was found that statistical averaging allows improving the linearity of analog circuits by a factor of at least four [2]. So, with the use of architecture regularity and optimized averaging principles it is even possible to extend the accuracy (linearity, temperature stability) beyond the capability of laser trimming or other kinds of calibration, by making use of the parameter distribution probabilities. Example 2: It could be demonstrated that the area of state-of-the-art RF- inductors can be reduced by more than 60% when taking care of eddy currents and skin effect by using algorithmic layout shapes and structures. The layout becomes extremely complex and cannot be created in a handcrafted manner or with standard layout generators (PCELLS) anymore. The discussed design examples partly were created and evaluated in the BMBF project DETAILS.

In case of standard interfaces to the outside world external qualified analog IP's may be an interesting alternative. Key IP's for analog signal processing require a deep target system understanding in order not to waste reliability, power or cost. The full system architecture in future has to be considered for basic device and IP structures definitions.

References

[8] R. Wittmann R.; Bierbaum D.; Ruhanen P.; Schardein W.; Darianian M.: "*A unified IP Design Platform for extremely flexible High Performance RF and AMS Macros using Standard Design Tools*," System on Chip Design Languages (Extended Papers: Best of FDL'01 and HDLCon'01), ISBN 1-4020-7046-2, Kluwer Academic Publishers, Boston, June 2002.

[9] R. Wittmann, W. Schardein, R. Kakerow, J. Bahr, "Robuster analoger Schaltungsentwurf für Sub-100nm Prozesstechnologien mittels statistischer Methoden", ", GMM Fachbericht *"Analog '06 - Entwicklung von Analogschaltungen mit CAE Methoden"*, Band 196, S. 191-195, VDE Verlag, September 2006

5. Digital Self-Calibration against Process Variations *(C. Münker, Infineon)*

One of the main challenges of designing RF transceivers in a DSM CMOS technology is the larger parameter spread compared to technologies optimized for analog performance. Especially during the introductory phase of a new technology node, these parameters and their variations are subject to frequent changes which are transferred to the simulation environment only with considerable delay. In-house RF design becomes difficult under these circumstances, external RF IP development nearly impossible.

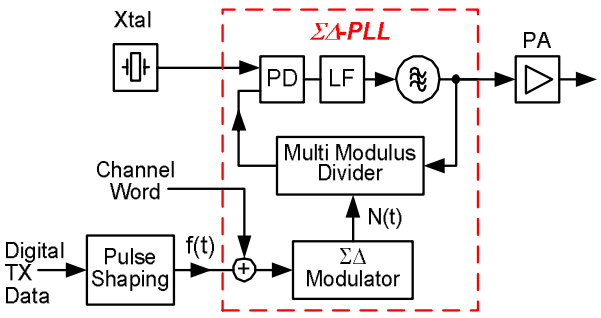


Fig. 1 Sigma-Delta modulation transmitter

The situation can be ameliorated by the high integration level of DSM CMOS technologies which enables the use of advanced DSP techniques for on-

chip calibration loops and signal correction. As a result, the optimum architecture of an RF CMOS transceiver is different from traditional BiCMOS solutions.

The digital sigma-delta modulation transmitter architecture shown in Fig 1 is an example for this trend. It operates by modulating the VCO frequency in a digital way, making this architecture inherently robust against parasitic PA feedback [3]. Additionally, the upconversion mixer which is sensitive against parameter variations and power-hungry is eliminated altogether, making this architecture the "work-horse" for frequency synthesis and modulation in DSM CMOS.

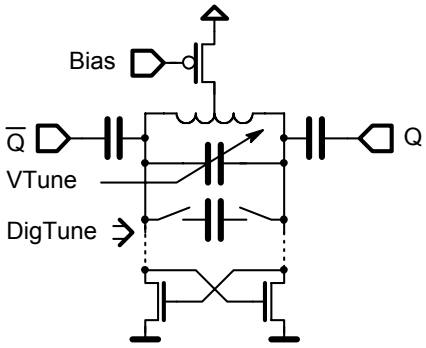


Fig. 2 VCO with digital band selection

VCOs in CMOS technologies are tuned using MOS varactors which have far more parameter spread than dedicated varactors in BiCMOS technologies, mandating a huge VCO gain to meet the required frequency span under all conditions. Automatic digital band selection (Fig. 2 and Fig. 3) achieves a much better performance by providing a wide overall tuning range and a low, controlled gain per band at the same time. This built-in self calibration (BISC) also opens up opportunities for reconfigurable multi-mode designs.

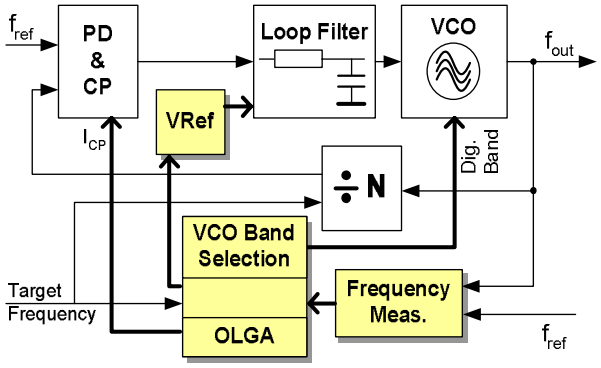


Fig. 3 Digital band selection and open-loop gain adjustment

Also shown in Fig. 3 is a method for automatic loop gain adjustment (OLGA) for keeping loop gain and bandwidth constant in spite of parameter variations [2].

Fig. 4 shows the significant reduction in open loop gain spread achieved by self-calibration.

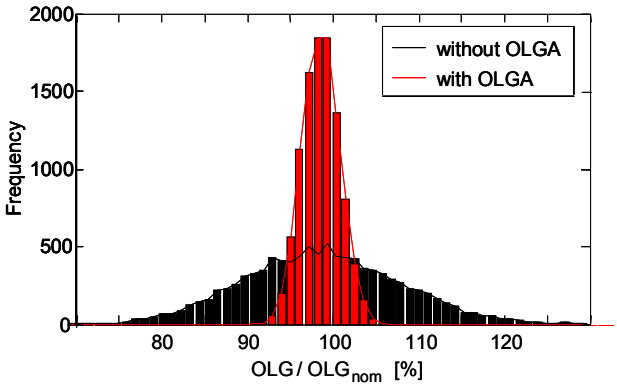


Fig. 4 Monte Carlo simulation of open loop gain before and after automatic calibration

The bad testability of embedded analog RF blocks like the VCO gives an extra edge to BISC solutions: Reading out the result of a BISC algorithm can provide a very effective Built-In Self Test (BIST) solution, reducing the number of slow RF tests.

Wrapping things up, the high integration density of DSM CMOS offers system level opportunities to overcome process parameter variations. Digital RF Built-In-Self Calibration circuits are integrated into the system to optimize overall system performance. This technique is compatible to existing design und modeling flows. Besides compensating process deviations, BISC enables the design of reconfigurable systems with minimized power consumption and production test costs.

In spite of digital calibration, high performance RF designs still require good knowledge of the process and its limitations as well as good communication between process and design engineers. This combination of system and technology know-how is an asset of Infineon Technologies as a mixed-signal semiconductor company with in-house foundry that is hard to beat by external IP.

References

[1] C. Münker, B.-U. Klepser, B. Neurauter, and C. Mayer, Digital RF CMOS transceivers for GPRS and EDGE, IEEE Radio Frequency integrated Circuits (RFIC) Symposium 2005, Digest of Papers, pp 265–268, 2005.

[2] E. Goetz et al., A quad-band low power single chip direct conversion CMOS transceiver with sigma delta modulation loop for GSM. Proceedings of the 29th European Solid-State Circuits Conference (ESSCIRC), 2003, pp. 217–220, Portugal, Sep. 2003.