Simulation Platform for UHF RFID

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Abstract

[1]*Developing modern integrated and embedded systems require well-designed processes to ensure flexibility and independency. These features are related to exchangeability of hardware targets and to the ability of choosing the target at a very late stage in the implementation process. Especially in the field of ultra high frequency radio frequency identification (UHF RFID) the model-based design approach leads to expected results. Beside a clear design process, which is applied in this work to build the required system architecture, the scope for UHF RFID simulations is defined and an extendable platform based on The MathWorks Matlab Simulink® is developed. This simulation platform, based on a multi-processor hardware target, using a Texas Instruments TMS320C6416 digital signal processor is able to run UHF RFID tag simulations of very high complexity. The highest effort is made to ensure flexibility to handle future simulation models on the same hardware target, realized by the continuous design and implementation flow of this platform based on model-based design.*

1. Introduction

In recent years model-based design became the preferred methodology for designing, modeling and simulating complex technical systems. Designs of embedded systems, like RFID tags, are often based on the development of a detailed formal system specification, whereby an expectably high effort is often spent to ensure the correctness of their specifications. In succession, the first implementation and later maintenance is usually done using traditional programming like C++, C or HDL. Divergences are expected due to putting it into affect in the chosen programming language.

[1]This project has been supported by Austrian government under the grant number 809340

1.1 State-of-the-art

To overcome the above named issues, it is desirable to derive the implementation directly from the specification that is state-of-the-art. For this several approaches are known and established in the developer's community [1], [5].
The complexity of UHF RFID simulations involve special purpose embedded systems that are carried out as embedded multi-processor systems. Two challenging tasks in such environment are considered. The first is the development of an accurate model, which follows all real requirements precisely and the second is to obtain a flexible and high performance coupling between the embedded system and the simulation model [2]. A recent study [9] presents a concept for behavioral modeling of wireless communcation devices on a case of a WCDMA transceiver. Another work [10] developes a framework for a RFID system validation with the stress on the antenna parts of the transmitter and the receiver using VHDL-AMS language.

2 System and application modeling and simulation framework for UHF RFID

In this work, we propose a simulation and modeling methodology for UHF RFID in order to support the development of integrated circuits and decreasing simulation time and further to allow more comprehensive evaluations. A robust modeling methodology for simulation of integration of the system in the application level has been developed based on a layered simulation and modeling framework. Critical aspects specific for UHF RFID have been solved on various levels of system model abstraction. The major topics are coexistence of high carrier frequency and low rate data signals in the system, modeling methodology for system integration into application layer, and real-time aspects of the HW/SW model co-simulation. Previous works discuss the aspect of model accuracy and simulation

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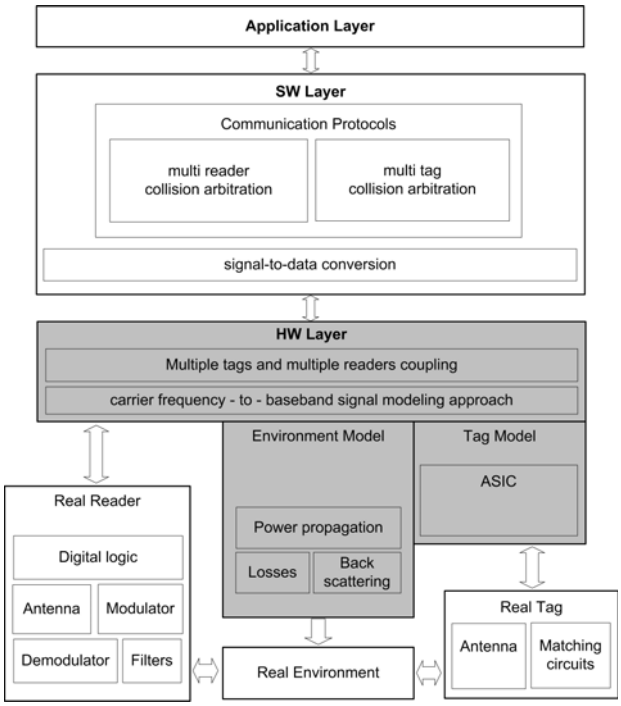

Figure 1. Framework for UHF RFID simulation

efficiency in the transition from frequency to time domain [7]. A model of an UHF RFID tag for system and application level simulation with the prime focus on the radio frequency link is presented in [6].
The modeling and simulation framework presented in Figure 1 allows creating a hardware-software-application wide model with the stress on high modularity. A simulation tool [4] has been developed based on this framework, which can be used to optimize the setup in the application area to evaluate design of hardware components and system parts of UHF RFID systems.

Hardware layer is the basic block of the whole system. It includes a robust model of UHF RFID hardware part with independent and exchangeable modules for reader, tag and environment. A possibility exists to physically connect hardware parts to the simulation model.

Software layer handles simulations of the influence of foreign subjects on the data flow and the quality of communication protocols evaluation including multi reader collision arbitration and multi tag collision arbitration

Application layer allows adapting to the above described layers to RFID application specific conditions, like e.g. warehouse or library environments bringing real-world stimuli into the simulation.

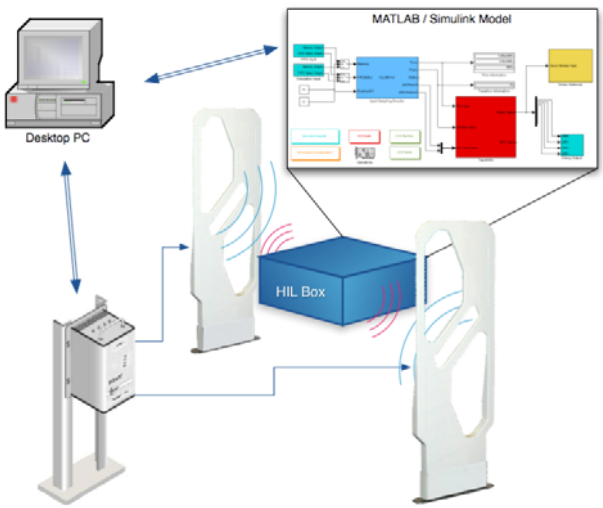

Figure 2. Proposed solution for UHF RFID system verification

The main focus of this paper is the design of a prototype that is used to simulate several UHF RFID scenarios in the real world environment, as shown in Figure 2. The target technology is less important than the extensibility for simulating complex scenarios. The use-case presented in this work is focused on the design of RFID tags, which's behavioral models are described in high-level languages embedded into a Simulink® model.

3 Design flow

Commonly, simulations are not executed in real time, they often run in powerful system environments where real inputs and outputs are also simulated. In this work the simulation is executed interacting with the real world environment, what requires it to be executed in real time. During the implementation process, the whole model of the simulation device is simulated on a PC with virtual, simulated, or already recorded input data, to determine the validation before deploying it to target hardware. At the first stage of the design simulation is not executed in real time.

3.1 Flexible simulation deployment

Models of UHF RFID tags are created in Matlab Simulink®, containing special modules to communicate with the real world environment, via hardware

interfaces. These modules are signal input, signal output and at least the simulation HW configuration. In the first instance, to implement these functionalities standard Matlab Simulink® Embedded Target blocksets are used, and customized to fit the requirements. The Simulink® models are built on the host PC with use of the Real Time Workshop Embedded Coder® and compiled with use of Code Composer Studio® to the destination platform. Code Composer Studio® communicates with the simulation DSP through an embedded JTAG emulator with an USB host interface, and deploys the simulation models. The whole process is achieved within one step, from compilation in Matlab Simulink® Real Time Workshop® until deployment in Code Composer Studio®.
The basic flow of code generation begins with designing a model containing one or more tags using Matlab Simulink® tools and adding device driver blocks to the Simulink® model. These device driver blocks are developed in this work, for providing a flexible model structure. The target compilable C or C++ code is generated from the Simulink® circuit, via Real Time Workshop® compiled and linked with hardware and DSP specific library files by Code Composer Studio®, to finally obtain the executable file. In a number of intermediate steps the code is passed through optimizers, which are configured to optimize in terms of execution speed. An extensive implementation task is adapting an existing tag model to embed in the developed architecture before running on a simulation host. The software model drivers are developed to interface with hardware modules and to provide a runtime environment to existing tag simulation models.

4 Novel simulation platform for UHF RFID

Figure 3 describes the HW module stack for UHF RFID tag simulations. The whole system is split into two main parts, one is called Signal Acquisition Unit (1) and the other is called Tag Simulation Unit (2).

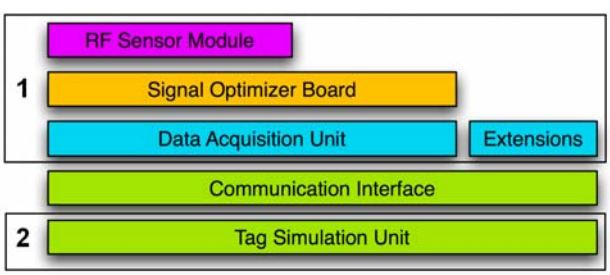

Figure 3. Hardware module stack of the simulation platform

4.1 Components

RF Sensing Unit: To retrieve information from the RF air interface an RF Sensor Module (Figure 4) is used, which is attached to the Signal Optimizer Board preparing the data for processing. The RF Sensor Module (Figure 4) is based on an analog front-end of a tag providing the signals for data detection and RF field strength level measurements and supporting the back link via a modulation. Some debug and monitoring features are implemented in the module, which considers the constraints of keeping it additionally slim and cheap to manufacture. In the first instance the antenna is a dipole antenna, trimmed for the European frequency band around 868 MHz.

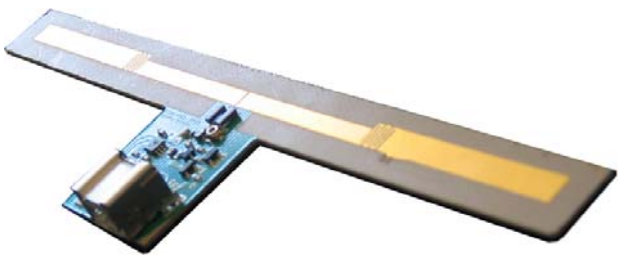

Figure 4. RF sensor module [3]

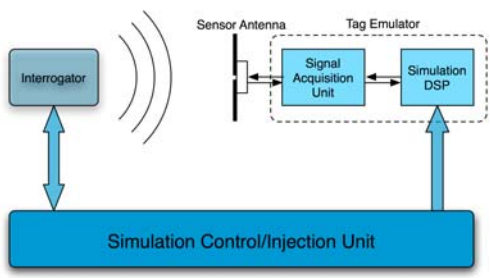

Figure 5. Data Acquisition Unit samples and modulates

Data Acquisition Unit: This module is mainly realized by an Infineon XC167 microcontroller embedded on a developer board from KEIL[2], which provides interfaces to sample RF field data and transmit it to the Tag Simulation Unit. As displayed in Figure 5 the RF Sensor Module receives and provides the RF field coverage data and demodulated baseband information to the Data Acquisition Unit. In detail, the acquired signal consists of digital protocol data and the RF field

[2] `www.keil.com` last visited on 1st of May 2006.

level information represented as analog voltage. Both are sampled by the Data Acquisition Unit and handled over to the Tag Simulation Unit.

Tag Simulation Unit: The Data Acquisition Unit is attached through an asynchronous bus interface represented by a FIFO memory to the Tag Simulation Unit, a Texas Instruments DSP Starter Kit board using TMS320C6416 DSP, where the simulation model is deployed. The simulation is compiled and deployed to the board, which uses several external interfaces for environmental coupling. In the first prototype the programming of the simulation model is achieved by the USB[3] JTAG interface embedded on the DSP Starter Kit board.

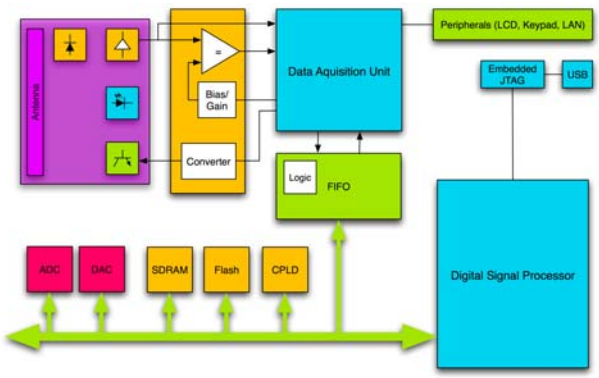

Figure 6. Block model of the HW simulation platform

Figure 6 describes the signaling on the system, beginning with the sensor antenna connected to the Data Acquisition Unit via the Signal Optimizer Board. Further the Digital-to-Analog Converter and Analog-to-Digital Converter illustrated on the left bottom side of the block diagram are not implemented in the first approach but reserved as idea for future implementations.

4.2 Performance requirements

In the RFID use-case with EPCglobal Class1 Generation2 protocol [8], communication link timing determines the requirements on the simulator performance. The maximum time allowed from the end of the interrogator data to a tag response is the maximum computation time for the simulation model, which is depending on the complexity of the model used and the number of parallel simulated tags. In Figure 7 the transmission sequence is presented, the upper

[3]Universal Serial Bus

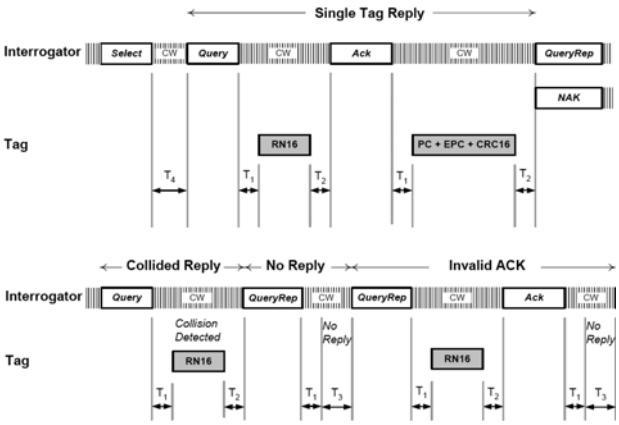

Figure 7. Link timing sequence [8]

sequence shows a single tag reply and the lower one shows a collision if more than one tag reply at the same time. The proposed simulation device is able to achieve the shortest timings or even shorter than required, also to simulate such violation scenarios. In the equations below the simulation parameter of link timing, T_1 is explained with respect to its absolute minimum and maximum values for the according link frequencies (data rates) f_{Link}:

$$\max(RT_{cal}, 10\frac{1}{f_{Link}})(1-FT) - 2\cdot 10^{-6} \leq T_1 \leq \max(RT_{cal}, 10\frac{1}{f_{Link}})(1+FT) + 2\cdot 10^{-6} \quad (1)$$

$$T_{1_{min}} = \max(6.25\cdot 10^{-6}, 10\cdot\frac{1}{640\cdot 10^3})(1-0.22) - 2\cdot 10^{-6} = 14.19\cdot 10^{-6}s \quad (2)$$

$$T_{1_{max}} = \max(25\cdot 10^{-6}, 10\cdot\frac{1}{40\cdot 10^3})(1+0.04) + 2\cdot 10^{-6} = 262\cdot 10^{-6}s \quad (3)$$

The obvious result defines the minimal response delay of 14.19 μs targeted for the simulation device. Every response below 262 μs is valid for the slowest link rate.

The maximum of RT_{cal}[4], the duration of the interrogator to tag calibration symbol, and the link pulse repetition interval, the inversion of the link frequency, is multiplied by a term including the frequency tolerance (FT) in Equation 1, which can take values from $\pm 4\,\%$ to $\pm 22\,\%$, increasing with the link frequency. The time is measured from the last rising edge of the last bit of the interrogator transmission to the first rising edge of the tag response at the tags antenna terminals.

[4]Reader-to-tag calibration: gains values from $6.25{\cdot}10^{-6}$ to $25{\cdot}10^{-6}$, based on link frequency

Further presented in Figure 7 are the times T_2, T_3, and T_4 whereby these time intervals are only of interest for the interrogator internals, instead of influencing the simulation performance.

4.3 Hardware Configurations

The system configuration developed in this work is implemented in the stack design presented in 4.1. Figure 8 shows the working hardware in a UHF RFID environment.

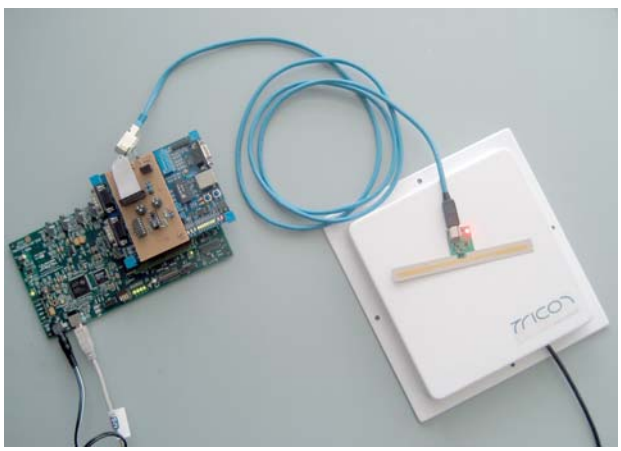

Figure 8. Development hardware in UHF RFID environment

The Data Acquisition Unit firmware is programmed into the Infineon XC167 Flash ROM and kept unchanged during simulations, whereby the simulation model code is downloaded via USB to the Tag Simulation Unit on demand, e.g. on changing models or extending functionalities.

The top most module *CISC RF Sensor Module* [3] is connected via a cable to the Signal Optimizer Board, which leads the PCB stack. The manual adjustment of the trim-potentiometer is done initially for every antenna setup, to reach optimum results. The sampling accuracy is directly related to the defined comparator level – also depending on the RF field input signal. After personalizing the settings the Signal Optimizer Board is stacked with standard 2.54 mm pinheads to the KEIL Infineon XC167 development board.

4.4 Task scheduling in the real time environment

Matlab Simulink® does not provide any methodology to perform an early performance estimation on the final target hardware. At this state any power considerations are left out, although power estimations are more and more subject of designing embedded systems. The first implementation of the UHF RFID simulation platform was based on Matlab Simulink® R14SP4. Matlab Simulink® in this version generates a massive overhead when running simulation models on an embedded target. The background timer routines are controlling the main model steps. In the generated *main* function the runtime timer is configured and interrupts are enabled. At every timer interrupt the model step is executed.
At the shortest timer interval the task scheduling routine is called which implements a deterministic rate-monotonic multitasking scheduler for a system with 3 rates. The function is called by the generated step function, hence the generated code self-manages all its sub rates. It computes which sub rates run during the next base time step. Sub rates are an integer multiple of the base rate counter. Therefore, the subtask counter is reset when it reaches its limit.
Matlab Simulink® in the version R14 SP3 only allows model of defined sampling rates. Further blocks with different sampling rates in these models are necessarily related to the fastest sampling rate by an integer multiplicand. These are realized by configuring one hardware timer and interrupt and the generated interrupt service routine, which is requested with the highest rate. Further counters determine model blocks, executed at the current time.
In the newest version of Matlab Simulink® 2006a this architecture changed to allow free definable tasks. With these it is possible to register tasks running with native clock speed of the used target hardware, so-called background *priority 0* tasks. These tasks are used for asynchronous data acquisition and are able to handle complex models with varying execution periods efficiently. The final implementation of the proposed UHF RFID real-time simulation platform is therefore based on Matlab Simulink® 2006a models.

5 Experimental results

Transmitter filters, quality of communication channel and receiver have significant influence on data detection reliability. Important measure is the comparison of RF field input signals on the simulation device to the optimized digital baseband signals and their timing information. Table 1 illustrates a measured output recorded by the simulation model in free space, which shows the sampled time values in the first four columns with their according pulse, respectively transition, information. Initially the measurement is triggered to the first negative transition to start recording, which occurred at time 28724. Columns *Time* contain times of detected pulses in μs. This example also presents a timer overflow from 64665 to 183, which does not influence the symbol detection.

Time 1	Pulse	Time 2	high	Time μs	Time μs	Symbol
		28724	low		12.45	Delimiter
29164	high	29725	low	12.775	12.225	data-0
30164	high	32222	low	50.2	12.275	RTcal
32663	high	33725	low	25.3	12.2	data-1
34163	high	34725	low	12.8	12.2	data-0
35163	high	36223	low	25.25	12.25	data-1
36663	high	37222	low	12.725	12.275	data-0
37663	high	38222	low	12.725	12.275	data-0
38663	high	39723	low	25.25	12.25	data-1
40163	high	40723	low	12.75	12.25	data-0
41163	high	41722	low	12.725	12.3	data-0
42164	high	42722	low	12.7	12.275	data-0
43163	high	43721	low	12.7	12.325	data-0
44164	high	44721	low	12.675	12.3	data-0
45163	high	46223	low	25.25	12.275	data-1
46664	high	47221	low	12.675	12.325	data-0
47664	high	48220	low	12.65	12.35	data-0
48664	high	49220	low	12.65	12.35	data-0
49664	high	50220	low	12.65	12.35	data-0
50664	high	51221	low	12.675	12.325	data-0
51664	high	52221	low	12.675	12.325	data-0
52664	high	53220	low	12.65	12.35	data-0
53664	high	54220	low	12.65	12.35	data-0
54664	high	55219	low	12.625	12.4	data-0
55665	high	56220	low	12.625	12.35	data-0
56664	high	57220	low	12.65	12.35	data-0
57664	high	58219	low	12.625	12.375	data-0
58664	high	59220	low	12.65	12.35	data-0
59664	high	60219	low	12.625	12.375	data-0
60664	high	61219	low	12.625	12.4	data-0
61665	high	62219	low	12.6	12.425	data-0
62666	high	63219	low	12.575	12.425	data-0
63666	high	64220	low	12.6	12.375	data-0
64665	high	183	low	25.1	12.4	data-1
629	high	1684	low	25.125	12.375	data-1
2129	high	2683	low	12.6	12.4	data-0
3129	high	4183	low	25.1	12.375	data-1
4628	high	5182	low	12.6	12.4	data-0
5628	high	6682	low	25.1	12.425	data-1
7129	high	8183	low	25.1	12.4	data-1

Table 1. Recorded field data and computed symbols

The overall accuracy in these results is good. Major statistical measures are presented in Table 2 showing a good match on transmitted and received data. For measurement improvements the signal pre-processing can be further calibrated automatically according the modulation depth.

6 Conclusion

This work establishes the base architecture for UHF RFID tag simulations. In the implementation one single tag simulation is targeted, but the system architecture is designed to handle multiple tag simulations of different complexities. The process of compiling the model in Matlab Simulink® Real Time Workshop® is done in one batch. A framework for UHF RFID systems is presented, where customized models are embedded and simulated, with only few restrictions. Recent work is focusing on advanced DSP architectures enhancing multiple tag simulations and virtual mapping of multiple tag models onto one physical RF sensor antenna to further allow simulations of large tag populations.

	Transmitted		Detected	
Time μs	Data-0	Data-1	Data-0	Data-1
Median	25	37.5	25	37.5
St. dev.	0.000	0.000	0.014	0.015
Min	25	37.5	24.975	37.475
Max	25	37.5	25.025	37.525

Table 2. Data detection quality measures

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