Circuit-Level Modeling and Detection of Metallic Carbon Nanotube Defects in Carbon Nanotube FETs

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Abstract

Carbon Nanotube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance, very dense and low power circuits. The core of a CNTFET is a carbon nanotube. Its conductance property is determined by the so-called chirality of the tube; chirality is difficult to control during manufacturing. This results in conducting (metallic) nanotubes and defective CNTFETs similar to stuck-on (SON or source-drain short) faults, as encountered in classical MOS devices. This paper studies this phenomenon by using layout information and presents modeling and detection methodologies for nano-scaled defects arising from the presence of metallic carbon nanotubes. For CNTFET-based circuits (e.g. intra-molecular), these defects are analyzed using a traditional stuck-at fault model. This analysis is applicable to primitive and complex gates. Simulation results are presented for detecting modeled metallic nanotube faults in CNTFETs using a single stuck-at fault test set. A high coverage is achieved (∼98%).

Keywords: Carbon Nanotube, CNT, CNTFET, Defect Modeling, Fault Detection, Nanotechnology

1 Introduction

Since their inception in 1991, carbon nanotubes (CNT) have been the subject of extensive research [1]. A carbon nanotube is a hollow cylinder made of one or more layers of carbon atoms arranged in a honeycomb lattice form. A nanotube with one layer of carbon atoms is referred to as Single-Wall (SWCNT), while those with multiple layers are called Multi-Wall (MWCNT).

Theoretical and experimental research has revealed the unique electrical features of a SWCNT, such as the ability to act as both a semiconductor and a metal (conductor) [2]. Semiconducting SWCNTs have been experimentally used to build electron devices similar to Metal Oxide Semiconductor Field Effect Transistors (MOSFET). These devices are generally known as CNTFET [3, 4] (or TUBEFET [5]). CNTFETs have shown excellent electrical properties including high transconductance (i.e. the ability to efficiently convert voltage into current) and high on/off current ratio (nearly optimal switching). Figure 1 shows the cross-section of three common CNTFET devices known as *back-gated* and *top-gated*.

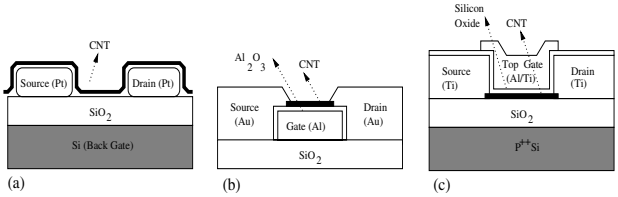

Figure 1. CNTFET: (a) Back-gate [5] (b) Back-gate [6] (c) Top-gate [7]

1.1 Contribution

The manufacturing of CNTs is challenging and they are prone to certain defects unique to this technology. This paper presents modeling and detection for a physical defect when CNTFET devices are used for circuit implementation. This defect appears when the underlying CNT in a CNTFET is always conducting, i.e. it is metallic (m-type) rather than semi-conducting (s-type). CNTFETs constructed using metallic CNTs show a behavior as *stuck-on* (SON), i.e. similar to the *source-drain short* defect in conventional CMOS circuits. For a circuit made of CNTFETs, we show the following features:

- All SON faults due to metallic carbon nanotubes can be modeled by *single stuck-at faults* (SSF), the location and the type of the SSF are determined.

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- The presence of reasonably sized complex gates does not impact the proposed model.

By combining these two novel contributions, a single metallic CNT defect in a CNTFET-based circuit (made of primitive/complex gates) can be modeled by a SSF and detected by the corresponding SSF test. The ability to detect such defects in a logic testing environment is particularly useful for future highly dense CNTFET-based circuits when complex current measurement instrumentation fall short of the necessary resolution.

The rest of this paper is organized as follows: Section 2 presents a brief review of CNTs and the issues associated with manufacturing and the presence of metallic CNTs. Section 3 presents integration and circuit implementations using CNTFETs and details the effects of metallic CNT defects that lead to stuck-at behavior in logic gates. Section 4 presents an approach for detecting metallic CNT defects using stuck-at tests and tools. Section 5 presents experiments and results for verifying the suitability of stuck-at test sets for detecting metallic CNT defects. Section 6 concludes the paper.

2 Review of CNT

The conductance properties of SWCNTs is mostly determined by the diameter and the angle of the atom arrangement along the tube. As shown in Figure 2, the graphene sheet is conceptually cut along a *chiral* vector; it is then wrapped along the cut to form the CNT. The chiral vector $\vec{C}$ is specified in terms of the unit vectors $\vec{V_1}$ and $\vec{V_2}$ as

$$\vec{C} = n \cdot \vec{V_1} + m \cdot \vec{V_2} \quad (1)$$

where n and m are integers. It is known that if $|n - m|$ is divisible by 3, then the tube is metallic (m-CNT); else, it is semiconducting (s-CNT) (when $m = n$, the CNT has a very small bandgap ($\sim$0.005eV) and can be effectively classified as metallic type [3]). For example CNTs with $(n, m) = (4, 4)$ or $(n, m) = (5, 2)$ are both metallic as shown in Figure 2. Moreover, CNTs with $(n, m) = (3, 2)$ or $(n, m) = (5, 6)$ are semiconducting.

Chirality control is the process of controlling chiral vector $\vec{C}$ in order to grow CNTs with specific electrical properties. To our best knowledge, chirality control is very difficult with current technology for mass production of CNTFETs, even though techniques for diameter controlled synthesis of CNTs are available [8]. Chirality and diameter of a CNT are related by

$$d = \frac{|\vec{C}|}{\pi} = \frac{a\sqrt{m^2 + n^2 + mn}}{\pi} \quad (2)$$

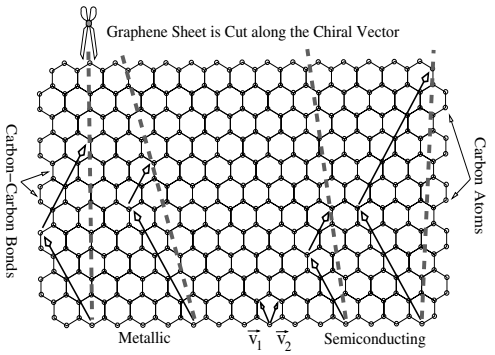

Figure 2. Chirality in a CNT

which promises the possibility of chirality control through the control of CNT diameter ($a = |\vec{V_1}| = |\vec{V_2}|$). For example, in *chemical vapor deposition* (CVD) based CNT synthesis, a nano-particle (such as Nickel) is used as catalyst to grow the nanotube. Engineering of the nano-particle and the growth process can control the features of the CNTs [9]. The CNT diameter has a sharp (narrow) Gaussian distribution, but some m-CNT defects are expected to occur due to the tails (out of 3σ) of the Gaussian leading to defective CNTFETs. This highlights an extra source of SON faults in CNTFET-based circuits, we present a minimal effort technique for modeling and detecting such defects.

3 Metallic CNT Defects

A (metallic) m-CNT used in a CNTFET device is always conducting, independently of the electric field applied by the device gate. The CNTFET source and drain are connected together and therefore, a short exists. Similar defects can be present also in conventional CMOS; they are generally known as SON (Stuck–ON) fault and modeled under the more general category of *bridging faults* (BF). It is known through several studies that more than 40% of conventional CMOS defects can not be modeled by SSF. The first contribution in this work is that, *all m-CNT defects can be modeled by SSFs* for a particular layout style of every gate (primitive or complex) in the circuit netlist. For a given cell, different layouts can be generated [10] and several works have addressed the optimal design of cell layouts in terms of area and performance [11, 12]. Optimal cell layouts are commonly produced using the *line-of-diffusion* style in which two lines of diffusion are used for implementing the pullup and pulldown transistor networks. This style uses the diffusion itself for inter-transistor source and drain contacts (i.e. the so-called *diffusion abutment*), therefore significantly reducing the layout area.

Figure 3 (a) shows a generic line-of-diffusion layout with only two semiconducting areas for the CMOS design of Fig-

ure 3 (b). These lines are replaced by CNTs (diffusion) in CNT-based CMOS (conventional CMOS). The top (bottom) line implements the pullup (pulldown) transistor network(s). The output line is conditionally connected to the supply or ground lines (but not both) and its condition is determined by the inputs. The top (bottom) line is always connected to supply (ground) in at least one point. The output line is always connected to both top and bottom lines in at least one point. This generic layout will be later used for SON fault analysis in conventional and CNT-based CMOS.

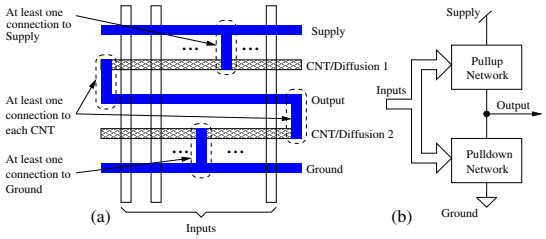

Figure 3. (a) Generic Line-of-Diffusion layout style (b) CMOS design style

3.1 Defect Analysis

A novel analysis for modeling the effect of m-CNT defects in a CNTFET-based cell is presented. To our best knowledge, such an analysis has not been presented before. In conventional CMOS, a SON fault is often caused by *missing polysilicon* defects. Missing polysilicon can cut a MOS device lengthwise, causing the underneath diffusion area to connect the source-drain of the MOS (independently of the gate voltage, i.e. a SON has occurred). Additionally, a polysilicon transistor cover must stretch beyond the diffusion. If the stretch is not sufficiently long, process variations or mask misalignment can cause a diffusion cover loss and a SON fault will appear. Figure 4 shows the mask layout of a MOS device and the aforementioned defects.

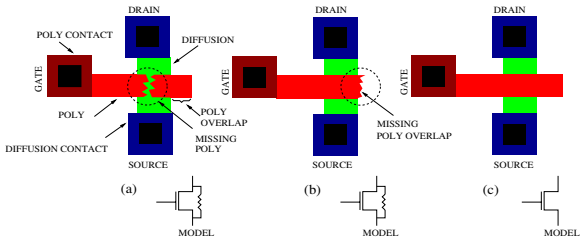

Figure 4. Possible SON scenarios in conventional CMOS: (a) Missing poly (b) Missing poly overlap (c) No defect

In CNT-based CMOS, this defect mechanism is different: while diffusion is naturally semiconducting in a conventional MOS device, in a CNTFET the semiconducting property of a CNT is not guaranteed and can cause SON faults. To analyze the outcomes of this phenomenon, the CNT-based CMOS layout must be studied as shown in Figure 3 (a): when the top (bottom) CNT is metallic in a CNT-based CMOS, the output will be connected to supply (ground) independently of the inputs because the output is always connected to the top (bottom) CNT in at least one point and that CNT is always connected to supply (ground) in at least one point. This results in a stuck-at-1 (0) at the output of the CNT-based gate. Therefore, a single m-CNT in a CNT-based CMOS gate is modeled by a SSF at the gate output.

For designing line-of-diffusion layouts, transistor networks are represented by a graph in which each transistor is mapped to an edge and its source and drain to two vertices. The edges are labeled by input lines. The graph is undirected as transistors are bidirectional switches. An *Euler* path in either the pulldown or pullup graphs guarantees a line of semiconducting area for that network. Its existence in both graphs[1] is sufficient for the validity of the proposed model. If the two paths have the same edge labeling, the input line order is preserved for pullup and pulldown transistor networks but this is not a necessary condition for two (and only two) lines of semiconducting areas. We examine the graph representation of primitive and reasonably sized complex gates and show that their transistor graphs have an Euler path.

3.2 n-Input Primitive Gates

Figure 5 (a) and Figure 5 (b) show n-input NAND and NOR transistor lists and the corresponding graph representations. Both graphs have an Euler path (the paths are marked on the graphs). $n = 2k + 1$ (i.e. odd) is assumed in Figure 5 (b); this does not affect the validity and generality of the proposed model. For $n = 2k$, the last edge in the parallel subgraphs will return to the vertex corresponding to the output node (rather than the supply (ground) vertex). Hence, the proposed model is applicable to primitive gates in a CNT-based cell library. The layouts are shown in Figure 5 (c). Both layouts show two lines of diffusion that for CNT-based cells, are replaced by two CNTs. Among them, a m-CNT will connect the output to either supply or ground, thus creating a stuck-at-1/0 fault at the output.

3.3 Complex Gates

A complex gate is a direct implementation of a multi-level (> 1) gate netlist in the layout. Complex gates are

[1] Dual Eulerian Graphs.

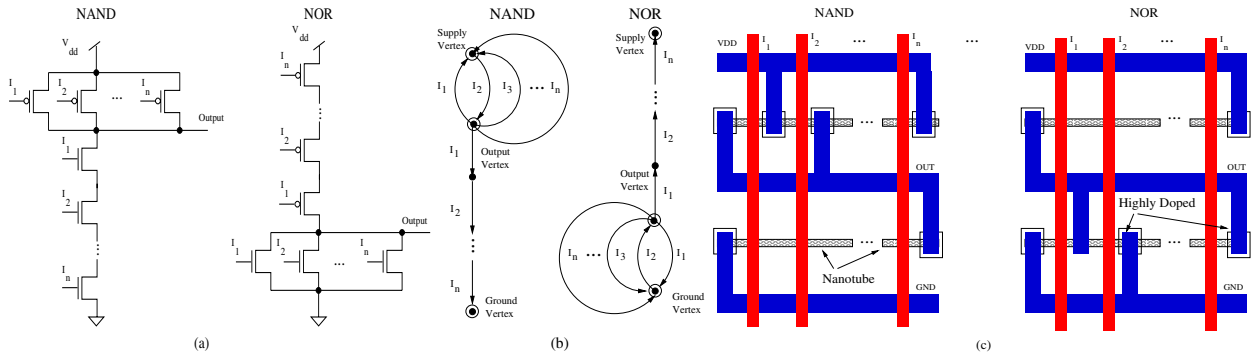

Figure 5. n-input primitive gates: (a) Transistor list (b) Graphs (c) Layouts

not frequently included in cell libraries due to their specific nature, but they allow for a more compact layout. In this paper, the depth of a complex gate is limited to two (also called AND-OR-INVERTER/OR-AND-INVERTER gates, AOI/OAI), because as found in practice, higher level circuits are too specialized for inclusion in a general purpose cell library. For such complex gates, we show that the cell layout is implementable by two lines of diffusion, i.e. there is an Euler path in the circuit graphs. This guarantees that a single m-CNT produces a stuck-at value at the output.

The necessary and sufficient condition for the existence of an Euler path in an undirected connected graph, is to have either none, or two vertices with an odd degree (the degree of a vertex is the number of edges incident on it). Consider the graph representation of either transistor networks. The complex gate is 2-level, so the graph is a parallel (serial) collection of serial (parallel) edges, as shown in Figure 6. There are P parallel (serial) subgraphs; the subgraphs are denoted by $\{G_1, G_2, \cdots, G_P\}$, where each subgraph G_i is a serial (parallel) collection of B_i branches for the pulldown (pullup) networks in Figure 6 (a) (Figure 6 (b)). For the pulldown network, excluding the terminal vertices, every vertex in the graph has a degree of 2, i.e. an even degree. Both terminal vertices have the same degree given by P. If P is odd, then the graph has two vertices with odd degree; if P is even, then the graph has no vertex with odd degree. Therefore, the graph has either none or two odd degree vertices, i.e. it has an Euler path.

For the pullup network, we can rearrange the serial subgraphs such that all subgraphs with an odd number of parallel edges (x subgraphs) are at one end of the graph and the remaining (if any) subgraphs at the other end. This can be done by a permutation of the serial subgraphs[2], $\pi()$. The vertices of the new graph are $V_{\pi(1)}, \cdots, V_{\pi(P+1)}$ with degrees $B_{\pi(1)}, B_{\pi(1)} + B_{\pi(2)}, \cdots, B_{\pi(P-1)} + B_{\pi(P)}, B_{\pi(P)}$. As all subgraphs $G_{\pi(1)}, \cdots, G_{\pi(x)}$ have an odd number of edges, then $V_{\pi(1)}$ has an odd degree and all vertices $V_{\pi(2)}, \cdots, V_{\pi(x)}$ have even degrees (the sum of two odd numbers of edges results in an even number as total number of edges). As all subgraphs $G_{\pi(x+1)}, \cdots, G_{\pi(P)}$ have an even number of edges, therefore $V_{\pi(x+1)}$ has an odd degree (corresponding to the sum of an odd number and an even number of edges) and $V_{\pi(x+2)}, \cdots, V_{\pi(P+1)}$ all have an even degree (as the sum of two even numbers of edges). Therefore the graph has two odd degree vertices, $V_{\pi(1)}$ and $V_{\pi(x+1)}$. If all subgraphs have even number of edges, $x = 0$, i.e. the graph has no odd degree vertices. Therefore, the graph has either none or two vertices with odd degrees, i.e. it has an Euler path.

[2]This is allowable due to the exchange property of AND/OR logic operators.

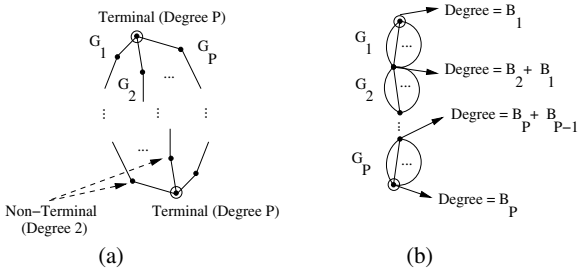

Figure 6. 2-Level complex gate transistor graphs: (a) Pulldown (b) Pullup

4 Detecting Metallic CNT Defects

It is pointed out that at least 5% of BFs can not be detected by a SSF oriented test set in conventional CMOS as BFs can cause intermediate logic values (i.e. non logic). For example, when a BF exists between the source-drain of the PMOS device in a INV gate (i.e. PMOS is SON) and the input is 1, then the output is neither 1 nor 0, but its value depends on the relative strength of the transistor on-resistance. These intermediate logic values imply a supply-

	Stuck-At Faults (SSFs)			m-CNT Modeled Faults		
Benchmark	Count	Detectable	Coverage	Count	Detectable	Coverage
s5378	4603	4563	99.1310%	5558	5491	98.7945%
s9234	6927	6475	93.4748%	11194	10569	94.4167%
s13207	9815	9664	98.4615%	15902	15792	99.3083%
s15850	11725	11336	96.6823%	19544	19273	98.6134%
s35932	39094	35110	89.8092%	32130	29282	91.1360%
s38417	31180	31015	99.4708%	44358	44282	99.8287%
s38584	36303	34794	95.8516%	38506	36698	95.3046%
c432	524	520	99.2366%	320	317	99.0625%
c499	758	750	98.9446%	404	404	100%
c880	942	942	100%	766	766	100%
c1355	1574	1566	99.4917%	1092	1092	100%
c1908	1879	1870	99.5210%	1760	1758	99.8864%
c2670	2747	2630	95.7408%	2538	2467	97.2025%
c3540	3428	3291	96.0035%	3338	3237	96.9742%
c5315	5350	5291	98.8972%	4614	4612	99.9567%
c6288	7744	7710	99.5610%	4832	4815	99.6482%
c7552	7550	6970	92.3179%	7026	6772	96.3849%

Table 1. Detection of SSFs and m-CNT Modeled Faults using a SSF test set

to-ground path, causing an extra current flow that can be sensed through an appropriate *current supply monitor* (or CSM)[3] for detection of these faults.

As for the difference of 35% between modeling and detecting BFs using SSF tests, one concludes that a portion of BFs cause a logic discrepancy in the circuit that can be activated and propagated to the outputs using the SSF tests. This suggests the application of a SSF test set for the detection of BFs such as SONs. In [13], SSF tests are used in a CSM environment and a BF coverage of $\sim 90\%$ is obtained on average for the ISCAS85/89 benchmark circuits. Depending on the gate types in the cell library and the design style pursued for a given circuit, the effectiveness of SSF tests for detecting BFs (and particularly SONs) varies. For example, if the cell library is limited to only primitive gates (i.e. no complex gates), a SSF test set covers all intra-gate BFs (including SONs) using CSM [13].

CSM is possible in CMOS style because the power supply current remains low during the steady state (when the inputs and outputs are stable); the current is essentially the aggregate leakage currents of all devices. However, as circuits become highly integrated and devices are being scaled down, the difference between steady state current and the excessive current due to a supply-ground path decreases, thus implying a greater difficulty in current measurement and judgment on the pass/failure outcome of the test. The second contribution of this work is that, *single m-CNT defects can be detected by the modeled SSF test in a logic testing environment rather than relying on a CSM*.

[3] Also known as IDDQ testing.

5 Simulation Results

In the evaluation pursued in this paper, the netlists of ISCAS85 (names begin with 'c') and the full-scan version of the seven largest ISCAS89 (names begin with 's') benchmark circuits are bound to cell libraries made of line-of-diffusion layouts. A metallic CNT fault list is compiled for each circuit by selecting one (and only one) CNT and replacing it with a m-CNT. Fault simulation was performed for the fault list using SSF test sets; the percentage of detected faults in the metallic CNT fault list is then found. Table 1 shows the number of m-CNT modeled faults and the percentage detected by the SSF test set. The SSF tests used in this evaluation are given by the widely used set of *dynamically compacted test vectors* from MINTEST [14].

All simulations are performed at switch level, i.e. at a level between SPICE and digital logic. SPICE simulation is very time consuming and does not provide extra information; logic simulation does not consider the switching behavior of CNTFETs within a cell. SSFs are collapsed using an equivalence method. The subset of SSFs that model m-CNT defects are not collapsed. The number of m-CNT faults is equal to twice the number of logic gates in the circuit netlist (in this table, all m-CNT fault counts are even numbers). This is due to the condition by which each gate has only two CNTs (due to the line-of-diffusion layout style), each CNT can be metallic/semiconducting. The m-CNT coverages are not necessarily 100%; this is expected

as some of the SSFs are redundant and therefore they are not detectable (i.e. the m-CNTs modeled by these SSFs are also not detectable). This is not a problem in practice as these m-CNTs cannot be activated and propagated to the outputs at the same time, i.e. they do not change the normal operation of the circuit[4].

6 Conclusion

This paper has studied a particular defect that is unique to CNTFET-based integrated circuits, i.e. when used for implementing a CNTFET, the CNT is metallic rather than semiconducting. It presents a technique that relies on the physical design of layouts for CNTFET-based cells. Using a graph model, it has been shown that single m-CNT defects can be modeled as SSFs and detected by the application of a SSF based test set. Experimental results have been presented for the evaluation of the proposed technique; these results have confirmed that on average, $\sim$98% m-CNT defect coverage can be achieved over all benchmark circuits.

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[4] Redundant faults can however mask other faults, this is not an issue due to single fault assumption.