

Portable Multimedia SoC Design: a Global Challenge

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Abstract - The intrinsic capability brought by each new technology node opens the way to a broad range of system integration options and continuously enables new applications to be integrated in a single device to the point that almost everything seems possible.

In reality the difference between a successful design and a failure resides today more than ever in the ability of the design team to properly master all the critical design factors at once. In essence, today's System on Chip design represent a multidiscipline challenge that spans from Architecture through Design to Test and finally mass production.

SoC design for portable applications has to cope with very unique constraints that normally greatly challenge the ability of an organization and most of the times of an entire Company to fully master its industrialization capabilities and pushes concurrent design to new limits.

In the end, only a well thought out Architecture followed by best practices design techniques with a high level of understanding of the manufacturing constraints and excellent logistics can result in a device that can be produced in the volume required by the cell phone industry today.

This paper will try to capture how these challenges have been addressed to design the family of Application Processing Engines named Nomadik™. The paper will specifically focus on the third generation device labeled STn8815S22 where the integration capabilities of silicon technology have been pared with those of System in Package design to provide an extremely compact and effective System on Chip for portable multimedia applications.

An overview of the main success factors and challenges will be presented driving the reader from the Architecture conception through the chip industrialization. Both Silicon design and packaging design will be illustrated, highlighting those techniques that made this incredible product a reality.

I. Introduction

Since the term System on Chip has been coined the crazy loop between finer silicon geometries and integration of new features on single die has possibly gained speed.

It is harder and harder to say whether each new product generation demands for the latest silicon technology node because of the set of features to be implemented or rather that products become richer in features because of the extremely huge capacity and density of today's available silicon technologies. What is though sure is that, either way, the job of the Design Teams put around such SoC challenges is increasing in complexity faster than the product complexity itself and it is seldom properly supported by an adequate EDA solution.

Overall the different speed at which product development
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time shrinks and new EDA environment can be qualified and introduced is adding another dimension of complexity and risk on the Design Team which is deemed to continuously play on a moving ground. So much for the goal of any R&D organization that should strive for predictability and reasonable stability of its design environment and practices.

In front of all the forces that inject complexity into the picture, STMicroelectronics has planted the seed of simplicity in its architecture definition and design practices to cope with the challenges of the Nomadik™ Multimedia Application Processing Engine family as it is presented in the following paragraphs.

Wherever helping the explanation, reference to the STn8815S22 [1] SoC is used. STn8815S22 is the third generation of Nomadik™ Multimedia Application Processing Engines packaged together with its FLASH and DDR type master storage memory.

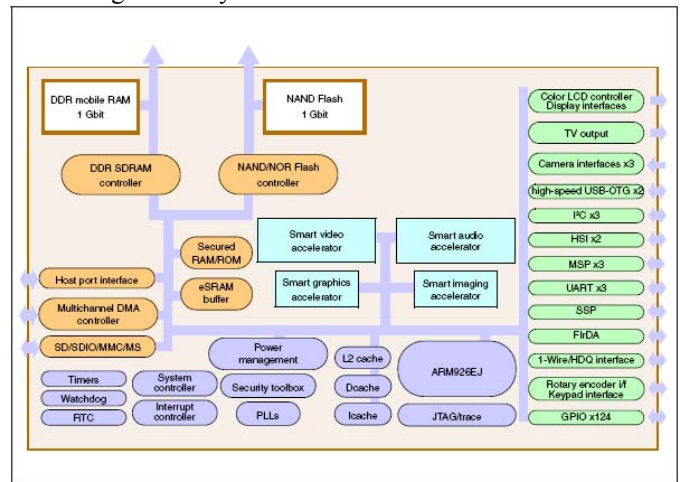


Figure 1 - STn8815S22 block diagram

II. Architecture in Nomadik™

Start it simple to keep it simple. This is a key contribution of and underlining rule guiding the architecture definition of all the components inside the Nomadik™ family.

In fact, the ability to run high performance Multimedia Applications on a battery does not call for a straightforward solution in a natural way. Nomadik™ product family addresses especially the requirement of selective and variable levels of performance on a battery through a sophisticated multiprocessing structure standing on a central processing unit and a set of Smart Accelerators implementing Digital Signal

Processing for the specific Video, Imaging, Audio, and Graphics functions.

Yet the clean way in which bus interconnect and memory hierarchies have been defined as well as the clean cut between the different components building the system and a clear protocol for them to co-operate represented one of the key success factor in the design of the STn8815S22.

The massive set of models built around the Nomadik™ devices paid a fundamental contribution to the simplicity of implementation and predictability of results. TLM and Bit true models provide both the tools for the chip conception as well the environment to verify the HW and SW elements of the SoC.

As a closing highlight of the benefits of the selected architecture, none of the Nomadik™ SoC's had the luxury to complete design with the same specifications decided at the beginning of the project. STn8815S22 has registered a few hundred change requests in the course of its design life. Design practices at all levels strongly contributed to making this possible, but once again a clean and simple architecture made it simpler and practical and allowed the introduction of new HW features late in the design cycle.

III. Design in Nomadik™

Designing for Performance under huge Power Consumption constraints do not leave much flexibility. A conventional RTL design capture has been used to achieve the targets of the device. In this case, as it will be repeated several times in the course of the article, the human factor, i.e., the ability and preparation of the engineers working on the project has made the difference.

Physical Design of the chip has for sure been a big and interesting challenge. The need to meet aggressive performance targets while shooting for minimal area and power has forced the use of available tools in innovative and creative ways. Several iterations and refinements of constraints as well as scripting have been necessary to complement what the EDA tools could provide. In several occasions the introduction of R&D versions of the EDA tools has been made necessary to either cope with the complexity of the chip or some specificity introduced by extremely aggressive power containment techniques. This has demonstrated how important it is to have solid and trustworthy relations with your EDA vendors: their R&D involvement and quick reaction times would have been impossible otherwise.

STn8815S22 is making broader use of power islands compared to previous Nomadik™ generations. This technique that allows a flexible and independent management of the supply of different portion of the SoC has been one of the most critical design constraints to cope with in the device. This design structure introduced to maximize power efficiency of the SoC depending on its active use case and configuration can become a nightmare at physical implementation time. Here again co-operation with STMicroelectronics' central research functions as well as with our EDA vendors has lead to the definition of a design flow and design practices that allowed us to successfully build the chip.

A massive use of Hard Macro for the critical IP's of the design has further contributed to simplify the problem and find the right trade offs between area efficiency, power, circuit

speed, and speed of design. Chopping the design in manageable pieces has had a positive impact not only on the Physical Design, but on all the other aspects of the SoC build up, there including specifically verification.

Design for Manufacturability and Test has been another area requiring a great investment in techniques and expertise. The huge amount of memories in the device, the large number of sequential elements, and their being distributed on different supply domains made it necessary to resort to using the known tools and techniques in a different way. Especially the power islands partitioning required effort and attention in the scan stitching as well as in the overall scan definition to avoid issues of IR drop on ATE.

Clock Tree Synthesis is the start of a painful process in most of the complex SoC like Nomadik™. Here again Power Islands and Hard Macro's on top of the natural complexity of the STn8815S22 raised the bar significantly compared to the previous generation of the SoC. Aggressive techniques exploiting preferential routing, useful skew, scripting, dedicated library has made the trick.

IV. Verification in Nomadik™

Verification has been on the critical items list of the industry for as many years as design of chips exist. The increasing complexity of the devices generation to generation is intrinsically moving the challenge of verification to new highs every SoC revision. Exhaustive verification of complex SoC's like Nomadik™ is becoming almost and oxymoron. Yet techniques and tools that reduce the risk of design faults and unwanted side behaviors exist.

SPECMAN has been the backbone of the Nomadik™ SOC's verification strategy from the beginning. The library of tests is enriched at each generation and provides a robust verification environment.

This paired with Formal Proof techniques used at each stage of refinement of the design capture and physical implementation stages can be categorized as the HW oriented verification environment exploited in the design of the STn8815S22.

Yet alone they are not sufficient. Nomadik™ solution is an optimized balance between HW and embedded SW. It is unavoidable and natural that a considerable amount of embedded SW becomes part of the verification suite of the SoC. This though introduces on the other hand the need to have an early prototype of the SoC available and in a format that can be put in the hands of a SW Engineer.

Nomadik™ has selected a dual path approach to this side of verification to provide different levels of debug ability and co-operative tools between the SoC design team and the Embedded SW design teams. The SoC mapped on Palladium Emulators has been complemented by an FPGA based prototype to serve the verification need and to allow concurrent SW development at same time.

The ability to expose the SoC design to Embedded SW developers so early in the design process allowed having a massive number of indirect test patterns exercised on the design as well as spot early enough in the SoC design and industrialization phases opportunities to improve the speed and easiness of programmability of the STn8815S22. A more than rewarding return for the investments in prototyping.

V. Validation in Nomadik™

Prototypes validation is the time design team finally confronts the truth. All assumptions, uncertainties, trade-offs and related risks can be finally measured and matched against actual silicon.

Design time needs to be shortened for time to market reasons at every generation and leaves shorter and shorter time for proper modeling and at times for getting a thorough understanding of all the new physical effects brought by the new silicon geometries. It is not obvious that EDA platforms and libraries fully match the actual behavior of the silicon especially for the designs that first use a newly introduced technology.

Nomadik™ SoC's has been traditionally the type of products in STMicroelectronics to utilize the latest technology available even in a pre-qualification stage. As a consequence, Nomadik™ design teams have developed a special sensitivity to the way to cope with this major uncertainty and consequently applied them during the design of the STn8815S22. Just taking *enough margin* is not a valid paradigm anymore. Too many factors play a role in the final silicon behavior and force designers to grow an understanding and mastering of the problem with a different sensibility.

Prototype Validation provides a set of tools to finally correlate simulation results with actual silicon and enable a set of silicon process tunings and silicon process re-centering actions to optimize both speed and power of the devices. The use of corner samples of the device, i.e., silicon that is pushed by construction into corner conditions of process parameters, is fundamental in this phase. Such material tested in extreme conditions of Temperature and Voltage provides all the set of parameters and relative values to complete the process centering for the product.

Just after the basic tests demonstrating the SoC is alive and kicking, each Nomadik™ platform is integrated into its development kit. The kit is made up of both the PCB and the set of tools for the embedded software development. The PCB is hosting and mimicking an actual mobile multimedia product, i.e., STn8815S22, as all his predecessors, has been integrated together with Power Management components, Audio Codecs, Camera Sensors, Display, keyboard, connectivity devices of all sorts.

The development tools, though based on standard solutions readily available from the usual industry leaders, have been especially tuned to allow concurrent debugging, monitoring, and profiling of all the CPU's and DSP's inside the STn8815S22.

The kit is distributed to a vast community of developers inside Nomadik™ Embedded SW community, STMicroelectronics sister divisions, third party Embedded SW development companies, as well as end customers. All of these teams concur in different ways to the final full validation of the functionality and performances of the Nomadik™ SoC and help declaring the final qualification of the product.

VI. Packaging Nomadik™

Packaging is growing in importance and weight on both product cost and performance.

STn8815S22 being a System In Package hosting the Nomadik™ SoC together with its non volatile and dynamic

memories is a good example of that.

Assembly and testing the devices puts a challenge of logistic on top of the usual technical challenge.

Memories market life is way shorter than the Multimedia Application Processing Engine one. This forced Nomadik™ team to put in place specific processes to limit the need to re-qualify the STn8815S22 whenever a new DDR or FLASH needs to be updated, to keep tight control of the relative die and final good stocks. The whole performed in full coordination with its customers to minimize end product qualification efforts.

The mechanics of stacking several dies in the same package is not a trivial task either, given the constraints that the overall size of the end product, especially of today's cellular phones, imposes. Package planar dimensions are expected to be small for real estate purposes, but package thickness is becoming more and more important to allow slim, fancy phones to be built. Shooting for minimal thickness is naturally in contrast with the constraints of wire bonding and demands techniques like flip chip to be introduced.

Stacking devices also requires special attention on warping effects of the package substrate. Improper combination and sequencing of the dies inside the package can induce distortions of the package substrate that makes connection with the PCB unreliable if not sometime impossible. STn8815S22 required the design of three different packaging solutions before achieving an optimal stacking of the four dice it embeds.

High speed interfaces, high number of internal and external connections can make the design of the package substrate a true challenge for signal integrity. Nomadik™ SoC designers are exploiting an STMicroelectronics proprietary package design kit to simulate early on in the design phase the effect of signal integrity as well as other effect, like thermal hot spots inside the package. This technique has been extremely effective on the STn8815S22 especially to properly manage high speed interfaces like that between the Multimedia Application Processing Engine and the integrated DDR memory.

VII. Engineering Nomadik™

Test program optimization is always a fundamental element in the overall cost of a product. Nomadik™ Product Engineering team has paid specific attention to the matter and has specifically worked together with the design community to maximize test coverage, yield, and effectiveness of failure analysis in case of field returns.

Great attention has been spent during the STn8815S22 test program development in the area of yield monitoring and yield improvement processes. Sustaining the production rate of cell phone manufacturer simply requires state-of-the-art practices in the field.

The STn8815S22 adds on that the need to have an optimal co-ordination and co-operation among all the suppliers of the dice embedded in the System in Package, being them inside and outside of STMicroelectronics.

Security Management poses additional multidisciplinary challenges to the Product Engineering job on Nomadik™ SoC's. Each customer of Nomadik™ can request to *customize* the SoC through the embedded HW security features. Each

SoC is customized at test time through the ATE. A proprietary signature is then used to effectively enable proprietary Embedded SW to run on the machine hence allowing each Nomadik™ customer to implement its own set of proprietary and unique features on the end product. Such technique though to be safe as all security frameworks requires that the master key is actually maintained secret and known only to the customer of Nomadik™ originating and consequently using it. Because of that a specific process for key communication to STMicroelectronics, confidentiality maintenance, and actual utilization has been put in place since the first generation of Nomadik™ devices. For the STn8815S22 it has been perfected to the point that all transactions happen electronically with no possibility for anybody but the person first issuing the set of keys on customer side can know the master key or get access to it in un-encrypted mode. Such solution has been made possible thanks to the creativity and preparation of the IT departments of STMicroelectronics, its customers, and partners in conjunction with Nomadik™ design and product engineering teams.

VIII. Project Managing Nomadik™

Several times in the course of this article, reference to the experience and ability of the people involved in the project and their effective co-operative effort has been made as a key factor for the successful implementation of the final device.

Like all SoC design teams today, Nomadik™ R&D organization is distributed over several locations on geographical areas spanning several time zones.

Project organization, exploitation of effective communication means, the selection of the right people, a positive attitude toward all challenges, either planned or accidental, is no doubt a fundamental piece of the successful story of the STn8815S22.

STMicroelectronics has a tradition for effective Project Management techniques and team organization that has been the underlining element of the entire design life of the STn8815S22. Overall over 400 people worked at different stages and contributed to the design and industrialization of the device. The adequate management of such a conspicuous multidisciplinary design team has made the difference between success and failure.

IX. Summary

Nomadik™ SoC design and industrialization main challenges has been illustrated making reference to the third generation of the family named STn8815S22.

The importance of clean and simple Architecture as the mandatory starting point and underlining guide through the whole design cycle has been highlighted.

The way Embedded SW development has been turned into a powerful complementary verification and validation tool for the STn8815S22 has been presented together with the importance of an effective early prototyping system and Embedded SW development kit.

The specific challenge directly and indirectly put by power management on the logical and physical design of the STn8815S22 has been described.

The management of the HW security framework on board the STn8815S22 to the product engineering and IT organizations inside and outside STMicroelectronics has been paired with the activities regulating the packaging of the device to exemplify the type of multidisciplinary challenges the design and industrialization of Nomadik™ like products call for.

Finally the accent has been put on the fundamental role that the correct project organization, communication and co-ordination tools, and selection of the right people have had in the successful conclusion of the design and industrialization of the STn8815S22.

X. References

- [1] See www.st.com/stonline/products/families/mobile/mobile.htm