DATE 2007 "Best Industrial Designs" Session: From Algorithm to First 3.5G Call in Record Time - A Novel System Design Approach Based on Virtual Prototyping and its Consequences for Interdisciplinary System Design Teams

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Abstract

Increasing system complexity not only in wireless communications forces design teams to avoid errors during the process of system refinement thereby keeping ambiguities during system implementation at a minimum. On the other hand the chosen system design approach has to ensure that a system design project rapidly advances through all stages of refinement from an algorithmic model to a real "System on Chip" (SoC) while maintaining backwards equivalence of the produced HW and FW/SW code with the original algorithmic model.

This system design challenge also demands a new interdisciplinary team approach encompassing all design skills ranging from concept to HW and FW/SW engineering as well as system verification to increase the overlap in the system concept, implementation and verification phase.

But how do these interdisciplinary teams cooperate efficiently, as they are used to metaphorically "speak different design languages"?

Resulting in an industry record development time for a 3.5G UMTS modem the employment of a novel system design approach is shown which serves as common system design language, avoiding the babylonian language disaster of isolated engineering worlds.

The motivation for an increasing overlap of system concept, implementation and verification phases is obvious: it can save time (to market) in the magnitude of several months or even more and thus drastically shorten design cycles by parallel development of HW and FW/SW. The proposed approach also helps to avoid costly redesign cycles due to conceptual errors and optimizes the quality of the developed system HW and FW/SW thereby also substantially reducing system development R&D costs.

1. Introduction

Turning a system concept into a complex SoC system has always meant to carry it through several stages of abstraction, thereby detailing the HW - FW/SW split and adding implementation details. System refinement is carried out until a synthesizable representation of the SoC is reached which can be compiled into a netlist for semicustom hardware design and a code image running on an embedded microprocessor core.

This iterative process of refinement and decomposition (also often referred to as "V-model") can only be successful if a seamless system modeling approach is employed. It has to guarantee that errors during refinement into HW and FW/SW are kept at a minimum and "implementation" ambiguities can be largely avoided, because these are likely to result in system malfunction.

Modern design flows are not (yet) entirely capable of generating optimized synthesizable HW and executable FW/SW code for complex embedded SoCs out of a high level algorithmic system description. But still this algorithmic system model can be used as the reference to verify it against RTL code and should also ideally be reused in a Virtual Prototype (VP), on which embedded FW/SW is developed.

Based on this approach a seamless system design flow is demonstrated, which also has quite some consequences on a crossfunctional team setup. It literally represents a common language, which concept and HW respectively FW/SW engineers speak when the composition of the previously decomposed system is performed.

Virtual Prototyping has already been successfully implemented on many microprocessor-centric system designs (such as application processor designs for mobile phones) before. For signal-processing dominated systems however the question of integrating the algorithm models into a VP has to be additionally answered. In the discussed 3.5G modem design the algorithm models were tightly integrated in the system VP and co-simulated against the HW RTL code using slave simulation techniques.

2. From Algorithm to HW

Meeting the performance requirements imposed e.g. by the 3GPP specification obviously represents the key requirement for a 3.5G modem. To do so, the entire receiver and transmitter system has to be modeled and simulated demonstrating that the employed algorithms meet - or better exceed - the standard requirements. This model was the first developed by concept engineers and is naturally simulated in a communication systems

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simulator, e.g. SystemStudio (based on an abstract algorithm modeling language).

Obviously considerations which algorithms best fulfill e.g. BLER and SINR requirements can best be done on this high system description level.

This so-called algorithm model does not have to be cycle-accurate, unlike a synthesizable HW RTL description. The latter is usually developed clock-cycle accurate by engineers with HW design background. Yet these two representations at different abstraction levels have to be equivalent with respect to the processed data. How can this apparent contradiction be resolved?

The approach requires HW and concept engineers to cooperate and work on a HW-model co-simulation allowing proof of equivalence.

The successful way chosen here was to further detail the algorithm model to an abstraction level which allowed the RTL code to be compared against it at slot-level timing resolution (a 10ms UMTS frame consists of 15 slots). Not only was timing information added to the algorithm model but it also was refined from floating to fixed point precision.

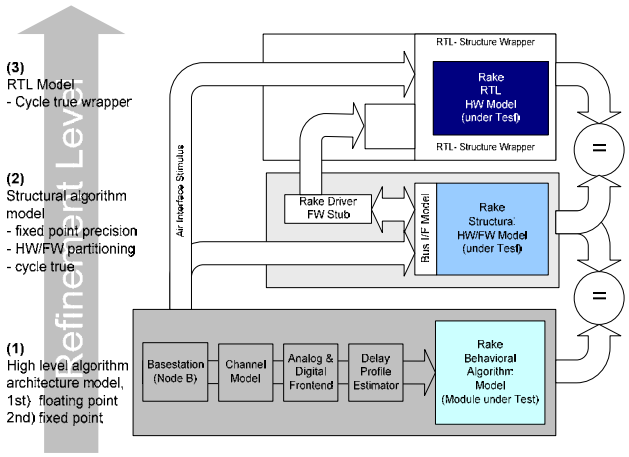

Figure 1: HW – algorithm model co-simulation of Rake receiver

In the end HW- and concept engineers were able to co-simulate RTL and algorithm model based on a single "schematic", thus allowing an automated pass/fail criterion for chip sign-off regression testing.

3. Project management: The concept of cross-functional teams

In the previous section we came across the idea of a team of two different skills (namely algorithm or concept engineers (CE) and HW designers (HW)), which have to approach to allow for a thorough co-simulation. Needless to say, that a co-simulation also requires FW/SW for HW configuration and status evaluation.

In the 3.5G modem project this concept was followed further by setting up cross-functional teams ("XFTs"), in which all aforementioned disciplines were represented and a fourth skill group taking care of system verification (CV) completes the XFT.

All of the engineers in a XFT usually have a different engineering background (e.g. HW design usually requires a RTL knowledge; FW/SW engineers work in real time embedded SW design environments), yet they all share familiarity with programming and simulation techniques.

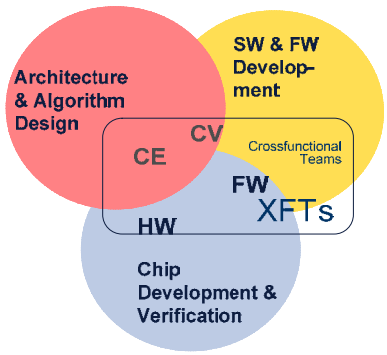

Figure 2: The concept of cross-functional teams

Therefore, making a XFT successful requires a common denominator, or better a common language, which describes the system behavior down to the desired abstraction level and allows FW/SW to be developed on an abstracted model of the HW before engineering samples are available. A Virtual Prototype ideally serves this purpose.

4. Assembling the pieces: VP as detailed system model for FW/SW design

In the presented 3.5G project a maximum reuse concept was chosen for the VP, which uses existing SystemStudio algorithm simulation chain building blocks. These signal processing peripheral models were wrapped with SystemC and integrated with SystemC models of the chip control blocks. Re-using identical models in the VP as were used for HW verification ensures consistency between the VP and the target HW. A fast instruction set simulator completes the VP.

For the entire prototype an easy to use stimulus / response mechanism is essential. It represents both the basestation (Node B) and host (comprising the higher layers of the 3.5G protocol stack). The testbench implementation details for the 3.5G basestation (Node B) and the host are hidden for the users (testers) and accessible by an easy-to-use API and encapsulated test bench libraries.

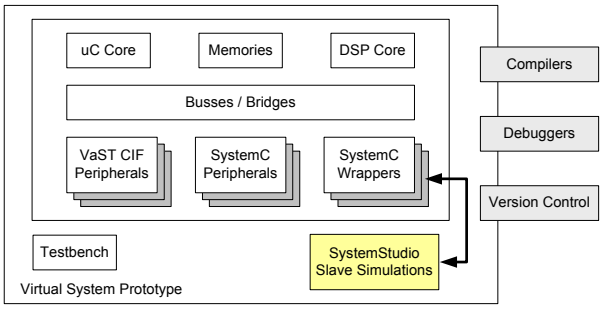

Figure 3: Virtual System Prototype (VP)

The testcases developed on the VP were designed to be reused for silicon verification without major changes. This adds value enabling a fast characterization of the HW and allows for an easy porting and verification of FW/SW developed on the VP on the target system HW.

The entire VP is fully transparent and can be suspended / resumed in system verification to ease debugging. This is a major advantage over the target system HW. Hence incremental FW/SW design with source code level debuggers attached to the 3.5G modem model continued on the VP even after the first silicon was available.

As the FW/SW development design was carried out incrementally, so was the VP design. The advantage being, that the VP did not have to be complete from the very beginning (and so did the system testbench) and could also incrementally grow as system requirements afforded it. E.g. 3G "Compressed Mode" functionality was only added late in the system design (and consequently to the 3G basestation stimulus), as it was not necessary for basic call setup system simulations.

5. Results of VP system design approach

A comparison of the system design approach with a conventional (i.e. sequential) approach using classical RTL design and e.g. FPGA prototyping has to contrast savings in project schedule with invested project efforts.

The VP approach allowed for incremental development of the modem system FW/SW shortly after design concept freeze (in fact the VP was developed concurrently with the system concept to also form a "proof of concept"). The alternative would have been a full FPGA based system prototype, which requires an almost complete RTL system representation (after synthesis and verification). Due to the size and complexity of the 3.5G modem a FPGA prototype would have also required a system partitioning onto several FPGAs with the associated efforts. With the availability of the system VP the HW - FW/SW integration could be started approximately half a year earlier.

The developed 3.5G modem HW was first time right. Only two weeks after HW availability the first FW/SW builds were ported onto the target HW. 18 months after system design start the first call in a 3.5G life network was achieved and functionality of HSDPA was demonstrated.

As previously mentioned many of the VP building blocks are necessary and hence available for a complex system setup anyhow (e.g. the algorithm models which constitute the receiver & transmitter of the modem). The extra efforts were adding SystemC models to complete the VP and the system bring-up and initial verification of the VP. Together with maintenance these efforts amounted to approximately 6 man-years, which is surely bound to decrease, once the methodology matures into a standardized design-flow. Moreover this R&D investment in VP technology is already reused in successor projects and a design framework (called SysWay) has been set up based on the successful experience with Virtual Prototyping.

The employment of the VP also saved expenses for expensive 3.5G signal generators & FPGA systems, which would have been required for most of the FW/SW developers.

6. Summary and Outlook

The presented VP based system design approach greatly increases the design productivity of design teams developing complex embedded SoCs. A VP is an utterly useful common system model, as it can be used by both system concept and HW respectively FW/SW designers, thus noticeably decreasing design time by allowing a bigger overlap of concept, implementation and verification phases of complex system projects.

As the VP methodology matures into more mainstream system flows, it will offer increasing benefit in the area of high level architecture exploration, before exposing its strength during the system refinement phase. Additionally HW verification is easily imaginable also in the full VP context (e.g. replacing individual algorithmic blocks by the corresponding HW) instead of stand-alone co-simulation with the algorithm models.

For wireless communication systems the aspect of minimized power consumption is becoming increasingly important. As a consequence the modeling of this key system requirement will find its way into VP modeling as well in the near future.

References

[1] S. Heinen et al. "Virtual Prototyping for a 3G baseband chip based on VaST CoMET / Synopsys System Studio Cosimulation", SNUG Europe 2006