Re-Configuration of Sub-blocks for Effective Application of Time Domain Tests

Jens Anders*, Shaji Krishnan, Guido Gronthoud

*University of Hannover, Institute of Electromagnetic Theory,
30167, Hannover, Germany

Philips Research Laboratories,
5656 AE Eindhoven, The Netherlands

e-mail: jand@tet.uni-hannover.de,
{shaji.krishnan, guido.gronthoud}@philips.com

Abstract

AC sensitivities guide most Analogue Automatic Test Pattern Generator (AATPG) while determining the optimal frequencies of a sinusoidal test stimulus. The optimal frequencies thus determined, normally lie in the close vicinity of the operating frequency of the circuit. Although these frequencies are justifiable by the principles of the circuit, these test frequencies do not bring any added value to the ultimate goal of cheap alternatives (low frequency test signal and cheaper measurement equipment) for the analogue and RF tests. In this paper, we propose to re-configure the circuit blocks, in such a way that the operating frequencies of the respective sub-block are shifted to lower testable frequencies. We have validated our proposal on a sub-block of a satellite receiver circuit that resulted in lowering the test frequencies of the corresponding sub-blocks from 12 GHz to 4MHz, while attaining the same level of defect coverage.

1. Introduction

Some structural test methods for RF and analogue circuits are already gaining popularity as cheap alternatives to functional tests. Notably are [1][2], where an abnormal supply current is used as an indicator of defective IC's. Although these tests are cheaper and do not require expensive equipments, the defect coverage is not exceptionally high, since these tests does not consider the dynamics of the circuit. In [3], the power supply rail is pulsed and the temporal and or the spectral characteristics of the resulting transient rail currents are analyzed. Here the authors have not explicitly provided a means to determine the rise and fall times of these test pulses. For rapid production testing of RF circuits, a solution has been proposed in [4], where optimization algorithms generate a suitable test stimulus.

Several ATPG techniques [5][6][7][8], for analog and mixed signal circuits make use of the AC sensitivities as a metric to determine the test signal (sinusoidal) frequency. However it is seen that the most effective test frequency is in the close vicinity of the operating frequency of the circuit [6] and hence do not seem to accomplish the goal of a lower frequency test stimulus.

Knowing that the test signal frequencies lie close to the operating frequency of the DUT, the alternative possibility to attain lower test frequency signals are by configuring the sub-blocks, in such a way that the operating frequencies are shifted to a lower range, thus enabling us to determine a comparatively lower test frequency signal. In this paper, we describe such a methodology for RF and mixed signal circuits. The overall objective of this methodology is to configure the sub-blocks of the DUT to achieve low operating frequencies, thus enabling the possibility of determining a low frequency test signal frequency. Once the sub-blocks have been re-configured, we also describe our ATPG flow in detail.

The section is organized as follows; section 2 provides a background on the optimal test signal generation for analogue circuits in general, section 3, discuses how sensitivities are related to test signal generation. In section 4 we elaborate on how we configured the sub-block of an industrial circuit and in section 4 we describe the analogue ATPG flow. Finally we derive our conclusions in section 5.

2. Background

It has been proven using control theory methods, particularly the '*pontrajagin maximum principal*' [9], that for a general analog circuit, a piecewise constant signal is the optimal test signal [10]. This optimal signal is able to maximize an arbitrary merit function, which in our case is the function *f (t),* equation (1), which in itself is the fault-detecting criterion. Knowing this signal characteristic, the structure of the required stimuli can be formulated as equation (2) and Fig. 1. Determining an optimal test signal is then an optimization problem that maximizes the merit function, with constrains on the

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maximum and minimum allowable ranges (V_{min}, V_{max}), for the input signal and a maximum time domain simulation time (T_{sim}).

$$Maximize : f(t) = \sum_{i=0}^{n} \psi^{f_k}(t)$$

$$\psi^{f_k}(t) = \int_0^{T_{sim}} | V_{out}^{g}(t) - V_{out}^{f_k}(t) |$$

$$Fault(f_k), k = 1...n \quad (1)$$

The above optimization problem is formulated as a non-linear problem (NLP) that requires the computation of the gradients. The gradients are the transient sensitivities and computed using the adjoint method [11].

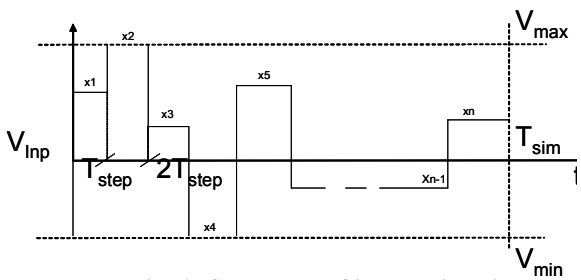

Fig. 1: Structure of input stimuli

$$V_{inp}(t) = \sum_{i=1}^{n} x_i[(t-(i-1)T_{step}) - (t-iT_{step})]$$

$$Such : V_{inp}(x,t), V_{\min} \le V_{inp} \le V_{\max}$$

$$Where : n = \frac{T_{sim}}{T_{step}} \quad (2)$$

However, this approach is not suited for large industrial circuits for two major reasons. On one hand, computing the transient sensitivity at every stage of optimization is very expensive while the other, it is not a trivial task to control with high precision, especially a test signal with varying amplitude and timing on a tester. Hence we have parameterized the input signal on the amplitude and frequency. This restricts our test signal with fixed amplitude and frequency (the optimal, although has to be determined through an optimization process), that can be easily generated by tester programs. The modified (V_{inp}), now takes the form as equation (3.) and Fig. 2

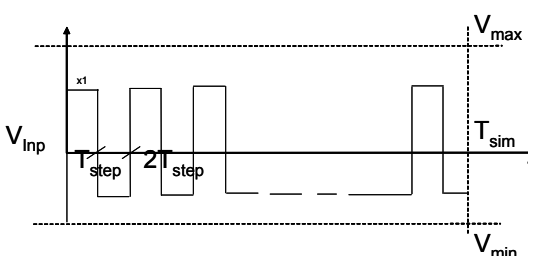

Fig. 2: Structure of modified input stimuli

$$V_{inp}(t) = x_1 - 2x_1 \sum_{i=2}^{n} [(t-(i-1)T_{step}) - (t-iT_{step})]$$

$$Such : V_{inp}(x,t), V_{\min} \le V_{inp} \le V_{\max}$$

$$Where : n = \frac{T_{sim}}{T_{step}} \quad (3)$$

3. Sensitivities as metrics for analog test signals

Sensitivities [12], are defined as the tendency of one circuit quantity (sensitivity item) to vary with a change of another circuit variable (sensitivity parameter). Therefore, by definition, sensitivities provide information how much a change in a certain circuit parameter (the faulty value) causes changes in a measurable output of the circuit. Although there exist several different kinds of sensitivities that can be classified according to the magnitude of the change in the sensitivity parameter as differential sensitivities (small changes) as in equation (4), where p_i is the parameter and T_j the circuit output under investigation,

$$S_{p_i}^{T_j} = \frac{p_i}{T_j}\frac{\partial T_j}{\partial p_i} = \left[\frac{\frac{\Delta T_j}{T_j}}{\frac{\Delta p_i}{p_i}}\right]_{\Delta p_i \to 0} \quad (4)$$

or incremental sensitivities (large changes) as in equation (5),

$$\rho_{p_i}^{T_j} = \frac{p_i}{T_j} \times \frac{\Delta T_j}{\Delta p_i} \quad (5)$$

and the domain in which they are measured as AC-sensitivities (frequency domain) or transient sensitivities (time-domain), most of the work in the past [6][7], was restricted to AC-sensitivities, simply due to the fact that all commercial circuit simulators were not capable of calculating their transient counterparts.

Given a fixed circuit topology and fixed circuit parameters, an AC-sensitivity analysis reveals at which frequencies a certain parameter change yields the largest difference from the nominal value and therefore can be detected most easily. Because sensitivities only provide gradient information, i.e. relative changes, to ensure that the actual difference caused by the parameter shift is indeed measurable at a frequency with a large sensitivity value, a necessary condition for a good test signal is that the circuit output is sufficiently large at this frequency, i.e. the circuit must have a pass-band in this frequency range.

One straightforward way of using sensitivities in the test-signal generation process is to simply detect all sensitivity peaks that lie in a pass-band of the circuit, i.e.

yield a sufficiently large signal at the circuit's output and use the frequency corresponding to the largest of these peaks as the test frequency. Two questions that now arise naturally are: (i) In which frequency regions, relative to the operating region of the circuit, do these sensitivity peaks occur? (ii) How close are the frequencies obtained from sensitivity calculations to the optimal test signal (as calculated by an optimizer)?

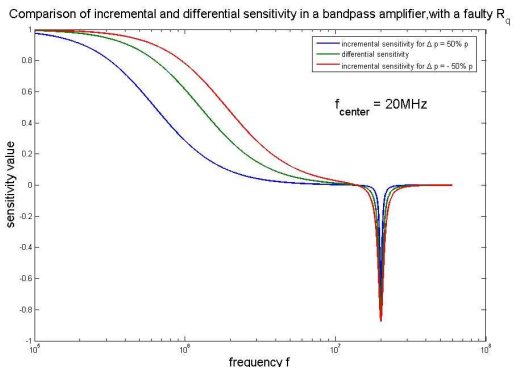

Fig. 3: bandpass amplifier, parameter (P1)

To answer the first questions, several smaller test circuits have been investigated in great detail, among which were, a low-pass amplifier, a band-pass amplifier, a state-variable filter and a Gilbert-cell mixer. As our analysis revealed, the sensitivity peaks for both small and large, i.e. around ±50%, parameter changes resulted in sensitivity peaks in the pass-band or around the cut-off of the low-pass characteristic, respectively. This very intuitive result is exemplarily shown for a band-pass amplifier (2 parameter variation: P1, P2), with a center frequency of 20 MHz in Fig. 3 and Fig. 4.

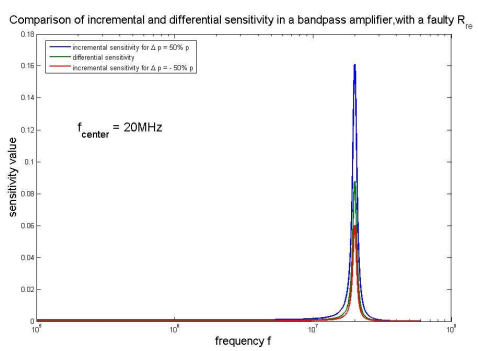

Fig. 4: bandpass amplifier, parameter (P2)

The second question can only be answered rigorously for linear circuits, which can accurately be described with the aid of transfer functions. In these cases, the sensitivity peaks coincide with the optimal test frequencies. Thus, we can conclude that the sensitivity peaks will always lie in a frequency region close to the operating frequency of the device under test (DUT). Hence, although sensitivities are indeed ideal metrics to obtain good test signals for analog circuits the resulting test frequencies, one would obtain, are essentially the same ones one would apply in a functional based testing of the circuit and accordingly the same drawbacks apply, e.g. possibly very high testing frequencies requiring expensive test equipment. Thus, to use sensitivities as a metric and still receive the desired low-test frequencies, some DFT has to be incorporated into the circuit that brings the operating range of the device down to lower frequencies during the test phase but does not disturb the normal circuit operation.

4. Sub-block re-configuration

In this section we will be exemplarily shown how the topology of a circuit can be modified during testing to bring the operating frequency down to lower frequencies and thus allow the use of low and thus cheap test frequencies. As already alluded in the previous section, the reason for doing this is that it enables to use sensitivities as a simple and fast means of obtaining optimal test frequencies and still test with signals that do not require very expensive testing equipment. To illustrate the idea, an industrial satellite receiver as shown on a block level in Fig.5 will be considered.

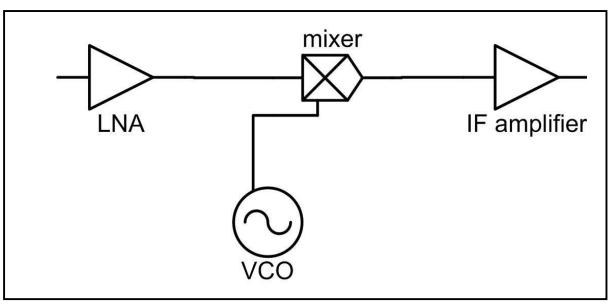

Fig. 5: Satellite receiver – block diagram

The design comprises four main building blocks, whose functionality are as follows, the first block in the receiver is a low-noise amplifier (LNA) both providing a match to a 50 Ω antenna at the operating frequency around 12 GHz and amplifying the signal sufficiently to make it immune against the noise contributed by the following stages, especially the mixer. The second component is the mixer, which is driven by a local voltage controlled oscillator (VCO) and serves the purpose of down converting the signal from the RF-frequency to the lower IF-frequency band where the final signal amplification is done in some gain-controllable IF-amplifiers. For the purpose of low-frequency test signal generation it is important to note that the input of the overall system, i.e. the LNA input, is working at the RF-frequency around 12 GHz and shows a rather selective frequency response, that is, it heavily attenuates signal components outside this frequency band. Recalling the findings in section 3, it is impossible to apply any useful test signals at the LNA input outside a rather narrow band around 12 GHz. Still, one knows that the whole IF-part of the receiver is working at a much lower frequency

in the megahertz range. Therefore, it is natural to seek a way to test as much of the receiver using frequencies from the lower IF-range. The idea now is to make the mixer reconfigurable. That is, while in the normal operation mode, it down converts the signal from the RF- to the IF-range, during testing, it can operate in a different mode, directly passing through signals from the IF-range. During test, the LNA and the VCO are disconnected from the mixer, the LO is replaced with appropriate bias voltages and the mixer input (suitable multiplexing) is fed with lower frequency test signals as will be described in detail later in this section.

A problem with this is that switches have to be placed in the signal path. Thus, there will be an unavoidable loss and distortion associated with these switches. However, a careful design using modern processes with transit frequencies well above 100GHz can provide satisfactory performance (e.g. a loss of less than 2dB) even at an operating frequency of 12GHz. Therefore, in view of the drastic reduction in the requirement on the speed of the testing equipment, the additional circuitry might well be a price worth to be paid.

A structure particularly suitable for this type of DFT is the Gilbert-cell type mixer, which is commonly used nowadays and is also incorporated into the satellite receiver. A simplified schematic of such a circuit is shown in Fig. 6.

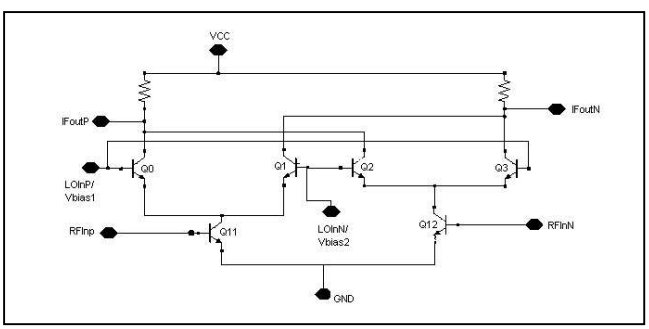

Fig. 6: Schematic of Gilbert-cell type mixer

In normal mode the switches connect the local oscillator ports (labeled LOInP and LOInN in the figure) to the switching transistors of the mixer and the mixing operation takes place. During test mode, the LOInp, LoInn are disconnected from the switching transistors Q0 through Q3 and replaced by a constant bias voltage. Firstly, Vbias1 is adjusted such that transistors Q0, Q11, Q12 and Q3 are turned on in saturation region while Vbias2 is zero to disable transistors Q1 and Q2. To be able to test for faults in the latter two devices, in a second test phase Vbias1 is grounded while Vbias2 is set to the former value of Vbias1. Thereby, the mixer is turned into a low-pass amplifier with a 3dB corner frequency set by the RC-load in the two legs. Depending on the conservatisms of the mixer design, this 3dB corner is typically five to ten times larger than the IF-bandwidth of the system. The procedure just described was applied to the mixer in the satellite receiver and the resulting transfer characteristic is shown in Fig. 7. One clearly sees that there is a pass-band section between 10 and 100 MHz and one can expect to find test frequency candidates in this frequency region.

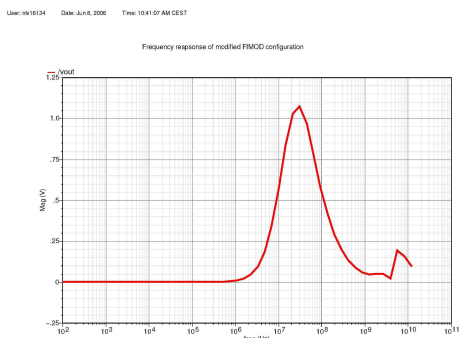

Fig. 7: Transfer characteristic after re-biasing

Thus, by introducing a pair of additional switches it has been achieved to lower the required test frequencies by approximately two orders of magnitude. This result is generic in the sense that most of today's integrated receiver structure incorporate Gilbert cell mixer and hence the proposed method is widely applicable.

5. Analogue ATPG flow

In order to determine the test frequencies in an analogue ATPG flow, firstly a reference fault list of all possible short faults in the bipolar transistors of the DUT blocks (mixer, differential-to-single-ended and IF-amplifier) was generated and afterwards optimal test signals for each of these faults were calculated using a new test signal design flow, which is shown in Fig. 8, and will be explained in detail in the following.

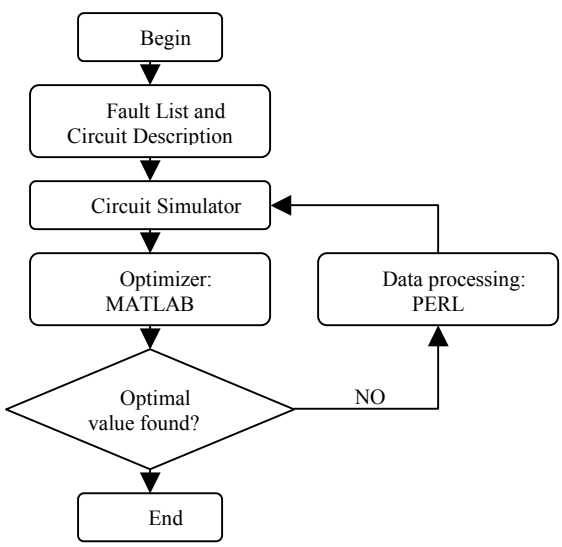

Fig. 8: Analogue ATPG work flow

The core of the test signal generation procedure is a general-purpose optimization tool running, in the

MATLAB environment. The optimizer uses Perl scripts to inject faults from the fault list into the circuit netlist one at a time. Then the circuit simulator to calculate the integral difference between faulty and golden device in a periodic-steady state analysis (PSS) according to equation.(6), where p is the faulty parameter, $\Delta T_{sampling}$ is the sampling interval and $v_{out,g}$ and $v_{out,f}$ are the outputs of the golden and the faulty device respectively.

$$f(p) = \frac{1}{\Delta T_{sampling}} \int_{\Delta T_{sampling}} | v_{out,g} - v_{out,f} | dt \quad (6)$$

The value f(p) is then fed back to the optimizer and, based on this value, the new values of the optimization variables amplitude and frequency are selected. Finally, the optimization process will give an optimal test signal, defined by the corresponding amplitude and frequency values and, if the corresponding difference value is sufficiently large, the fault is declared to be detectable. It was found that with the method just described all faults injected were detectable resulting in the ideal fault coverage of one hundred percent. Table 1 list all the transistors in the design together with the injected faults, the corresponding optimal amplitude and frequency values as well as the resulting integral difference. The detectability threshold was set to be 100 mV, a rather pessimistic value.

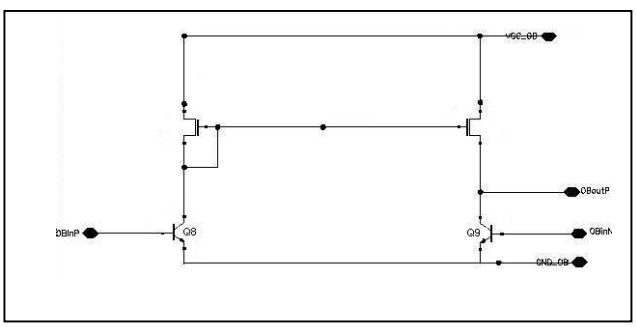

Fig. 9: Schematic of Differential-to-Single-ended

The table can be read as follows. The first column lists the transistor name in which the fault was injected. The first six transistors belong to the core mixer, Fig. 6, while the next four were part of an intermediate differential-to-single-ended conversion stage, Fig. 9 and the last six transistors belong to the IF amplifier, Fig. 10. The second column lists the optimal amplitude for the test sinusoid. There are three entries corresponding to the three possible short faults in a bipolar transistor, collector-base (CB), base-emitter (BE), collector-emitter (CE). The third and fourth column list the optimal test frequency and corresponding integral difference value in the same format. Since the minimum integral difference value listed is 116mV, all faults were safely detectable. There are two main aspects to be noted from Table 1. Firstly, the optimal amplitude is not fixed to the maximally tolerable value of 3V, as it would have been predicted by linear theory, but can take on almost any value between 0.13V and 3V.Thus, a pure small signal, linear view of the problem is insufficient and nonlinear effects have to be taken into account to achieve good test performance. Secondly, the range of optimal test frequencies lies between 0.1 MHz and 40 MHz. Thus, compared with the normal operation frequency of the system around 12 GHz, there is a minimum reduction factor of 12GHz / 40Mhz = 300, which results in a great relaxation for the testing equipment in terms of operating frequency and accuracy.

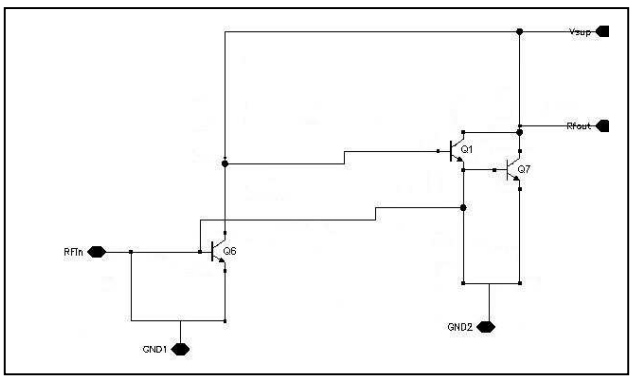

Fig. 10: Schematic of IF Amplifier

Conclusions

We have described a methodology to effectively apply time domain periodic test signals. Although AC sensitivities can determine effectively the frequency of a sinusoidal test signal, these test signal frequencies tend to lie in the close proximity of the operating region of this DUT. This is a less motivating on the ultimate goal of cheap alternatives (low frequency test signal and cheaper measurement equipment) for the analogue and RF tests. The method that we described above is one of the many ways to reconfigure the sub-blocks of the circuit, with a goal to lower the operating frequency of the respective sub-block. The method we have chosen to reconfigure the mixer sub-block has resulted in shifting the operating band of the mixer from thousands of MHz to few MHz.

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Table 1: Transistor Faults									
Transistor	Aopt/V			fopt/MHz			integral difference/V		
Mixer	CB	BE	CE	CB	BE	CE	CB	BE	CE
Q11	0.81	0.55	1.92	37.1	40	40	0.504	0.42	1.164
Q12	3	1.38	0.42	4.6	31.9	31.9	0.195	0.138	0.166
Q0	3	0.5	0.43	4.7	25.1	25.1	0.213	0.116	0.167
Q1	0.5	0.96	2.29	25	40	40	0.404	0.833	1.057
Q2	3	0.5	0.43	4.7	25.1	25.1	0.213	0.116	0.167
Q3	0.5	0.96	2.29	25	40	40	0.404	0.833	1.057
Diff-to-single-ended	CB	BE	CE	CB	BE	CE	CB	BE	CE
Q9	1.2	0.4	3	20.5	0.1	0.1	0.699	1.481	0.928
Q8	0.13	3	0.44	0.1	40	40	1.764	0.93	1.839
IF amplifier	CB	BE	CE	CB	BE	CE	CB	BE	CE
Q7	3	1.17	3	40	20	20	0.944	0.795	1.342
Q6	0.13	3	0.41	0.1	40	40	1.8	0.927	1.342
Q1	3	0.16	3	35.5	40	40	1.208	0.521	0.944

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