Testable Design for Advanced Serial-Link Transceivers

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Abstract

This paper describes a DfT solution for modern serial-link transceivers. We first summarize the architectures of the Crosstalk Canceller and the Equalizer used in advanced transceivers to which the proposed solution can be applied. The solution addresses the testability and observability issues of the transceiver for both characterization and production testing. Without using sophisticated testing instrument setting, the proposed solution could test the clock and data recovery circuit and characterize the decision-feedback equalizer in the receiver. Our experiments demonstrate that the proposed method has significant higher fault coverage and lower hardware requirement than the conventional approach of probing the eye-opening of the signals inside the transceiver.

1.0 Introduction

Improved fabrication technology enables the continuing increase of both on-chip operational speed and the data rate of inter-chip communications. Modern serial links maximize the interconnect performance by employing high fan-in multiplexing transmitters (TX) and high fan-out demultiplexing receivers (RX). Industry standards [1] for specifications of I/O electrical characteristics of 6+ to 11+ Gb/s interfaces have been developed, which target various applications in optical modules, high-speed backplanes, and chip-to-chip interconnect [2]. The long-range backplane applications are particularly challenging for robust high-speed I/O due to the combined effects of the physical impediments in legacy backplane channels. The impairments include the frequency-dependent loss characteristics of the copper channels and the interference from the adjacent channels, known as Crosstalk [3]. Moreover, the presence of the open-ended vias at the thick backplane intercard as well as channel discontinuities between the intercards induce reflections which further degrade the signal integrity [4].

To improve the data transmission quality, the TX and RX equalization has been employed to remove the inter-symbol interference (ISI) resulting from the finite channel bandwidth and reflections caused by a non-ideal channel. The incorporation of a decision-feedback equalization (DFE) scheme in the RX and a feed-forward equalization (FFE) scheme in the TX allows much more reliable NRZ (bi-level) data transmission at multi-GHz, and thus relieves the need for multi-level data transmission which demands higher design complexity and power consumption for the transceiver [2][5][6]. Meanwhile, crosstalk (XTalk) which is the dominant noise for microstrip interconnects is becoming a limiting factor for signal integrity. Among various types of XTalk sources, the near-end crosstalk (NEXT) is the most severe one [8]. Active NEXT cancellation in the transceiver could be an effective solution to addressing the XTalk problem [3][4].

Figure 1 illustrates the architecture of an advanced transceiver which includes a Clock and Data Recovery circuit (CDR) and a DFE in the RX, a FFE in the TX, and a XTalk Canceller between the TX and RX. This transceiver has the capability to equalize the lossy channels, to remove signal reflections, and to actively cancel the NEXT noise for achieving a 10-Gb/s+ data rate over backplane channels or other long-range applications.

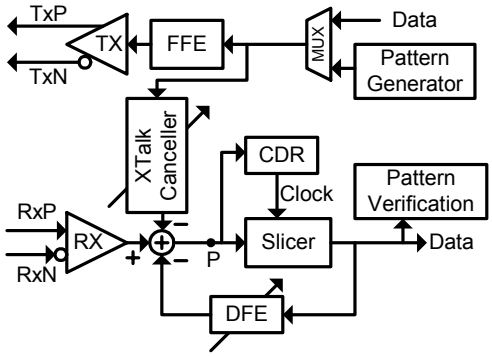

Fig. 1. The architecture of an advanced transceiver for 10-Gbp/s+ backplane interconnect

To test and characterize such a high-speed transceiver, however, is a challenging task, especially to test the DFE and the CDR of the RX in high-volume production. Testing the DFE in the RX requires an external instrument which could synthesize and drive an ISI-distorted signal to the RX, and a mechanism to measure and report the eye quality at the DFE output (Point *P* in Fig. 1). One simple solution is to connect the DFE output to an external access point, and use an external oscilloscope with active probes to capture the signal. Nevertheless, the probe contact degrades the integrity of the captured signal. In addition, examining the eye-diagram would not be cost-effective for production testing. An alternative and more sophisticated solution is to incorporate self-test circuitry for on-chip waveform capture [7]. However, the hardware overhead of the on-chip, self-test solution could be high and may not be acceptable for some applications. Meanwhile, for the CDR, characterizing the transfer function and testing the jitter tolerance necessitate sophisticated instruments for synthesizing jittery signal, with specified jitter amount and characteristics, and driving it to the RX. This requirement further drives up the production cost.

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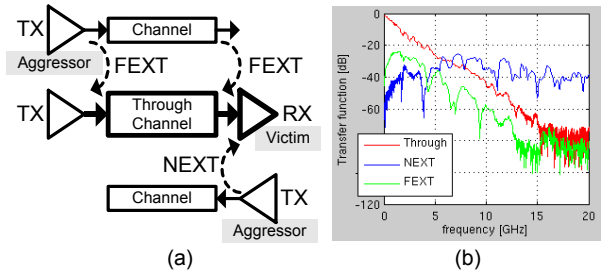


Fig. 2. Two types of XTalk: (a) Definitions. (b) Frequency Response of 10G Ethernet backplane channel

To alleviate the above-mentioned problems of characterizing and testing the RX with a CDR and a DFE inside, we propose a testable design for the transceiver. The idea is general and thus applicable to a wide range of circuit implementations of the transceiver. The design requires only some additional flip-flops, a digital pattern generator in the RX, and mechanism for configuring signal paths during testing, to achieve the desired observability and testability.

The remainder of the paper is organized as follows. Section 2 covers the architectures of the XTalk Canceller and the DFE. Section 3 and Section 4 describe our test methodologies for the CDR and the DFE respectively. Section 5 concludes the paper.

2.0 Background

Among various circuit approaches and adaptation algorithms to adjust the circuit coefficients, the architectures of XTalk Canceller and adaptive DFE are similar. They are described in this section.

2.1 XTalk Canceller

XTalk which occurs between the interconnects in the die, the package, and the PCB is the unwanted coupling of signals between an aggressing transmission line and an adjacent victim transmission line. XTalk can be categorized as either Near-End or Far-End Crosstalk (denoted as NEXT and FEXT respectively in Fig. 2(a)). When two signals are traveling in the same direction, the coupling is referred to as FEXT. On the other hand, when two signals travel in the opposing directions, the coupling is referred to as NEXT [8]. Fig. 2 (b) shows the magnitudes of the NEXT, FEXT, and the victim signal (denoted as "Through") based on the S-parameter measurement of an IEEE802.3ap backplane channel [9]. The measurement of FEXT, for example, is made by sending a signal from one TX which acts as the aggressor, and measuring its effect at the RX side of the victim channel whereas all other TXs, including the TX of the victim channel, are shut off. While there could be several aggressor channels for each victim channel, typically only few among them incur significant amount of XTalk on the victim channel.

As indicated in Fig. 2(b), both the FEXT and the victim signal are attenuated by the channel loss and the attenuation becomes more significant when the frequency increases. Nevertheless, the NEXT is not attenuated by the channel and remains roughly at the same level across the entire frequency range of interest. The NEXT corrupts the

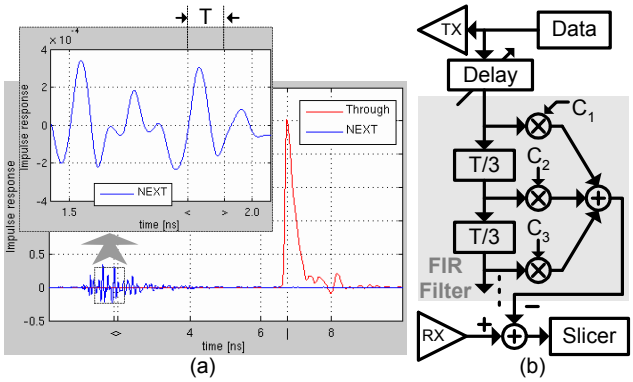


Fig. 3. (a) 10Gb/s Pulse Response derived from Fig. 2. (b) Architecture of XTalk canceller

victim signal at the RX side after the victim signal has been attenuated by the channel. Therefore, the impairment caused by the NEXT is more severe than the FEXT. Furthermore, as indicated in Fig. 2(b), at a data rate higher than 10Gb/s (i.e. Nyquist rate higher than 5GHz), the magnitude of the NEXT is even higher than that of the victim signal. To address this problem, active XTalk cancellers have recently been proposed to remove NEXT [3][4].

Based on the measurement data of Fig. 2(b) and suggestions in [1], the 10Gb/s pulse responses of both the victim signal and the NEXT are calculated and plotted in Fig. 3(a). As indicated in the magnified diagram of the figure, the NEXT has a total of 3 rising or falling transitions within a single one-bit period (T=100ps). Accordingly, the XTalk canceller, whose architecture is shown in Fig. 3(b), can be realized by an adjustable delayer for temporal alignment followed by a FIR filter with each tap spaced T/3 apart [3][4] to imitate the NEXT. The output signal of the XTalk canceller is deducted from the received signal at the RX before the signal is reconstructed by the slicer.

The number of taps implemented in the FIR filter varies for different applications, often determined by the requirement on the signal integrity. Also, there are a number of distinct adaptation algorithms for adjusting the delayer and the coefficients of the FIR in the XTalk Canceller. While there are a wide variety of implantations, most XTalk cancellers fit into the common scheme shown in Fig. 3(b). Under this architecture, the XTalk canceller can be utilized as part of the loopback path between the TX and the RX for testing the RX.

2.2 Adaptive DFE

Modern multi-Gb/s transceivers consist of pre-emphasis/de-emphasis equalizers in the TX and FFE/DFE equalizers in the RX. The TX equalizers are typically not adaptive. For a time-varying channel (which, for example, incurs temperature-induced variation), a TX equalizer can only achieve suboptimal performance. Handling such variations demand an adaptive equalizer. An adaptive FFE at the RX, while capable of flattening the channel response, cannot differentiate noise from the desired signal. On the other hand, an adaptive DFE in Fig. 4(a) is very suitable for RX equalization as the slicer in the RX for constructing the

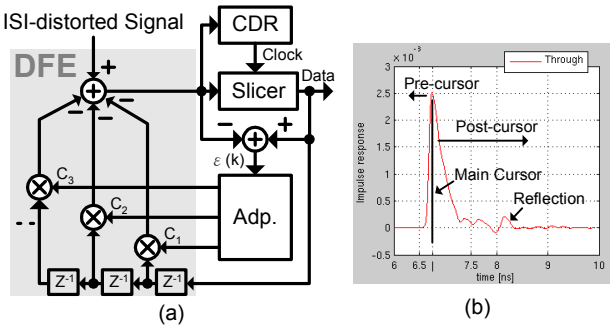


Fig. 4. (a) Architecture of a Decision Feedback Equalizer (DFE). (b) Pulse response of the through channel.

estimated logic symbol (i.e. 0 or 1) allows the DFE to amplify the recovered signal while rejecting the noise. However, a DFE alone is not a complete solution because it can cancel only postcursor but not precursor ISI (shown in Fig. 4(b)). Additional equalization, such as adding a FFE to the TX [5], is needed for achieving optimum system performance.

Fig. 4(a) illustrates the DFE with each tap separated by a one-bit time-delayer (Z^{-1}). There are several adaptation algorithms available for the implementation of the adaptation engine (*Adp.*), including the popular sign-sign least mean square (LMS) algorithm [5][10][11]. Most of these engines are implemented by mixed-signal circuitry and the tap coefficients are typically handled digitally. With such implementations, the equalizer combines the advantages of high-speed analog continuous-time filtering and accurate digital tap adaptation. More importantly, the digital tap coefficients of the taps can be easily scanned out for testing purpose.

3.0 Using XTalk Canceller to Test CDR

The closed-loop transfer function of the CDR, which is the same as the jitter transfer function, encapsulates the dynamic characteristic of the entire CDR [16]. Examining this transfer characteristic requires a signal generator to synthesize and drive a jittery data signal to the RX. The XTalk canceller could serve this role with proper control to the coefficients (e.g., C_1, C_2, and C_3 shown in Fig. 3(b)) of the FIR filter. The XTalk canceller could be used to inject periodical jitter (PJ) into the signal from the TX, and then drives this combined signal to test the CDR. The *pattern verification* unit shown in Fig. 1 checks the output pattern of the CDR to determine the bit error rate (BER). Meanwhile, no external signal is applied to the RX, and the DFE is turned off, leaving only the CDR for testing. With this method, the CDR can be tested within the transceiver itself, and no external instrument is required.

Consider an XTalk canceller using a 3-tap FIR filter. To inject periodic jitter (PJ) with jitter frequency *fj,* we could set the waveforms in the 3 coefficients (C_1, C_2, and C_3) like the ones shown in Fig. 5(a), where Tj is the period of the PJ, i.e. Tj=1/fj. Basically, the 3 coefficients swing between 0 and 1 within one jitter period, Tj, of the PJ. The number of steps in the ramps of these coefficient values between 0

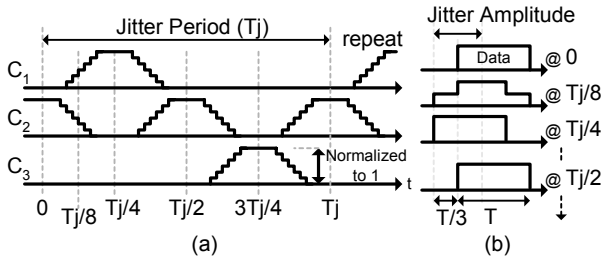


Fig. 5. (a) Coefficient values for XTalk canceller. (b) Output waveforms of the XTalk canceller

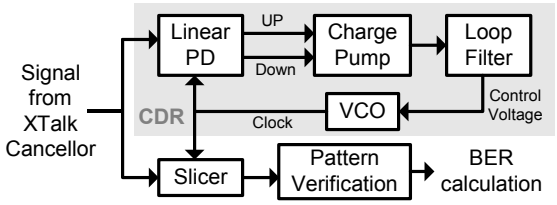


Fig. 6. A simplified CDR model for simulation

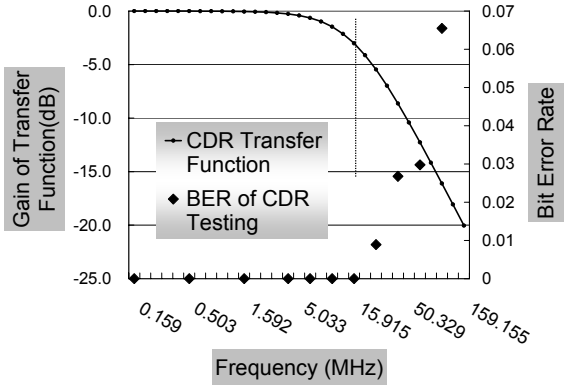


Fig. 7. Simulation result of CDR testing

and 1 depends on the resolution of the coefficients and the operation speed of the circuits. For example, at time 0 in Figure 5(a) where C_2 is set to 1 and the other two coefficients are set to 0, the XTalk canceller can drive the full swing of the data signal from the TX, with an extra delay of T/3 to the data. The output waveforms of the XTalk canceller at various time instances are shown in Fig. 5(b). Note that the data period T is much smaller than the jitter period Tj. So there will be a large number of data bits between any two adjacent time instances (say, time 0 and time Tj/8) indicated in Figure 5(b). The data waveforms of those data bits would have a waveform shape somewhat between the corresponding waveform shapes shown in the figure. With the attribute of the T/3 spacing between each tap in the XTalk canceller, the injected PJ would have a peak-to-peak jitter amplitude of 2T/3.

Note that in real operations, the magnitude of the XTalk is typically less than the data signal. Thus, for the purpose of crosstalk cancellation, the maximum value that can be set to the tap coefficients in the XTalk canceller is often designed to be smaller than 1. Therefore, to serve the purpose of testing the CDR, it would be necessary to over-design the XTalk canceller so that the coefficients can be set to any value in the full range between 0 and 1.

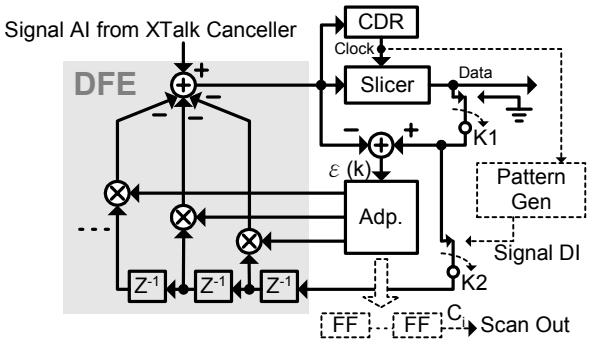


Fig. 8. Architecture of a testable DFE

To validate the proposed test methodology, a behavioral model of the CDR, shown in Fig. 6, is developed for simulation. For the purpose of simplicity, a linear phase detector (PD), a PLL-base VCO [12], and a first order loop filter are chosen to construct the simulation model. The overall closed-loop transfer function plotted in Fig. 7 represents the characteristic of the CDR. The jittery signal from the XTalk canceller which includes PJ with various jitter frequency, thus different Tj's, are applied to the CDR. For each jitter frequency, the corresponding Bit Error Rates (BER), calculated by the *pattern verification* unit, is also marked in Fig. 7. In this experiment, a certain amount of random jitter is also injected into the TX signal, before the PJ is injected through the XTalk canceller.

As indicated in Fig. 7, at the frequencies with a unit gain, the CDR tracks the jittery signal from the XTalk canceller very well and no bit error occurs. When the frequency of the PJ is slightly higher than the -3dB frequency (15.9MHz in the simulation), errors start to appear. This suggests that the CDR marginally tracks the signal at this jitter frequency, and any additional random jitter would result in bit errors. The error rate rises rapidly as the jitter frequency further increases, indicating the CDR can no longer track the PJ with a high jitter frequency.

According to this result, we can set the jitter frequency of the injected PJ to the -3dB frequency of the expected CDR transfer function for production testing. If the BER exceeds the spec., the transceiver would be considered defective, which could be due to either a defective CDR or excessive random jitter residing in the TX signal.

4.0 Testability of DFE

To achieve high testability, we propose modifications to the conventional DFE architecture (shown in Fig. 4(a)), and the resulting architecture is shown in Fig. 8. An additional shift register is inserted to store the digital tap coefficients c_i in the adaptation engine. During characterization and testing of the DFE, the coefficients, after being converged and becoming stable can be scanned out to external ATE. Meanwhile, for testing the DFE, switch K1 disconnects the slicer output from the *Adp.* unit, and switch K2 connects the *pattern generator* directly to the delay-line in the DFE. Under this configuration, the error signal $\varepsilon(k)$, which is the input to the *Adp.* unit, directly comes from the output signal of the DFE. We will show later that this proposed approach alleviates the need for analyzing the output waveform of the equalizer. In addition, all the DfT circuitry is digital, and thus the additional design effort for the DfT circuitry would be modest.

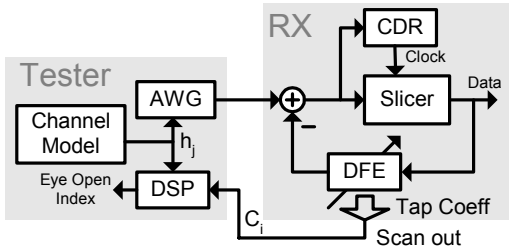


Fig. 9. Test setting for characterizing the DFE

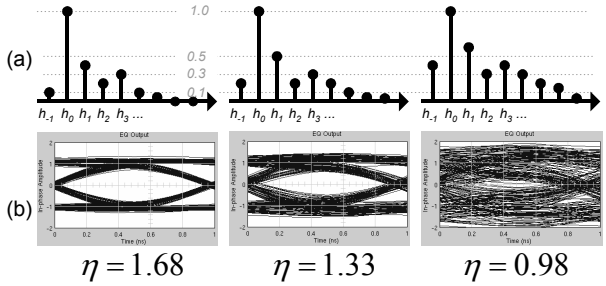


Fig. 10. (a) Pulse responses of 3 ISI channels. (b) Eye diagram of at the DFE output and their η's

4.1 Characterization of DFE

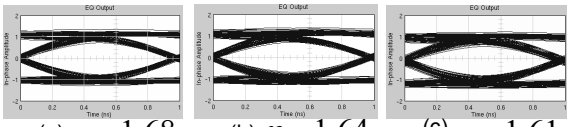
We assume the ISI-distorted channel model is known and given in the form of $H(z)=h_jZ^j$. Utilizing the method of examining the convergence of the DFE proposed in [13], the eye-opening of the DFE output can be calculated based on the given channel model, h_j, where $j \leqq m$, and the scanned out DFE coefficient, c_i, where $1 \leqq i \leqq n$ and n is the number of taps in the DFE. In the setting of Fig. 9, the arbitrary waveform generator (AWG) in the tester drives an ISI-distorted signal to the RX based on the given h_j. After the tap coefficients converge, coefficients c_i $i=1...n$ are read out by the tester to calculate the eye-opening index, η, of the DFE output:

$$\eta = \frac{2 \times \max_k \left(\left| h_k - c_k \right| \right)}{\sum_k \left| h_k - c_k \right|}$$

where $k \leqq \max(m,n)$. h_k equals to h_j if h_j exists; otherwise h_k equals to *0*. Similarly, c_k equals to c_i if c_i exists; otherwise it's *0*.

According to [14], if $\eta \leqq 1$, the eye at the equalizer output is considered closed, the channel is not equalized and the ISI still exists. If $1<\eta \leqq 2$, the eye is open. The larger the η value, the better performance of the DFE.

We conducted simulation to evaluate how closely the eye-opening index η correlates to the actual opening of the eye diagram at the DFE output. We used a 5-tap DFE for the experiment, and applied 3 different channel-distorted signals to the RX. The pulse responses of these distorted-channels are plotted in Fig. 10(a) with their corresponding channel models, characterized by h_j. By examining the eye-opening at the DFE output in Fig. 10(b) and their corre-



(a) $\eta = 1.68$ (b) $\eta = 1.64$ (c) $\eta = 1.61$

Fig. 11. Eye diagrams at the DFE output. (a) without defect. (b) with 5th tap broken. (c) with DC offset

sponding η, we indeed observed that the smaller the eye-opening, the lower the eye-opening index η value. Especially in the third example of Fig. 10, the eye at the DFE output is closed and the calculated index η is indeed less than 1.

For the DFE in the RX, we characterize its performance by using various ISI distorted waveforms driven by the AWG in the tester and calculating their index η with the captured tap coefficients. Therefore, it eliminates the need for direct probing or on-chip monitoring of the DFE output.

4.2 Production Testing of the DFE

Examining the eye-diagram of the DFE output in the production testing could result in a poor fault coverage. We show 2 simple examples to illustrate the relatively poor defect-detection capability of the eye-diagram approach. Consider a 5-tap DFE. The first example is a broken 5th tap which is always stuck at 0. The second example is a defective DFE which has a nonzero common mode voltage resulting in a DC offset voltage at the RX input. In this specific example, the DC offset voltage is 10% of the full swing of the data signal. We applied to the DFE the input signal distorted by the ISI channel whose channel model is the left-most one shown in Fig. 10(a). We then draw the eye diagram at the output. In comparison with the eye-opening of the DFE without defect (in Fig. 11(a)), the eye-openings of the 2 faulty DFE, one with the broken 5th tap (in Fig. 11(b)) and the one with a DC offset voltage (in Fig. 11(c)), are slightly smaller. The indexes η of the 2 faulty DFEs are indeed slightly lower than that of the fault-free DFE. However, the difference between the faulty and fault-free DFEs is insignificant and could not be reliably used for fault detection in production testing, resulting in test escape.

To enhance the fault coverage, we propose a new test method which targets the testable design shown in Fig. 8. To test the DFE, switches K1 and K2 select the *ground* and the *pattern generator* respectively. Through the control of the 1st tap coefficient (C_1 in Fig. 3(b)), the XTalk canceller along with the TX generates binary waveforms with an adjustable level, called Analog Input (AI), to the RX. Meanwhile, the *pattern generator* synchronized with the CDR asserts the binary signal to the delay-line in the DFE, called Digital Input (DI). The waveforms shown in Fig. 12 are examples for the AI and the DI signals. Each of them is a NRZ signal with its pulse width equal to the period of one data bit T, and is asserted repeatedly, once in every tap_count cycles. By adjusting the time relationship between the DI and AI pulses, shown in Fig. 12, we can choose a tap in the DFE to test and examine the functionality of the adaptation engine simultaneously. For example, testing the 1st tap requires AI(1) and DI(1), and testing the 2nd tap requires AI(1) and DI(2) which leads DI(1) by one cycle. After the convergence of the adaptation process, the normalized coefficient value of the tap under test should become 1, and others would be forced to 0. By examining all coefficient values, one tap is tested. We iteratively test the taps – one tap for each iteration.

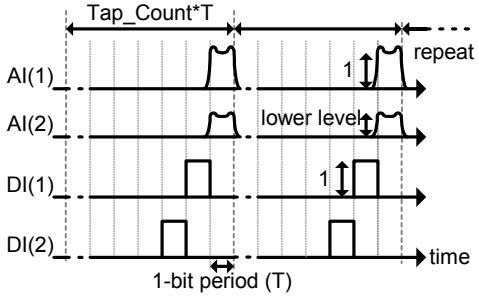


Fig. 12. Waveforms of signals AI and DI

Typically, the ISI distortion is smaller than the data signal. Thus, the full swing of the tap weighted signals in the DFE is typically designed to be smaller than the swing of the data signal [15]. For such cases, the expected coefficient value of the tested tap would not be 1. Therefore, we have to adjust the level of AI(2) to be lower than AI(1), as shown in Fig. 12. With this adjusted level, the new coefficient value of the tested tap will be the ratio of the AI(2) amplitude to the DI amplitude, which is less than 1.

To illustrate the fault detection capability of the proposed test method, we analyzed 3 different fault scenarios in the 5-tap DFE, and only consider single-fault instances for the purpose of illustration. The first two scenarios are the same as two previously used examples: a DFE with a stuck-at-zero 5th tap and a DFE with a 10% DC offset voltage. The third fault is a gain error occurred in the 5th tap for which the tap can only drive 80% of the expected voltage to the summing circuit in the DFE.

We individually test the DFE with 3 different faults by applying the signals of AI(1) and DI(5) which leads the DI(1) waveform by four cycles. The tap coefficients of the fault-free and faulty DFE with these 3 fault scenarios are shown in Fig. 13. When the first fault is present, the coefficient of the 5th tap (in Fig. 13(a)) changes from 1 to 0. It is interesting to note that the coefficients of the other taps are no longer 0 for the faulty circuit. During convergence, all tap coefficients are adjusted so that the equalizer output produces the optimal estimation for ISI reduction. In the presence of the broken 5th tap, the other taps work together to minimize the error $\varepsilon(k)$ in Fig. 8 before reaching an equilibrium. This explains why the coefficients of the other taps would also be affected when a tap is broken. Most importantly, the coefficient difference between the fault-free and the faulty DFE is significant.

For the second faulty circuit which has a 10% DC offset voltage, the tap coefficient of both fault-free and faulty DFEs are captured and shown in Fig. 13(b). The difference between these 2 sets of the coefficients indicates how the

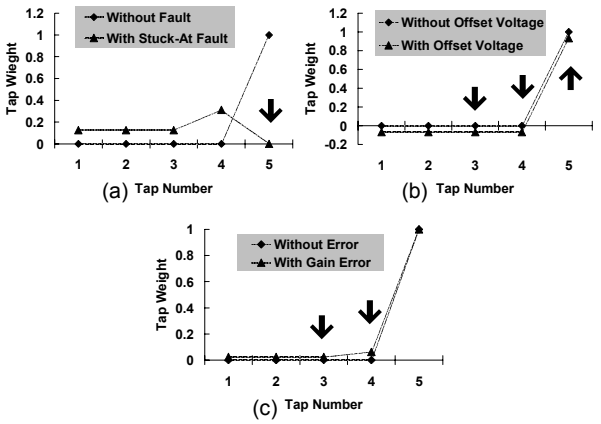


Fig. 13. Tap coefficients with and without defects. (a) Stuck-at-0 fault at 5th tap. (b) DC offset. (c) Gain error at 5th tap

offset voltage impacts the DFE. In the faulty equalizer, all tap coefficients are decreased by 10% of the full swing.

For the third fault, a 20% gain error of the 5th tap, the coefficients of both fault-free and faulty DFEs are shown in Fig. 13(c). In the faulty DFE, although the correct coefficient of the 5th tap was captured (i.e. 1), the gain error results in a 20% reduction from the fault-free voltage level. Therefore, the other taps, along with the 5th tap, attempt to jointly compensate the loss during equalization. The coefficients of the other taps, accordingly, will no longer be 0 after convergence. On the other hand, by adjusting the AI(1)'s amplitude, which results in a waveform like AI(2) of Fig. 12, we can further diagnose and identify the fault. With the stimulus AI(2) whose pulse height is 20% lower than that of AI(1), the 5th tap coefficient in the faulty DFE is 1, instead of the expected coefficient value 0.8 for the fault-free DFE. By such simple analysis of the captured coefficients, the defect can be located in the driving gain of the 5th tap. Similar adjustment to the test stimulus can be derived to diagnose other faults including missing steps and non-linearity in the taps.

These examples illustrate the characteristics of our test method. For each class of fault types and for each fault location, we can derive the ideal test stimulus for maximizing the differences in the tap coefficients.

5.0 Summary

We propose a DfT technique for advanced serial-link transceivers which include a CDR, a DFE, and an XTalk canceller inside. The hardware requirement for the DfT solution contains only one shift-register chain with a small number of flip-flops, one simple digital pattern generator in the DFE, and 3 full-swing taps in the XTalk canceller. The overhead and the additional design effort are modest. More importantly, with the proposed DfT solution, the transfer characteristic of the CDR in the RX can be examined, and the DFE can be characterized and tested without direct access to the DFE output. This alleviates the need of external instruments for jitter testing and the need for observing the equalizer output, which are often infeasible in the high-volume production environment. Furthermore, the examples provided in the paper indicate that various types of faults in the testable DFE can be detected by the proposed method, whereas the conventional method, which examines the eye-opening at the DFE output, might not be adequate for fault detection.

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