Low-g Accelerometer Fast Prototyping for Automotive Applications

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Abstract

This paper presents an application of the ISIF chip (Intelligent Sensor InterFace), for conditioning a dual-axis low-g accelerometer in MEMS technology.

MEMS are nowadays the standard in automotive applications (and not only), as they feature a drastic reduction in cost, area and power, while they require a more complex electronic interface with respect to traditional discrete devices. ISIF is a Platform On Chip implementation, aiming to fast prototype a wide range of automotive sensors thanks to its high configuration resources, achieved both by full analog / digital IPs trimming options and by flexible routing structures.

This accelerometer implementation exploits a relevant part of ISIF hardware resources, but also requires signal processing add-ins (software emulation of digital DSP blocks) for the closed loop conditioning architecture and for performance improvement (for example temperature drift compensation).

In spite the short prototyping time, the resulting system achieves good performances with respect to commercial devices, featuring a 0.9 mg/√Hz noise density with 1024 LSB/g sensitivity on the digital output over a +/- 2g FS, and an offset drift over 100°C range within 30 mg, with 2% of FS sensitivity drift. Miniboards have been developed as product prototypes, consisting of a small PCB with ISIF and accelerometer dies bonded together, firmware embedded in EEPROM and communication transceivers.

1. Introduction

The automotive market is requiring an always growing number of sensing elements, to be employed in numerous electronic systems: a car is estimated to feature about 100 sensors and the cost of electronics covers at least 30% of the total. Inertial sensors, in particular accelerometers, fulfill most of the sensing activity provided in a vehicle. The use of accelerometers to sense rapid deceleration in Automatic Braking System (ABS) is well acknowledged, however accelerometers are used in many sensing applications in cars and trucks: sensing for airbag control (SRS, based on detection of vehicle acceleration); Electronic Stability Control (ESC, VSC or VDC), which assist the driver when the vehicle starts skidding; active suspension (accelerometers monitors road conditions for hardening or softening suspension for safety and comfort); electronic parking brake (for applying a desired braking force depending on land inclination); Rollover Stability Control (RSC, similar to ESC); Adaptive Cruise Control (ACC, concurring to create a virtual description of the traffic) , anti-theft system (incorporating tilting detection) and GPS navigation dead reckoning assist.

Mechanical and electromagnetic devices have proved to fit well the first applications in the near past, but nowadays they are outperformed by the new generations of MEMS sensors, which guarantee remarkable savings in cost, area and power consumption. As a drawback they require effective electronic interfaces for signal conditioning and processing, in order to achieve high performances and reliability and be integrated with the modern ECUs (Electronic Control Units handling data of several sensors and being part of complex electromechanical systems). As a last issue, the evolution rapidity of automotive applications makes the sensor time-to-market a killing factor, in order to be competitive in such a quickly changing scene: the electronic interface has to be both optimized on the target sensor (for performance reasons) and fast developed and updated according to the sensing element progresses.

A first approach in this direction was the concept of Universal (or Generic) Sensor Interface [1], which undoubtedly succeeded in solving the time-to-market issue (the same interface could be configured for working with different sensor types) but at the same time it proved to be unfit for the high standards required by the automotive market, as the USIs inevitably feature power and area overheads due to the sub-optimal architecture, as well as a worsening in overall performances.

A more recent approach consists in employing the Platform Based Design methodology [2], which consists in the definition of a sequence of abstraction layers (each

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of them considered a Platform), each one including a set of modules, interfaces, and services that should be as much as possible configurable. They are assembled taking into account the wide-ranging signal conditioning electronics for different sensors classes, in a way that from such generic platform, the optimum interface for a specific sensor can be easily derived by means of system simulation, verification and prototyping. This design flow is indeed the best way to implement an area and power optimized interface, with best performances, yet it can find its weak point in the necessity of comprehensive and accurate simulations, at the system level stage, in order to choose the fittest architecture. They may require conspicuous design space exploration time and often do not guarantee a good matching with the post implementation results (mostly because of the discrepancies between sensor or blocks models and their actual implementations).

This paper presents the development of a dual axis accelerometer interface using the ISIF platform [3], a mixed signal system-on-chip conceived to speed up and ease a Platform Based Design Flow for optimized sensor interfaces. In section 2 the accelerometer operating principle is depicted, in section 3 ISIF architecture is disclosed, while in section 4 implementation details are provided.

2. Physical description of accelerometer

Low-g micromachined capacitive accelerometers are commercially successful inertial sensors. There are many different types of capacitive accelerometers but their basic structures are very similar. They typically consist of a proof mass suspended by beams anchored to a fixed frame [4]. The presence of an external acceleration displaces the support frame relative to the proof mass, thus changing the capacitance between the proof mass itself and a fixed conductive electrode separated from it with a narrow gap. This technique is carried out using two main basic structures: the vertical and the lateral one. In the vertical structure the proof mass is separated by a narrow air gap from a fixed plate, forming a parallel plate sense capacitance. In this case the sense direction is perpendicular to the proof mass plane as shown in figure 1 (z-axis).

In a lateral accelerometer, fingers extending from the proof mass (sense fingers) are interdigitated with fixed fingers, forming parallel differential capacitor elements. In these devices the proof mass moves along its plane as shown in figure 2 (x-y plane).

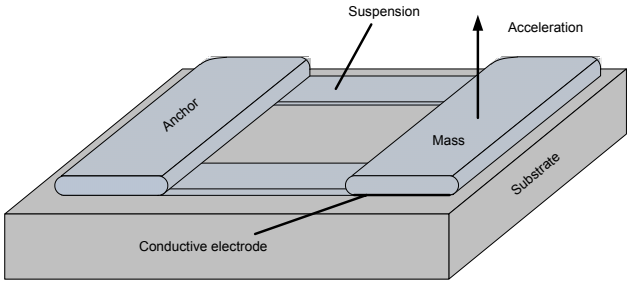

Figure 1: vertical structure

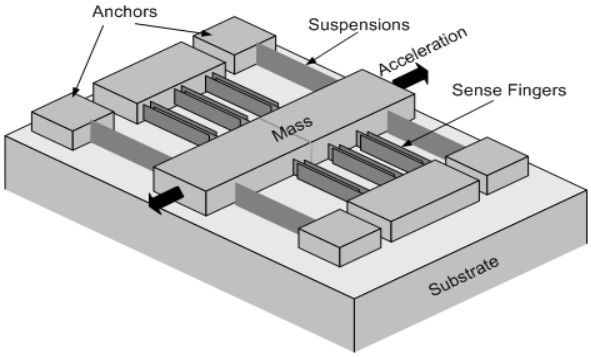

Figure 2: lateral structure

Typical values of sensing capacitances in low-g accelerometers are 1-100 pF.

A critical role in the sensor design is played by the proof mass, its size and its spring constant. Anyway the sensor design itself is not sufficient to guarantee a successful product. The package has to protect the structure without inducing significant stress or drift and without affecting negatively the frequency response or the temperature sensitivity. Also a sensor tilt can introduce an error in DC measurements or slightly change the sense direction. Any accelerometer product must also include the electronic interface that has to properly condition the sensor in order to enhance its performances. Readout circuits mostly use capacitance-to-frequency converters [5], [6], capacitive AC-bridges [7] or switched capacitor circuits [8]. Sometimes switched capacitor circuits are utilized to implement the correlated double-sampling technique in order to reduce the effect of 1/f noise [9]. Moreover accelerometers can be operated open loop or closed loop. The open-loop solutions are inherently stable and they require simpler circuitry but the linearity, band-width and dynamic range can't be better than the sensor itself. The closed-loop solutions improve these performances at the cost of a more complex circuitry and risks of instability.

3. ISIF architecture

In Figure 3 ISIF platform block diagram is depicted. The digital section is composed by the LEON core, a 32-bit RISC processor developed and freely distributed by European Space Agency under LGPL license, together with standard peripherals for communication with external devices, memories and buses (AMBA APB/AHB).

The analog section features a wide range of IPs for sensor signal acquisition, driving and basic analog conditioning such as DACs, ADCs, amplifiers, filters, and current/voltage sources.

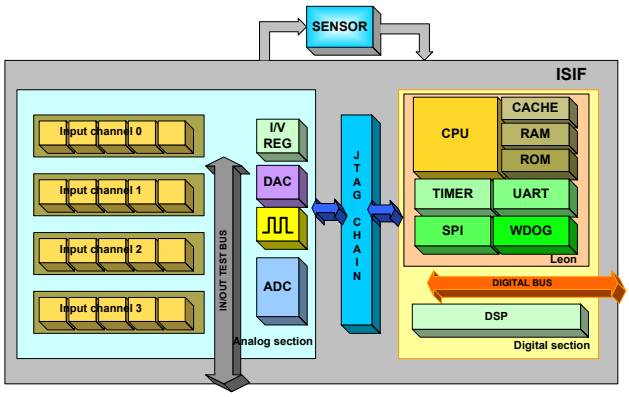

Figure 3. Platform architecture

ISIF platform has been implemented in BCD6 STM technology, the whole system is integrated into a single chip with area occupancy of about 72mm^2 (Figure 4).

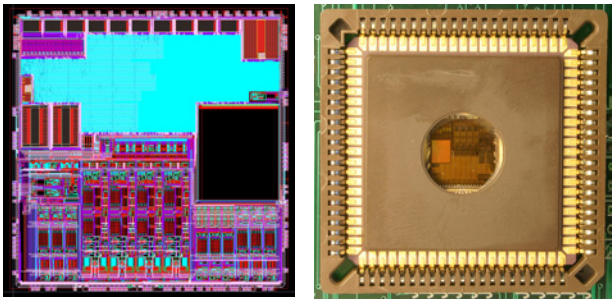

Figure 4. ISIF layout and chip photo

3.1. Analog section

ISIF analog section is based on 4 input channels for signal acquisition, each channel is composed of different stages as we can see in Figure 5. First an input charge amplifier is able to detect voltage, current or capacitance (thus covering the most of sensor typologies). After signal acquisition, differential amplifiers, low pass filters and level shifter provide proper analog conditioning with a high degree of configurability. Then the signal properly filtered and adjusted in gain and dynamic is converted by the Sigma Delta ADC. Additional analog blocks provide voltage/current references, oscillation for clock generation and DACs are used for sensor driving.

An input/output test bus is provided to supply stimuli and to probe output signals for each block. It represents a key issue for an effective and quick debug of the signal conditioning path.

A peculiarity of this system is the accuracy in design for improving the noise margin (e.g. the analog and digital supplies are separated) and that the digital bits for block configurations are handled by a JTAG-like approach, thus bits programming is simply realized with shift registers to overcome clock skew issue guaranteeing a safe communication between digital and analog structures.

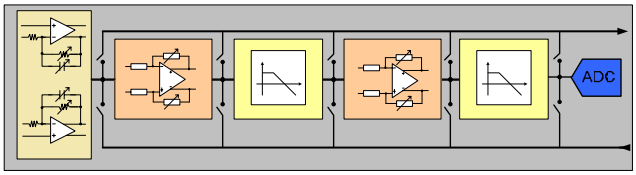

Figure 5. Input channel scheme

3.2. Digital section

The digital hardware section is composed of a CPU core with related peripherals and dedicated IPs for DSP purpose. CPU block (see Figure6) includes the LEON a general purpose processor based on a 32-bit RISC SPARC-V8 compliant architecture which features hardware multiplier and divider, interrupt controller, memories busses and peripherals for communication. The hardware digital signal processing block is made up of dedicated IPs optimized for low power consumption such as modulator and channel demodulators, a 6 DAC controllers, filters (FIR and IIR) and sine wave generator which can provide up to 16 waves with 3 different frequencies and programmable phases. The interconnection among these IPs can be hardware or they can be directly accessed at their input/output by software. The high flexibility of DSP section and CPU potentiality allows designers to implement complex and ad hoc algorithms for the target sensor conditioning, for example a digital PLL has been fully implemented and tested on a fast prototyping board [3]. LEON processor features system monitoring and controls signal processing chain and communication with external devices. The digital section is completed by standard peripherals such as timers, watchdog, SPIs (Serial Peripheral Interface), UARTs (Universal Asynchronous Receiver Transmitter) CACHE, ROM RAM and EEPROM memories as shown in Figure 6. Part of the software is included in ROM (boot

and few utility functions), while the rest can to be downloaded at startup via UART, or can be stored in external SPI EEPROM and so directly reboot from EEPROM (which can hold different software and data to speed up time in trimming and test procedures). Firmware utilities can change interconnections among digital IPs, handle communications with external devices (for debug, monitoring) and configure the whole analog front end section (adjusting parameters such gain, bandwidth e.g.) to match requirements of different sensors.

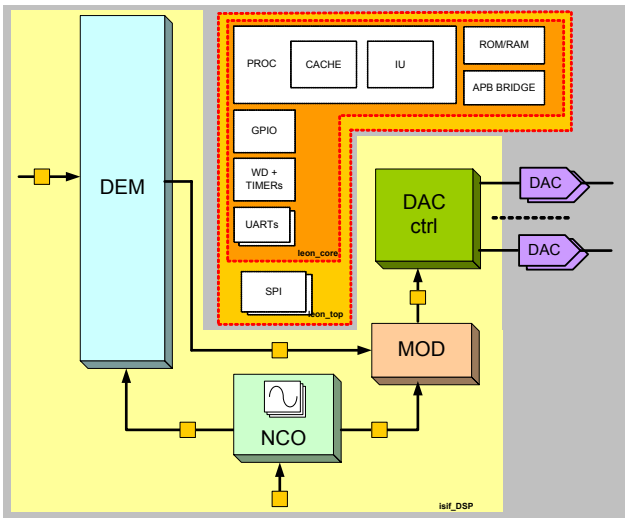

Figure 6. LEON and Digital hardware IPs

3.3. Software section

The strict automotive application requirements are pushing toward the use of hardware solutions (especially in term of safety), on the other hand presence of non-linearities, and quantity uncertainty make a right first time hardware implementation really difficult. Furthermore several digital IPs require detailed analysis for proper parameters setting, in fact automotive application often requires high performances together with reduced area that is not compatible with a module featuring a large number of configuration bits for trimming. To meet these requirements ISIF platform includes software peripherals (filters, controllers e.g.) with an exact matching with hardware devices. The LEON processor offers good signal processing features (hardware multipliers and accumulation) and guarantees flexibility and required computational power for real-time software IPs implementation. It is worth noting that the aim of this platform is not tended towards the direction of achieving the best performances, but lies in the maximum accurate emulation of a complete hardware optimized sensor interface (which could hardly afford such an area and power consuming processor). So the most common functionalities, which are not fulfilled by ISIF digital section, are modeled by software routines keeping the same behavior of the original DSP library IPs (concerning bits width, saturation, linearity e.g.). A DSP software environment allows input/output data from digital IPs to be acquired by routines, afterward elaborated and passed back to physical blocks: just as the data elaboration would have been realized completely hardware. The monitoring, control and communication functionalities are implemented via software too with a twofold benefit: flexibility is guaranteed and possible updating due to system modifications and new requirements.

These features help the designer to find out the most proper solution in DSP elaboration for a target sensor. With a Personal Computer connected via UART to the ISIF board the designer can quickly explore a wide project design space, changing analog settings, interconnecting digital IPs and even instantiating new ones in order to achieve architecture optimization both in terms of area and performances. The design space exploration and all analysis are realized since the first step of interface concept with the target sensor connected to the ISIF board.

In the final ASIC device, software routines can be quickly replaced by corresponding hardware IPs with a zero risk and cost for redesign minimizing time to market.

4. Implementation of YZ accelerometer

In this section an ISIF implementation with YZ dual axis accelerometer is described. Such accelerometer features an in-plain moving structure which shifts on Y axis when subject to an acceleration, causing a ΔC variation of about 10 fF/g in the sense capacitances, whose rest value is about 10 pF. The Z moving structure, instead, is subject to a torque under acceleration, thus featuring poor linearity, but is provided with feedback electrodes in order to implement a closed loop conditioning: up to +/-4 g acceleration can be compensated, making possible the closed loop architecture in the target low-g range of +/-2 g.

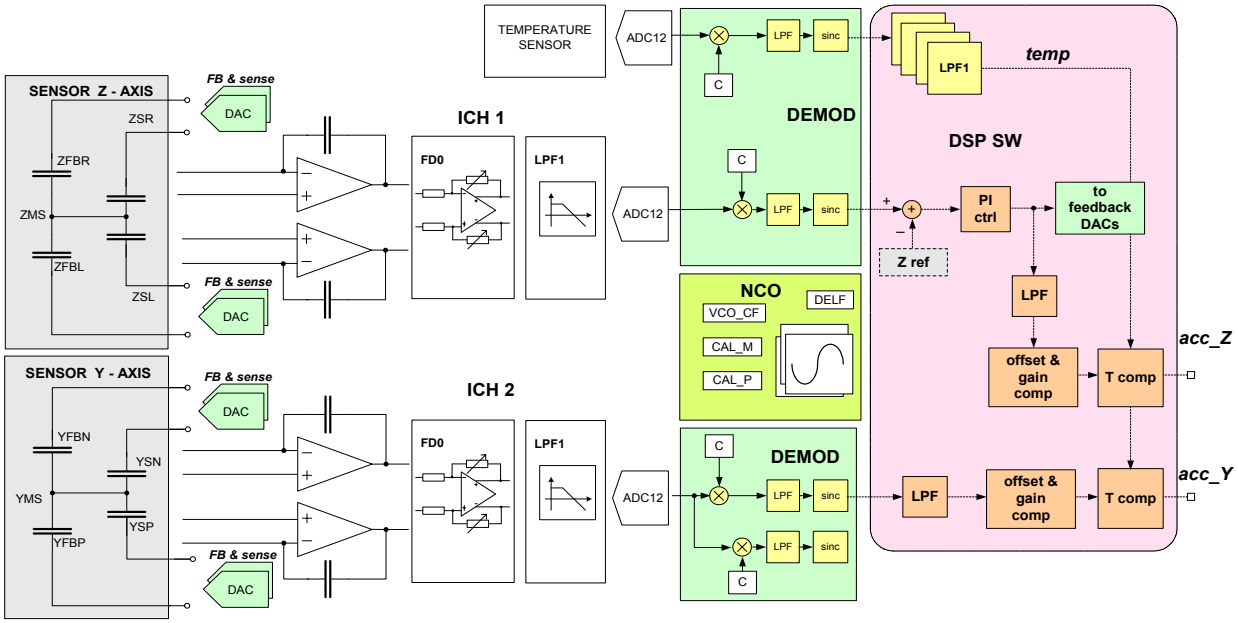

Figure 7. ISIF plus accelerometer architecture

The slight ΔC variation in low-g applications makes necessary a differential capacitance reading (provided by ISIF charge amplifier Figure 7). The input channel stages perform a further low pass filtering (the sensor features a mechanical damping on Z at less than 500 Hz, while Y axis has a resonating peak at about 1800 Hz) and gain adjustment, so that the input dynamic of the 12 bit ADC converter can be fully exploited. The digital section decimates the ADC output and low-pass filters, while software-emulated IPs complete the signal processing chain. Closed loop is implemented on Z axis by reference subtraction, PI controller and feedback actuation, being the acceleration value calculated as the difference between feedback driver inputs. Such signal requires further filtering (down to the target bandwidth of 10 Hz), offset compensation and gain correction in order to have the chosen sensitivity. Signal coming from Y axis (open loop) is directly fed through low pass filters and offset / gain correction stages.

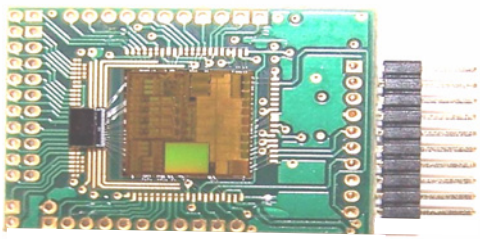

Figure 8. Miniboard setup.

Comprehensive studies on the influence of temperature on the combination of sensor and interface have revealed an almost linear trend of offset and sensitivity over T. For this reason a software T drift linear compensation has been set up, including ISIF temperature sensor readout, low pass filtering, and measured T employment for calculating offset and gain correction additional coefficients. Accelerometer firmware basically works on the execution of the DSP routine (all the emulated digital IPs such as filters, PID controllers, adders and multipliers are included here) on a time schedule given by data valid coming from hardware at about 1 KHz. The remaining time (within two interrupts) is used to handle communication resources such as UART and SPI (both can be used for sending commands and reading outputs) and to perform non time-critical calculations (like updating T drift compensation coefficients using the latest T reads). The firmware also includes a series of procedures conceived to automatically trim a module, which can be started by a UART or SPI command. First, Z reference has to be set with an average value read at the end of analog and digital signal conditioning when the sensor is in Z = 0 g position, then loop can be closed with confidence on the fact that the moving structure will stay in its rest position (thus improving linearity). Another procedure, to be started when the sensor is rotating along the sensitive axis at about 25 °/s, detects maximum and minimum acceleration values on both axes in order to compensate offset and set gain coefficients for the target sensitivity. The same routine, run with the sensor inside the climate chamber at three different temperatures, allows calculation of 2 linear trend lines both for offset and sensitivity, so that with proper conversion factors T compensation coefficients can be calculated at runtime

(trend lines are estimated within the ranges $T_{low} - T_{env}$ and $T_{env} - T_{high}$). The described implementation has been first evaluated with setups made by a PCB hosting two CLCC84 sockets for ISIF and accelerometer. A smarter setup is depicted in Figure 8 it consists in a very small PCB (about 3 cm^2 area) with ISIF and sensor dies glued on and bonded together, then covered by a cap. Such setup minimizes interconnection parasitics and is fit for commercialization. Thanks to its reduced size it also allowed parallel trimming and characterization of several modules in the turning table, with noteworthy time savings.

5. Results

The system provides digital output via UART or SPI, with sensitivity of 1024 LSB/g and FS of +/- 2g. The noise, which can also be evaluated by firmware, stays within 3 mg for both axes.

A mechanical setup has been developed to allow fast automated trimming of up to 6 modules simultaneously. It consists in a hard framework attached to the rotating plate of the turning table, provided with lodgings and blocks for the sensors. Tuning screws allow the support and lodgings orientation to be changed, in order to let sensors rotate fully exploiting the gravity force on both axes: the +/- 1g reference is used both for sensitivity trimming at T environment and for trimming over T (at -20°C, +30°C and +80°C). Automation is implemented by a LabVIEW interface, which sends the same SPI commands sequentially to each module and reads the answers. This procedure resulted in a max offset drift of 20 mg on Y and 40 mg on Z, and with sensitivity error within 1% of FS on Y and 3% of FS on Z.

With respect to commercial devices, as for example ADXL322 [10], this implementation features a slightly higher noise but better 0 g offset and stability over T.

6. Conclusions

An ISIF application for conditioning a dual-axis low-g accelerometer in MEMS technology has been presented. ISIF is a Platform Based System on Chip, accomplishing fast prototyping of several kinds of automotive sensors thanks to its high configurable architecture, featuring fully programmable analog and digital IPs for trimming and flexible routing structures. It has been implemented by Sensordynamics AG in 0.35µm BCD6 technology.

This accelerometer implementation brings to light ISIF potentialities for fast and effective sensor interfacing in the prototyping phase. Relevant part of ISIF resources, both analog and digital, has been exploited, furthermore signal processing required add-ins (software emulation of digital DSP blocks) for sensor conditioning in closed loop and for performance enhancement (e.g. temperature drift compensation). The presented system, despite the short prototyping time, displays good performances with respect to commercial devices, featuring a 0.9 mg/√Hz noise density with 1024 LSB/g sensitivity on the digital output over a +/- 2g FS, and an average offset drift over 100°C range of 30 mg, with 2% of FS sensitivity drift. A 3 cm^2 PCB housing both ISIF and accelerometer dies bonded together, with firmware embedded in EEPROM and communication transceivers, has been worked up as product prototype.

7. References

[1] J. Zhang; J. Zhou; Balasundaram, P.; Mason, A.; "A highly programmable sensor network interface with multiple sensor readout circuits Sensors" Proceedings of IEEE , Volume: 2, Pages:748 – 752, 22-24 Oct. 2003

[2] Sangiovanni-Vincentelli, A.; Martin, G.;" Platform-based design and software design methodology for embedded systems" Design & Test of Computers, IEEE Volume 18, Issue 6, Nov.-Dec. 2001 Page(s):23-33

[3] F. D'Ascoli, M. Tonarelli, M. Melani, M. De Marinis, a. Giambastiani, L. Fanucci, "Intelligent sensor interface for automotive applications" ICECS2005 Gammarth Tunisia Dec 11-14.

[4] N. Yazadi, F. Ayazi and K. Najafi, "Micromachined Inertial Sensors", Proceedings of the IEEE, 1998

[5] M. S. Smith, L. Bowman, and J. D. Meindl, "Analysis, design, and performance of micropower circuits for a capacitive pressure sensor IC," IEEE J. Solid-State Circuits, vol. SC-21, pp. 1045–1056, Dec. 1986.

[6] Y. Matsumoto, M. Esashi, "Low drift integrated capacitive accelerometer with PLL servo techniques," in Tech. Dig. 7th Int. Conf. Solid-State Sensors and Actuators (Transducers'93), Yokohama, Japan, June 1993, pp. 826–829.

[7] Jiangfeng Wu; Fedder, G.K.; Carley, L.R., "A low-noise low-offset capacitive sensing amplifier for a 50-/spl mu/g//spl radic/Hz monolithic CMOS MEMS accelerometer"; Solid-State Circuits, IEEE Journal of Volume 39, Issue 5, May 2004 Page(s):722 - 730 Digital Object Identifier 10.1109/JSSC.2004.826329

[8] Amini, B.V.; Ayazi, F., "A 2.5-V 14-bit /spl Sigma//spl Delta/ CMOS SOI capacitive accelerometer"; Solid-State Circuits, IEEE Journal of Volume 39, Issue 12, Dec. 2004 Page(s):2467 - 2476 Digital Object Identifier 10.1109/JSSC.2004.837025

[9] Junseok Chae; Kulah, H.; Najafi, K., "An in-plane high-sensitivity, low-noise micro-g silicon accelerometer with CMOS readout circuitry"; Microelectromechanical Systems, Journal of Volume 13, Issue 4, Aug. 2004 Page(s):628 - 635 Digital Object Identifier 10.1109/JMEMS.2004.832653

[10] ADXL322 Datasheet. www.analog.com