# Panel: "DFM/DFY: Should You Trust the Surgeon or the Family Doctor?"

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## Abstract

Everybody agrees that curing DFM/DFY issues is of paramount importance at 65 nanometers and beyond. Unfortunately, there is disagreement about how and when to cure them. "Surgeons" suggest a GDSII-centered approach, potentially invasive, while "family doctors" recommend a more pervasive approach, starting from RTL. As in real life, "surgery" and "medicine" represent two different schools of thought in the DFM/DFY arena. Both involve risks.

This panel will examine these two approaches from high-level design all the way to manufacturing. We have assembled a set of panelists that represent a broad cross-section of semiconductor industry. Although there is general agreement among the panelists that both approaches are necessary and that prevention is the best way to proceed, they also acknowledge that the surgery may be unavoidable in such "hazardous" conditions as state-of-the-art technologies.

However, as always, "the devil is in the details," and the diverse approaches to DFM presented below should make this panel quite interesting. We are also counting on the feedback from the IC design community to assess if these approaches are sufficient and practical enough to deal with the "health hazards." We are looking forward to an exciting discussion that will challenge our esteemed panelists.

## Panelists' Position Statements

### Rob Aitken, ARM Ltd.

The facile answers to the question of should you trust your family doctor or your surgeon are that you should trust both, or neither. These answers skate over some subtlety, however, both in medicine and in DFM. In both cases, the key to good health is a rigorous approach to preventative care, with the goal of resorting to surgery only when absolutely necessary. In the DFM context, this is especially important when using and developing IP (here the medical analogy breaks down). A key aspect of the IP use model is that IP is designed to be reused, and as such is somewhat independent of the context in which it is eventually used. In addition, from a designer's perspective the purposes of using IP include saving time and achieving a certain level of quality. IP that does not include preventative DFM medicine has the potential to fail in both areas.

Within physical IP, there are numerous preventative approaches that can be applied. For lithography issues, options depend on the type of IP. A key issue is maximizing DFM compliance without unduly increasing area. For some classes; e.g. I/O and analog IP, all foundry DFM recommendations can be followed. For standard cells, a strict set of metrics can be defined and implemented, managing issues such as metal and poly fill, adjacency analysis, RET suitability enhancement, and critical area optimization, as well as the tradeoffs that arise between them. Additional details have been reported previously [ISQED 06]. For memory, the same approaches can be applied to leaf cells, and additional wide area effects can be managed as well, including density management and boundary optimization between the memory and adjacent blocks of standard cells. For soft IP, recommendations for use of physical IP as well as DFM-friendly reference flows can be provided. Beyond pure lithography optimization, timing effects of both lithographical and wiring variation can be accounted for.

In each of these cases, a challenge for "family doctor" style approaches is lack of data: when IP is being developed, mass production in a process node has not begun, so subtle effects are often unknown. Careful design practices can anticipate some issues and avoid them, but the process cannot be perfect.

978-3-9810801-2-4/DATE07 © 2007 EDAA

Similarly, a challenge for "surgery" is lack of patient history, which in this models case design intent. Just as the appropriate treatment of a torn ligament will change depending on whether or not one intends to participate in an upcoming triathlon, so too the appropriate treatment for design issues changes depending on the criticality of the circuit, the yield and performance targets of the design, and so on. A rectangle may be more than a rectangle, depending on the context.

Of course, no matter how much preventative medicine is used, it's good to know that a surgeon is available if you need one, but high quality care from the family doctor can both reduce the likelihood of surgery as well as improving the prognosis should it become necessary.

**Antun Domic, Synopsys, Inc.**

Twenty years ago, at 1.5 microns, i.e., 1,500 nanometers, all that engineers needed to sign-off were: design's schematic, cell library data book, and a calculator. Unfortunately, since then, things have got more and more complex.

Ten years ago, at 250 nanometers, transistors and interconnect could not be handled separately by stand-alone logic synthesis and P&R; physical synthesis was introduced, bringing together the logical and the physical world to slash the number of iterations required to successfully converge on timing and area.

Today, at 65 nanometers, it's the design and manufacturing that can no longer be handled separately; physical synthesis has been extended to encompass DFM/DFY, slashing once again the number of iterations and re-spins, which would be inevitable to correct the thousands of problems detected at GDSII.

GDSII is just too late and too costly for the correction of topologies which may be critical for particle-induced defects, CMP, or lithography-related issues

Yield-rated synthesis, power network synthesis, vias minimization and timing-driven redundant vias insertion, timing-driven wires widening and spreading, timing-driven metal fill, variation-aware extraction and static timing analysis are just some examples of the rich arsenal of weapons available within the design implementation flow to prevent problems before they occur.

Surgery is not bad per se, but prevention is better.

**Carlo Guardiani, PDF Solutions, Inc.**

The importance of Design for Manufacturing (DFM) has increased as the semiconductor industry turned the corner of nanometer technologies (90/65/45nm).

As predicted by PDF Solutions a few years ago, this is dictated by the fact that the yield of complex SoC products with new technologies is increasingly dominated by systematic and variability effects that are probabilistic functions of the actual circuit layout properties.

In fact when the main type of yield detractor mechanisms were represented by particle contaminants and random defects, there was little need for the designers to pay attention to the yield implications of alternative design choices, beyond design rule and healthy design practices such as for example using contact and via redundancy, staying away from minimum spacing and minimum dimensions in general unless strictly required, etc.

After all an healthy lifestyle, lots of vitamins and a good cotton undershirt are sufficient in the flu season for the average people, so they don't need to take any medicines or see the doctor unless they get sick

However as circuit performance requirements get tighter, thus inherently driving process technology to always more advanced and complex territories such as immersion lithography and new gate and interconnect materials and engineering, healthy design styles and Design Rule compliance are no longer sufficient to guarantee IC product's yield.

In fact every process technology is characterized by a unique set of yield sensitivities that is determined by the particular choice of process integration, lithography equipment and RET recipes and equipment calibration.

It is therefore impossible to predict with reasonable confidence that a particular design choice is going to be always yield savvy unless those process sensitivities are accurately quantified and their impact on product yield properly modeled.

It is similar to achieving top performance in professional sports requiring that athletes be followed by a whole medical team which performs weekly check-ups and decide what they have to eat, drink and which medicines they need to take in order to maintain them in perfect efficiency and health based on their unique, personal profile.

**Philippe Magarshack, STMicroelectronics NV**

Until 0.13 microns, if you could manufacture each structure, you could manufacture the entire chip. What you designed on the polygon layout tool was what you got on the wafer. Designers had simple design rules with simple yes/no, pass/fail criteria for the design rule checker (DRC). Using this panel's analogy, the surgeons were ruling, in the case of a rare emergency.

However, some signs of trouble were already noticeable. The semiconductor industry had entered the sub-wave-length world, and the introduction of copper interconnect at 0.18um or 0.13um was posing more challenges than had been anticipated; not only designs became more difficult to manufacture, but design rules changed from quantitative to qualitative; and the result was less deterministic, because of atoms-level random dopant fluctuation, as well as because of interconnects, processed with Litho and CMP and their associated systematic and random defects.

Today, at 65 nanometers and beyond, features are manufactured with 193 nanometers lithography, causing an order of magnitude increase in the number of defects and faults; at 65 nanometers cost of test per transistors is only 200X smaller than cost of manufacturing, versus 1600X in 2001 at 130 nanometers.

Designers and process engineers must weigh improvements in manufacturability against the effects on the design's performance, size, and functionality; they need to proactively collaborate in analyzing the variables that contribute to critical design specifications. This means that manufacturability must start at the chip design level. Family doctors, with their deep knowledge of their patient's clinical history can play a fundamental role.

It is not enough however, as some have suggested, to merely include DFM specifications in physical design and verification tools. This method does not address how various components will react to each other when integrated into a system-on-a-chip. This means being able to look across hierarchical boundaries to see how the data in one cell interacts with data outside the cell; it might be possible to improve the manufacturability of one layer by manipulating another.

This more comprehensive model requires a new infrastructure that supports a feedback loop between designer and manufacturer. The feedback loop should include means of modeling the manufacturing constraints, verifying IC layouts, and translating manufacturing-related issues for the designer. To make this feedback loop possible, a complete cultural revolution must take place whereby designers understand the constraints of the lithography experts, and conversely, the yield production engineer participates up front in the design and design-for-test reviews, inducing a design-for-yield mentality in the design teams.

In other words, the surgeon and the family doctor must consult with each other for a greater good, avoiding unnecessary surgeries, without postponing the necessary ones, though!

**Douglas Pattullo, TSMC Ltd.**

For something as important as the life of your latest (or perhaps only) chip and with it the success or failure of your company the question of who to trust as a partner is critical. The core issue however is not the skill set of a Surgeon or a family doctor but much more who really knows what they are talking about and has the customers well being as they primary focus (as opposed to theirs). Fundamental here is the knowledge of the operators, an inexperienced Family doctor perhaps straight from medical college may appear to me to be little more that a witch doctor with impressive sounding hocus pocus and the Surgeon merely a butcher with a scalpel. For the health of my chip I want to rely on somebody I know, somebody who has experience in the diagnosis and treatment of diseases and somebody with an analytical mind so that they can use their knowledge base to determine the best treatment whether that be a daily vitamin pill or triple bypass surgery. The provider of the consultation is a matter of personal choice, this might be a doctor on the National Health Service, a private consultant in Harley Street or possibly even remote diagnosis via the internet - the key point is the knowledge of the provider and quality of the diagnosis they can provide.

They key to success relies on accurately assessing the history of the patient, the apparent and hidden symptoms and then determining what further tests are required for a proper diagnosis. Based on this diagnosis the most effective treatment can be determined and an appropriate treatment specified.

In this analogy the foundries here work like a central medical records departments for the associated hospital, clinics, teaching establishments and Research groups. The Foundries may have produced test chips two years or more before the fabless guys submit their first design and have already seen the success and failure of different implementations. They will then have worked to analyze and test their hypothesis and finally capture their knowledge as far as possible with traditional design rules and spice models however they know this can not cover 100% of all cases so now they need to formalize and share that extra of knowledge with the operatives in the field.

The foundries need a healthy chip industry with fast ramps on each new technology in order to recoup their investments in each new node and in turn to then finance the transition to the next technology, however they also wish to protect their investments and design partners, thus the complete opening of the Kimono can not be done on centre stage in front of all and sundry where it would shock and confuse those not expecting it whilst

potentially disclosing their "secret sauce" to competitors. The information required by designers (and Surgeons and Family Doctors) needs to be presented in an understandable, usage fashion using a language appropriate to its audience without damaging the source of that data.

For these reasons TSMC has pioneered the DUF (DFM Unified Format) which enables it to share essential manufacturing knowledge in a model based format in such a way that it can be easily used in the used by all parties in the domain they are familiar with whilst protecting the integrity of their intellectual property. Working in close collaboration with more that 20 partners DDK (DFM Design Kits) based on this DUF are now available for of TSMC's most advanced technologies. This ability to share and disseminate knowledge thus enables trust to be built up within the whole supply chain so that you know that your chosen medical professional is basing their treatment based on scientific facts and will quickly restore your good health."

**Joe Sawicki, Mentor Graphics Corp.**

The metaphor is apt. If you never go to the doctor, live an unhealthy lifestyle, and expect everything to get taken care of by the surgeon when things go wrong, live isn't going to be particularly pleasant.

On the other hand asking your family doctor to do bypass surgery may lead to a disappointing outcome.

It is critical to embed DFM concepts into the design creation phase. Just as you don't want to leave every health problem to the surgeon, waiting until you have completed the design phase to consider DFM issues will be a disaster.

In a recent customer engagement we analyzed routing from two different tools for litho hot spots. In one moderately sized case, one of the tools gave approximately six hundred category 1 errors. The other tool gave three. Three errors give a fairly easy ECO cycle, six hundred mean the chip will either be significantly delayed or yield badly.

Given the need to embed DFM into the design creation cycle, why not just handle all issue there.

Two fundamental problems:

The first is that algorithmically you want to be looking at different things between a "family doctor" design creation tool and a "surgeon" DFM tool. The design creation tool is focused on exploring an almost infinite solution space by constraining the topological exploration and getting things to meet an increasingly difficult spec. This spec has become increasingly difficult over the years as it has moved from having to meet basic ground rules like width and spacing to also having to meet issues of timing closure, signal integrity, and now DFM constraints. In all cases the computational complexity of the task means that simplified models capable of on-the-fly analysis are critical. In the case of all these specifications a corresponding sign-off tool has been necessary. The sign-off tool only has to explore the single solution produced by the creation tool and can afford more computational complexity.

The second is that we can only build in DFM effects to the creation tool that existed in the previous node. A great example of this is via doubling. Though the technique had been around for years, it only became critical with the 130nm node because of copper voiding. Adding via-doubling to the design creation tools requires changing the architecture of the tool. Adding via-doubling to a DFM tool requires writing a script. Virtually all via-doubling through the 90nm node was done with DRC scripts.

In the end each has an important role to play. The "family doctor" needs to make sure that the design is delivered downstream meeting the vast majority of manufacturing requirement. The "surgeon" DFM tool needs to have sophisticated, flexible analysis and improvement algorithms in place to handle the last (and thereby the most difficult) problems. And both need to work in consultation with each other to ensure the health of the patient.