

# Design of High-Resolution MOSFET-Only Pipelined ADCs with Digital Calibration

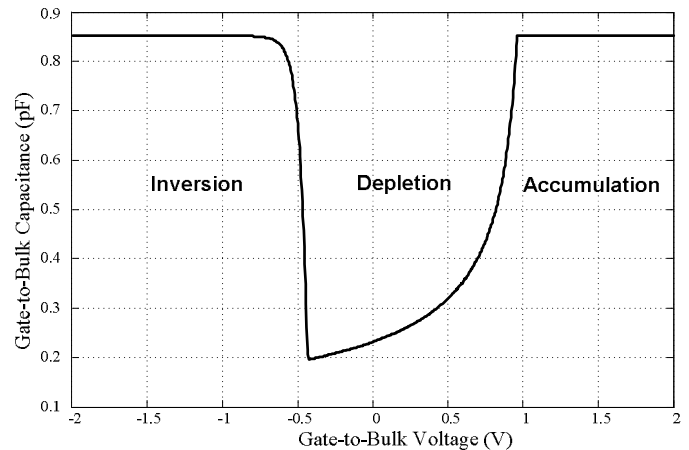
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## Abstract

*Design of low-voltage high-resolution MOSFET-only pipeline analog to digital converters (ADCs) has been investigated in this work. The nonlinearity caused by replacing linear MIM capacitors with compensated depletion-mode MOS transistors in all 1.5-bit residue stages of the ADC has been properly modeled to be calibrated in digital domain. The proposed calibration technique makes it possible to digitally compensate the nonlinearity of a 1.8V 12-bit 65MS/s MOSFET-only ADC in 0.18 $\mu$ m standard digital CMOS technology. It improves the values of signal-to-noise-plus-distortion-ratio (SNDR) and spurious-free dynamic range (SFDR) by approximately 27dB and 35dB respectively.*

## 1. Introduction

Pipelined analog-to-digital converters (ADCs) are used extensively in a wide range of high conversion rates and medium-to-high resolutions. Linear capacitors such as metal-insulator-metal (MIM) or poly-insulator-poly (PIP), necessary to realize switched-capacitor stages, could only be implemented when employing extra process layers, not available in standard digital CMOS processes. Employing such extra layers would increase the cost of fabrication. To realize capacitor in standard digital technologies, the gate-to-bulk capacitance behavior of a MOS transistor called as MOSCAP could be used as an alternative choice. Compared to linear capacitors, these capacitors benefit from lower mismatch and larger capacitance per unit area. The main obstacle which limits the utilization of MOSCAPs is their highly dependency on the voltage across them. This is due to different regions a MOSFET experiences when its gate-to-bulk voltage varies. These regions that are shown in Fig. 1 are accumulation, depletion and inversion respectively. While the variation in the capacitance value is not very large in accumulation, this capacitance is highly nonlinear in depletion region [1]. A DC source-to-bulk bias voltage can be applied to force a MOSCAP working in accumulation or strong inversion [2], [3]. But as providing such voltages may not be



**Fig.1 Simulated C-V characteristic of a p-channel MOSFET (W=L=10 $\mu$ m)**

feasible in low-voltage submicron applications, depletion biasing of MOSCAPs is inevitable. As a result, the depletion-mode MOSCAP behavior could be modeled as a nonlinear capacitor.

The nonlinearity caused by employing depletion-mode MOSCAPs in pipelined ADCs would increase the conversion distortion. Hence, the value of ENOB that shows the amount of valuable information in digital output is considerably decreased. In this work, the nonlinearity caused by MOSCAPs in analog stages is modeled. To digitally compensate the mentioned error, the inverse nonlinear transfer function of analog domain is then digitally implemented by using this model. Thus all the advantages of realizing a MOSFET-only analog domain of an ADC could be benefited while its nonlinear behavior is digitally compensated. In this paper, the behavior of a depletion-mode MOSCAP is initially modeled in section 2. The models are then used to predict the operation of a 1.5-bit residue stage in section 3. It is also compared with simulations in that section. Next, in section 4 the details of the calibration algorithm for suppressing the capacitor nonlinearity of a 12-bit 65MS/s pipelined ADC is presented. At last, simulation results and conclusion are presented.

## 2. Modeling of Depletion-Mode MOSCAP Behavior

As mentioned earlier, depletion-mode MOSCAPs are inevitable in low-voltage applications. To reduce the highly nonlinear behavior of MOSCAPs in this region analog compensation techniques are regularly used. Fig. 2 shows two possible serial and parallel circuit diagrams of compensated depletion-mode MOSCAPs with two transistors. Comparing these two methods, while parallel compensated depletion-mode (PCDM) is more area efficient, it has less linearity than the serial compensated depletion-mode (SCDM) [3].

The Bias node of SCDM in Fig. 2 could whether be connected to the analog ground by a large resistance (that could be implemented by a transistor) or to a biasing voltage by a switch. In both cases, source and drain are connected to ground rather than to bulk. In addition to the benefits in its implementation, it widens the predictable range of the capacitance behavior by the models. Fig. 3 shows the

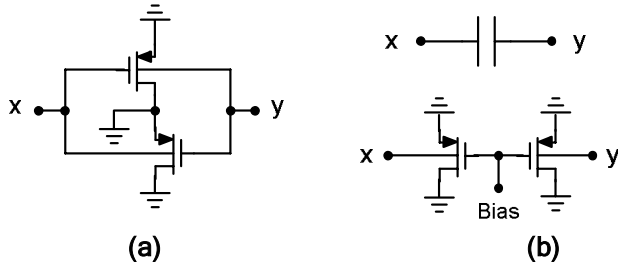


Fig. 2 Two possible approaches for the implementation of practical MOSFET capacitors:

- (a) Parallel compensated depletion-mode (PCDM) MOSCAP capacitor
- (b) Serial compensated depletion-mode (SCDM) MOSCAP capacitor

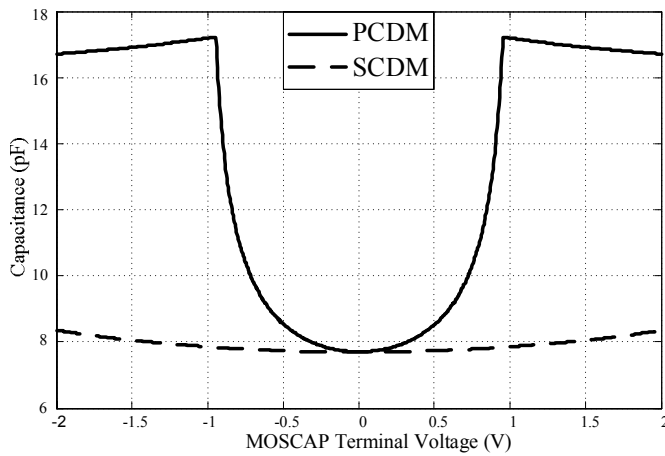


Fig. 3 Comparison between PCDM and SCDM C-V characteristics ( $W = 4.25$ ,  $L = 85\mu\text{m}$  for PCDM and  $W = 21.65$ ,  $L = 435\mu\text{m}$  and also bias = 0V for SCDM)

capacitance value as a function of voltage for both cases. For equal capacitance values in the origin, the size of PCDM is about five times smaller than SCDM. However the former has higher nonlinearity than the latter. Thus, more area efficiency can be obtained by employing PCDMs in analog domain but at the cost of a more accurate digital calibration algorithm. In this work unless otherwise mentioned, PCDMs are used.

As it will be shown later, for  $V_{REF}$  being the ADC reference voltage and  $2V_{REF} = 1.8\text{Vp-p}$  the fully-differential voltage swing, any capacitance behavior modeling in 1.5-bit residue stages for  $\pm V_{REF}/2 = \pm 0.45\text{V}$  is quite enough. Fig. 4 shows the PCDM C-V diagram in this range. As the capacitance value is an even function of its voltage, it can precisely be modeled by a Taylor expansion as:

$$C(V) = C_0 \left( 1 + m \left( \frac{V}{V_{REF}} \right)^2 + n \left( \frac{V}{V_{REF}} \right)^4 + \dots \right) \quad (1)$$

As there are infinite terms in this equation, higher than second order terms can be ignored to simplify its implementation:

$$C(V) = C_0 \left( 1 + m \left( \frac{V}{V_{REF}} \right)^2 \right) \quad (2)$$

where  $m$  depends on the type of compensation and also the technology and its value is approximately unchanged with capacitance value. This parameter can independently be obtained for each PCDM (SCDM) MOSCAP via simulations. Higher order term could also be taken into account for the depletion region model to become more accurate. For instance, fourth-order term is also included in the following model:

$$C(V) = C_0 \left( 1 + m \left( \frac{V}{V_{REF}} \right)^2 + n \left( \frac{V}{V_{REF}} \right)^4 \right) \quad (3)$$

These two models are compared with each other and simulation in Fig. 4 with  $V$  normalized to  $V_{REF}$ . To compare these two models in this figure, the best fitting model of (3) with simulation results is obtained with  $m = 0.28$  and  $n = 0.22$  and standard deviation of  $2.46\text{fF}$ . This model is measured to be

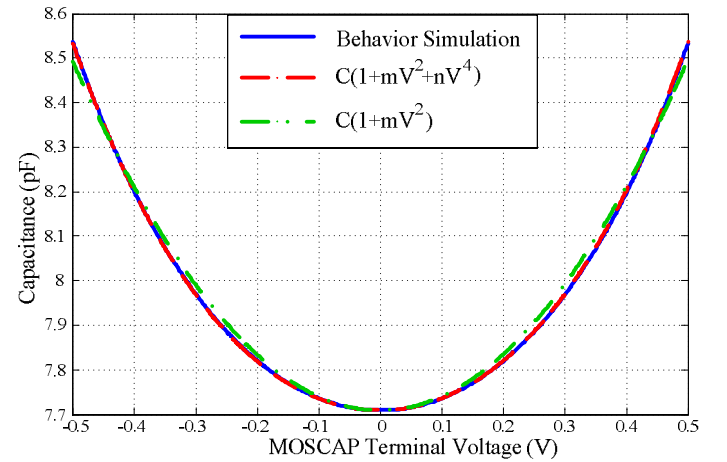


Fig. 4 Comparison between proposed models and simulation result in useful range for PCDM MOSCAP

approximately 6 times more accurate than the best fitting model of (2) obtained with  $m = 0.33$  and standard deviation of  $15.38\text{fF}$ . It is however at the cost of more complexity in the realization of model (3) due to the higher order terms in this equation.

### 3. Modeling of 1.5-bit MOSFET-Only Residue Stage Behavior

Fig. 5 shows the block diagram of a typical pipelined ADC with 1.5 bit/stage structure. It consists of multiple cascaded stages. In each stage (except the last stage which has only a 2-bit flash ADC), the input signal is first quantized by a sub-ADC, and then the output digital code is converted back to an analog signal by a sub-DAC. This quantized analog signal is then subtracted from the input signal, resulting in a residue that is amplified by two and then passed onto the next stage. The functions of sub-DAC conversion, subtraction, and amplification are commonly combined together and referred to as the multiplying digital-to-analog converter (MDAC). MDAC is often realized in switched-capacitor architecture. Assuming that the ADC is ideal and normalizing all voltages to  $V_{REF}$ , the analog output of each stage is given by:

$$V_O = (1 + \frac{C_S}{C_F})V_{in} - D\frac{C_S}{C_F} \quad (4)$$

where  $D$  is  $\pm 1$  or  $0$  depending on the input voltage level.  $C_S$  and  $C_F$  are the sampling and feedback capacitors respectively. A widely used switched-capacitor “capacitor-flip-over” MDAC to carry out (4) in transistor level is shown in Fig. 6. As it is seen, the common-mode voltage of the opamp is taken the same as the common-mode voltage of the input signal. This is necessary to limit the maximum voltage across each capacitor to  $V_{REF}/2$ . Using (2) and normalizing all voltages to  $V_{REF}$ , the nonlinear effect of replacing the sampling and feedback capacitors with MOSCAPs can be modeled by:

$$C_S = C_{S0}(1 + mV^2) \quad C_F = C_{F0}(1 + mV^2) \quad (5)$$

In the sampling phase (p1), as the capacitances values are dependant to the voltage across them, the total fully-differential charge stored on all  $C_{S0}$ s and all  $C_{F0}$ s is:

$$Q_S = \int_0^{V_{in}/2} C_{S0}(1 + mV^2)dV + \int_{-V_{in}/2}^0 C_{S0}(1 + mV^2)dV \quad (6)$$

$$+ \int_0^{V_{in}/2} C_{F0}(1 + mV^2)dV + \int_{-V_{in}/2}^0 C_{F0}(1 + mV^2)dV$$

Hence:

$$Q_S = 2 \int_0^{V_{in}/2} C_{S0}(1 + mV^2)dV \quad (7)$$

$$+ 2 \int_0^{V_{in}/2} C_{F0}(1 + mV^2)dV$$

and in the amplification phase (p2), feedback capacitors are connected to the output nodes and sampling ones are

connected to  $V_{CM} + D.V_{REF}/2$ . Hence the total charge stored on capacitors is:

$$Q_F = \int_{-V_O/2}^0 C_{F0}(1 + mV^2)dV + \int_0^{V_O/2} C_{F0}(1 + mV^2)dV \quad (8)$$

$$+ D.(\int_0^{0.5} C_{S0}(1 + mV^2)dV + \int_{-0.5}^0 C_{S0}(1 + mV^2)dV)$$

Thus:

$$Q_F = 2 \int_0^{V_O/2} C_{F0}(1 + mV^2)dV \quad (9)$$

$$+ 2D. \int_0^{0.5} C_{S0}(1 + mV^2)dV$$

As the total charge in both phases remains unchanged,  $Q_S$  and  $Q_F$  can be set equal to obtain the following expression:

$$V_O + \frac{1}{12}mV_O^3 = (1 + \frac{C_{S0}}{C_{F0}}).(V_{in} + \frac{1}{12}mV_{in}^3) \quad (10)$$

$$- D. \frac{C_{S0}}{C_{F0}}(1 + \frac{1}{3}m.(0.25))$$

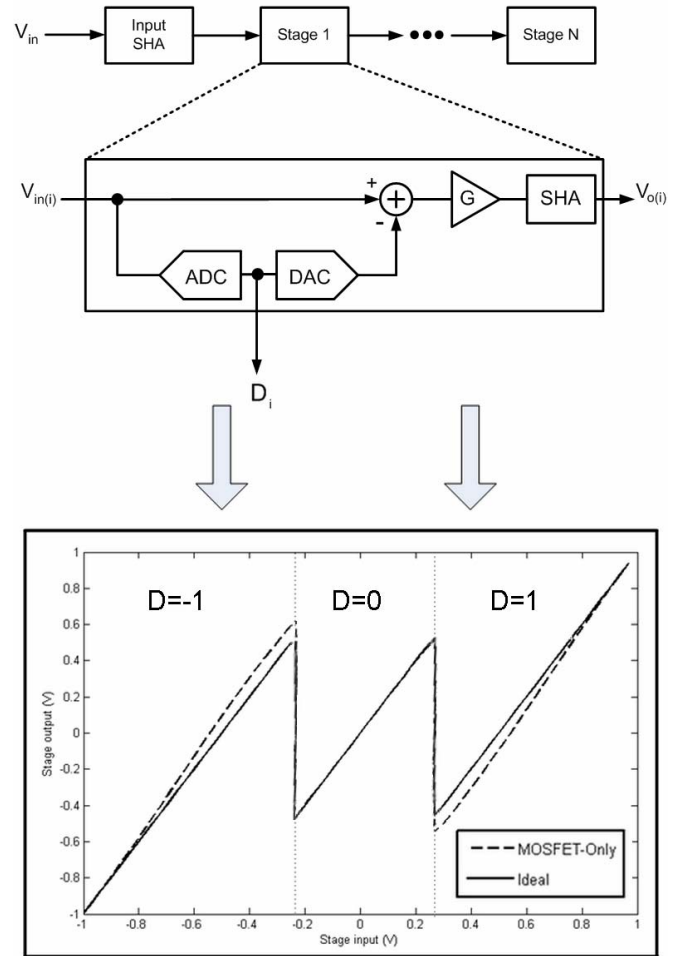


Fig. 5 1.5 bit/stage pipeline ADC and the transfer function of each stage

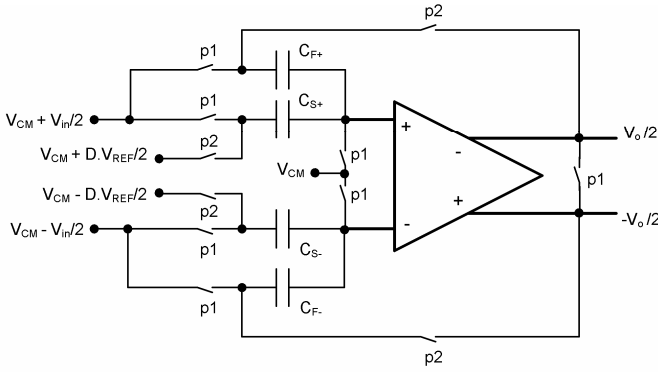


Fig. 6 A “capacitor flip-over” MDAC topology

As it is seen, this equation is a general form of (4) when the sampling and feedback capacitors are nonlinear ( $m \neq 0$ ). This equation could be simplified if the mismatch between MOSCAPs is assumed to be zero:

$$V_o + \frac{1}{12} m V_o^3 = 2 \cdot (V_{in} + \frac{1}{12} m V_{in}^3) - D \cdot (1 + \frac{1}{3} m \cdot (0.25)) \quad (11)$$

This expression has a closed-form solution for  $V_o$  or  $V_{in}$  that although rather complicated, it can be found.

As it was implied before, depletion-mode MOSCAP modeling with (3) can yield a more accurate result. By performing similar analysis with this model, the result is obtained to be:

$$V_o + \frac{1}{12} m V_o^3 + \frac{1}{80} n V_o^5 = 2 \cdot (V_{in} + \frac{1}{12} m V_{in}^3 + \frac{1}{80} n V_{in}^5) - D \cdot (1 + \frac{1}{3} m \cdot (0.25) + \frac{1}{5} n \cdot (0.0625)) \quad (12)$$

Unlike the previous case this expression does not have a closed-form solution. Hence, it should be solved numerically. Fig. 7 demonstrates the efficiency of these two models. It shows the SPICE simulation of a 1.5-bit residue stage with ideal capacitors replaced by PCDM MOSCAPs. The deviation between ideal and actual transfer functions demonstrates the need for a new modeling. Proposed models are also shown to prove their efficiency. For these models, all voltages are normalized to  $V_{REF} = 0.9V$  to be fitted with SPICE simulation. Equation (11) is plotted to represent (2) and (12) is numerically solved to represent (3). As it is seen, the result of (3) is more accurate than (2).

#### 4. Calibration Algorithm

Fig. 8 shows a possible implementation of a 12-bit MOSFET-only ADC. The first 6 stages receive the proposed calibration algorithm due to their nonlinear MOS capacitors. The nonlinearity caused by the remaining stages is assumed to be tolerable when it is referred to the ADC input because of being suppressed by the gain of the first six stages.

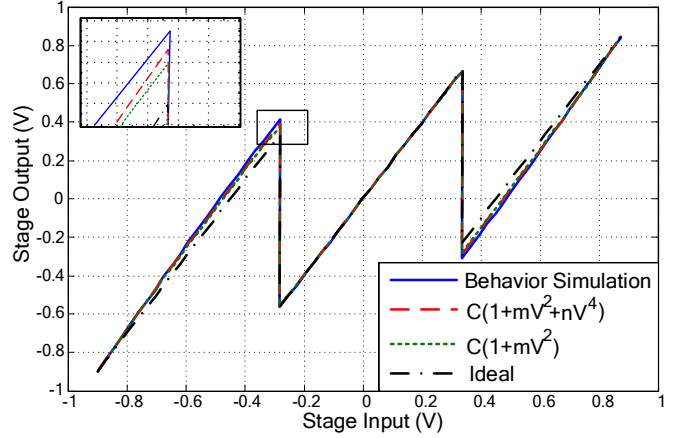


Fig. 7 Transfer function of a 1.5-bit MOSFET-only residue stage

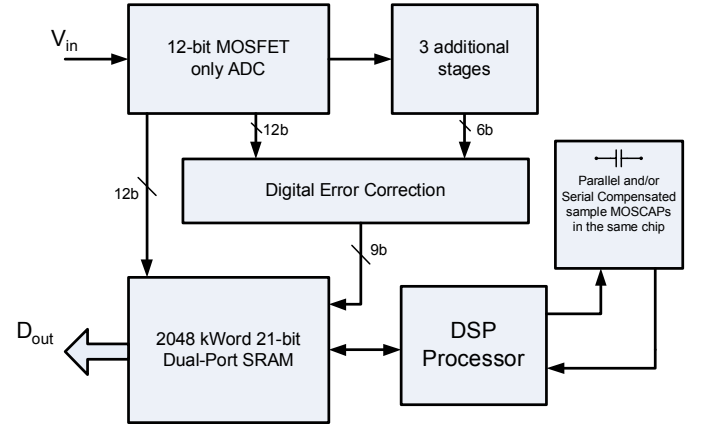


Fig. 8 Block diagram of ADC and calibration system

A dual-port RAM is used as a look-up table to store the corrected codes. During operation, it contains the mapping information between actual and corrected ADC output codes. This prevents the conversion rate of the ADC to be limited by the algorithm. The dual port RAM is directly addressed by the backend estimate and the decision bits of the first six stages. DSP processor should find the corrected codes to be filled in the RAM. Three additional stages are employed to reduce the quantization noise during calibration.

To obtain the backend estimate for the last stages (stages 7 to 12 and 13 to 15) the conventional approach to extract the digital output is used [4]-[5]:

$$V_{Backend} = \frac{1}{2} \sum_{i=7}^{15} \frac{D(i)}{2^{i-1}} \quad (13)$$

where  $D(i)$  is the  $i$ -th stage decision and the estimate is normalized to  $V_{REF} = 1V$ . To find each input in the first six stages, the estimated input of the  $i$ -th stage  $V(i)$  should be obtained from the estimated input of the  $(i+1)$ -th stage  $V(i+1)$  as:

$$V(i) = f(V(i+1), D(i)) \quad (14)$$

where  $f$  is the relation between  $V(i)$ ,  $V(i+1)$  and  $D(i)$ . DSP processor should estimate  $V(i)$  from  $V(i+1)$  and  $D(i)$  and store the corrected codes in RAM by the aid of a calibration equation. In this work, since a closed-form solution was available for (11), this relation was used for digital calibration of the first six stages.

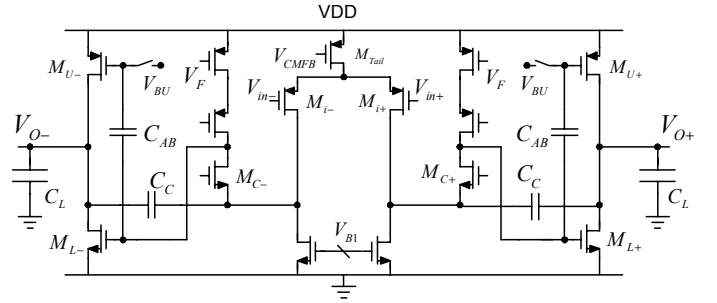
The link between DSP processor and sample parallel and serial MOSCAPs in the same chip can be manually provided by a converter so that the exact value of  $m$  in (2) could be found. However, this part could fairly be ignored if the processor is hardwired by an optimize value of  $m$  from simulation.

## 5. Simulation Results

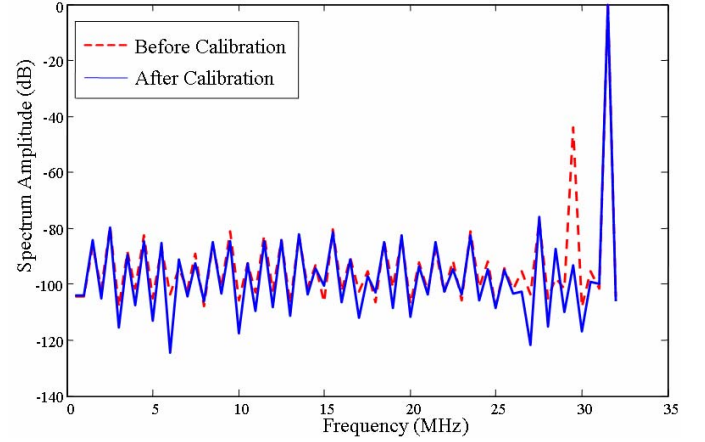
The calibration algorithm is applied to a 12-bit 65MS/s pipelined ADC shown systematically in Fig. 8. The digital calibration processor unit was implemented in MATLAB while the analog 1.5 bit residue stages were simulated by HSpice using 0.18 $\mu$ m BSIM3 models. As the input SHA opamp nonlinearities can directly degrade the performance, it was not employed in our simulated ADC. However the analysis in section III can be expanded to also compensate for the capacitor nonlinearities of this unit. The raw digital output codes were transferred to MATLAB where the calibration algorithm was realized. As it was implied earlier, the output of stage 7 onward was computed by (10) but each of the front-end six stages outputs were processed according to the algorithm. All 1.5-bit residue stages were identical similar to Fig. 6 with PCDM MOS sampling and feedback capacitors. The opamp uses a two-stage class AB cascode-compensated structure shown in Fig. 9 [6]-[7]. Class-AB capacitors were PCDM capacitors, but as compensation capacitors variations could directly change the opamp stability, SCDM structure with minor variations was used. Critical switches (input ones) were realized using bootstrap architecture [8], but all other switches were transmission gate type. At last, resistive divider comparators were used in every 1.5 bit residue stage [9]. Table 1 shows the ADC specifications for Nyquist rate input frequency before and after calibration. Fig. 10 shows the output spectrum before and after calibration. As it is seen the main spurious third-order harmonic is completely suppressed after calibration.

**Table. 1 Simulation Results**

|                           | Before calibration | After calibration |
|---------------------------|--------------------|-------------------|
| Resolution (bit)          |                    | 12                |
| Sampling Rate (MS/s)      |                    | 65                |
| $V_{DD}$ (V)              |                    | 1.8               |
| $m$ in Equation (11)      | 0                  | 0.33              |
| SNDR @ $f = 32$ MHz (dB)  | 43                 | 70                |
| SFDR @ $f = 32$ MHz (dB)  | 43                 | 78                |
| ENOB @ $f = 32$ MHz (bit) | 6.85               | 11.33             |



**Fig. 9 Operational amplifiers used in all 1.5-bit stages**



**Fig. 10 ADC output spectrum before and after calibration**

## 6. Conclusion

The design considerations of a 12-bit, 65MS/s pipelined ADC using compensated depletion-mode MOS capacitors, was presented in this paper. Digital calibration was used to compensate for the distortion caused by employing nonlinear MOSCAPs instead of linear MIMCAPs. Simulation results indicate that significant SNDR improvement can be achieved if the proposed digital calibration technique is used. Although the 1.5-bit architecture is chosen to demonstrate the operation of the technique it can generally be applied to other multi-bit architectures.

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