

# Flexibility-oriented Design Methodology for Reconfigurable $\Delta\Sigma$ Modulators

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## Abstract

*This paper presents a systematic methodology for producing reconfigurable  $\Delta\Sigma$  modulator topologies with optimized flexibility in meeting variable performance specifications. To increase their flexibility, topologies are optimized for performance attributes pertaining to ranges of values rather than being single values. Topologies are implemented on switched-capacitor reconfigurable mixed-signal architectures. As the number of configurable blocks is very small, it is extremely important that the topologies use as few blocks as possible. A case study illustrates the methodology for specifications from telecommunications area.*

## 1. Introduction

Reconfigurable systems aim to simultaneously offer the two main advantages of hardware and software: (i) similar to application-specific hardware, to provide high performance processing, and (ii) similar to software, to be flexible enough in tackling different applications. Reconfigurable systems are attractive implementation platforms for many embedded applications due to their capability of offering low development costs and short design times, while being accessible to less experienced designers.

While reconfigurable digital systems are very popular and well understood in terms of their capabilities and limitations, reconfigurable analog and mixed-signal (AMS) systems are - in contrast, much less studied or employed in practical applications. This prevents the more comprehensive harvesting of the possible benefits of reconfigurable systems, as the majority of embedded applications (e.g., embedded control and telecommunications) include significant amounts of analog signal processing. To tackle this major limitation, research must not only address new reconfigurable AMS architectural concepts, but also study the related design methodologies and EDA tools. More specifically, it is essential to develop efficient techniques for designing reconfigurable analog to digital converters (ADC) due to the importance of ADCs in embedded systems.

Several general-purpose reconfigurable AMS architectures are mentioned in the literature [3, 13]. Continuous-time and switched-capacitor reconfigurable ADCs have been presented in [4, 8, 12], but no design methodology or EDA tools were considered. More recently the PSoC reconfigurable mixed-signal array has been offered by Cypress Inc. [5, 15] as a cost-effective solution to embedded system implementation. While several ADCs have been implemented using PSoC [16], there is no design methodology and there are no EDA tools that would allow effortless and rapid design of new ADCs. Various techniques for single-mode (non-reconfigurable)  $\Delta\Sigma$  ADC design have been described in [2, 7, 11]. A systematic design flow for continuous-time reconfigurable  $\Delta\Sigma$  ADCs has been recently proposed in [14]. However, the produced modulator topologies are restricted to a set of predefined performance specifications (e.g., GSM, CDMA, and UMTS communication standards). The topologies have no flexibility in addressing new performance specifications. This is an important limitation because flexibility ought to be one of the main strengths of reconfigurable AMS architectures.

This paper proposes a systematic design methodology for creating flexible reconfigurable  $\Delta\Sigma$  modulator topologies implemented on switched-capacitor (SC) reconfigurable AMS architectures. The work considered an AMS architecture based closely on the PSoC reconfigurable architecture. As the amount of programmable analog blocks is very limited in PSoC, it is extremely important that the modulator topologies use as few blocks as possible. In contrast to the existing work, the proposed methodology generates a set of topologies that are optimized to meet performance attributes pertaining to ranges of values rather than being singular values. For example, the topologies are optimized for dynamic range (DR) requirements in the range  $[DR_{min}, DR_{max}]$ , and bandwidth (BW) constraints in the range  $[BW_{min}, BW_{max}]$ . The produced topologies can efficiently meet specifications  $SP \in [DR_{min}, DR_{max}] \times [BW_{min}, BW_{max}]$  while using minimum amount of hardware. In contrast, other design methodologies would produce a single topology corresponding to the most con-

strained specification  $\langle DR_{max}, BW_{max} \rangle$ . This topology is likely to be of higher order and with complex feedback and feed-forward structures [11]. The solution would obviously “waste” expensive programmable analog blocks for applications with less demanding requirements.

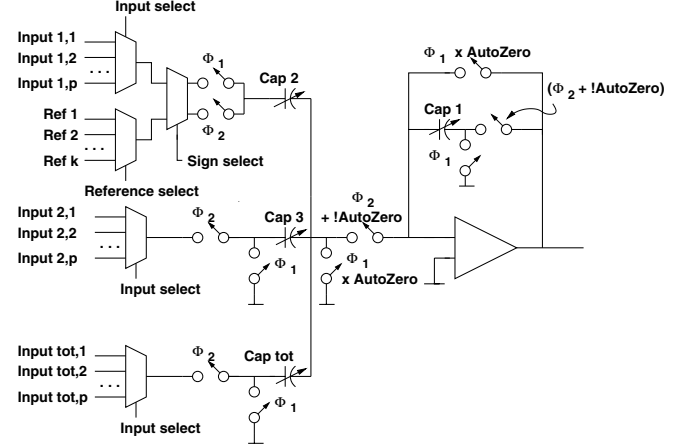
The design methodology considers first  $\Delta\Sigma$  modulator topologies of lower order, e.g., order one or two, and identifies the maximum performance ranges that can be met with these topologies. Then, it analyzes topologies of increasingly higher order, while maximizing the performance ranges that are not already covered by the architectures of lower order. This strategy avoids unnecessarily utilizing more hardware resources for specifications that can be also met by simpler modulators. A two step process finds the maximum specification ranges that are covered by the topologies of a certain order. First, for decreasing oversampling ratios (OSRs) (e.g.,  $OSR = 128, 64, 32, 16$ ), the signal and noise transfer functions of the modulators are computed using the Delta Sigma toolbox [10]. Then, the signal flow of the modulator topologies are computed by solving a set of mixed-integer nonlinear (MINLP) equations that are based on the computed transfer functions. The cost function minimizes the number of used programmable analog blocks and the power consumption of the topology. The MINLP procedure is a refinement of the method in [11]. As the MINLP equations assume ideal modulators, a post-optimization step fine-tunes the topology parameters while considering circuit nonidealities, such as jitter noise,  $kT/C$  noise, and the OpAmp white noise, finite DC gain, finite bandwidth, slew rate, and saturation [6]. The paper explains that the methodology is optimal, in the sense that it offers maximum covering of the performance ranges while minimizing the number of used programmable blocks.

The paper is organized as follows. Section 2 presents an overview of the reconfigurable AMS architecture. Section 3 discusses the proposed design methodology, and Section 4 describes a case study. Finally, conclusions are offered.

## 2. Reconfigurable Mixed-Signal Architecture

The reconfigurable AMS architecture that we considered is based significantly on the PSoC mixed-signal architecture of Cypress Inc. [5, 15]. Compared to the PSoC architecture, we simplified the structure of the reconfigurable analog cells, and increased the number of configurable input connections of a cell, so that  $\Delta\Sigma$  topologies with complex structures can be also implemented using the architecture. The section offers an overview of the AMS architecture.

The main part of the architecture is a bidimensional array of reconfigurable switched-capacitor blocks. The blocks are organized into  $m$  rows and  $n$  columns. Even though there is no theoretical limit for the number of rows and columns of an architecture, the number of rows and columns are ac-

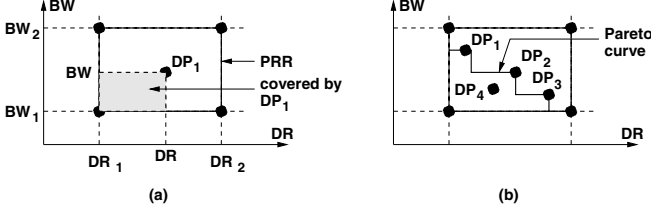


**Figure 1. Reconfigurable SC block based on the PSoC architecture [15]**

tually not very high due to the lower integration densities achievable for reconfigurable AMS circuits as compared to reconfigurable digital ICs. For example, the PSoC architecture includes at most three rows and four columns of configurable analog blocks [15]. This makes the programmable analog blocks a very valuable resource that should be used carefully in a design. Hence, minimizing the number of reconfigurable analog cells used for an implementation ought to be the main design requirement.

The reconfigurable analog blocks can be connected into various  $\Delta\Sigma$  topologies (netlists) through the programmable interconnect. The interconnect structure was designed, so that it offers versatile implementation of the feedback and feed-forward connections in a  $\Delta\Sigma$  ADC [9, 11]. The output of each block can be connected either to the longer *row* and *column interconnects*, to implement the global feed-forward or feedback structures, or to the shorter *local interconnect* between neighboring cells. In contrast, the PSoC architecture includes only column and local interconnects [15], which might be somewhat restrictive for implementing topologies with complex feed-forward and feedback structures. Such architectures might offer superior DR and lower sensitivity to circuit nonidealities than architectures with few feedback structures [11].

All configurable analog blocks are identical, and their internal structure is shown in Figure 1. The structure is similar to that of the type C configurable PSoC blocks [15], except of the following two differences: (i) we increased the number of programmable inputs connected to the summing node of the OpAmp, and (ii) eliminated the less used circuits, e.g., the comparator (available in each PSoC block), and the circuitry for producing interrupts. The first modification is needed for the implementation of complex high-order  $\Delta\Sigma$  modulators. The second change is justified by the fact that we are restricting the AMS architecture to implementation of  $\Delta\Sigma$  ADCs only rather than of a larger variety of circuits.



**Figure 2. Performance requirement region (PRR)**

Following are the main parts of a reconfigurable block.

The functionality of the SC blocks is programmed by configuring the topology of the network surrounding the OpAmp. Similar to the PSoC blocks, the programmable cell can be configured to operate as a comparator, a gain stage, or an integrator. If the capacitor array  $Cap_1$  is not connected then the circuit functions as a comparator, otherwise, the circuit is either a gain stage or an integrator.

In addition to the capacitor array  $Cap_1$ , each reconfigurable block has several other programmable capacitor arrays called  $Cap_2, Cap_3, \dots$  and  $Cap_{tot}$  in the figure. Array  $Cap_2$  is used for the input to the programmable cell. The rest of the capacitor arrays implement the ADC's feedback and feed-forward paths. The gain of the signal paths is set by programming the corresponding capacitor arrays. The value of  $tot$  is set by the maximum number of paths that can converge in a summing node. For ADCs of order up to five, the value of  $tot$  is six. The values of the capacitor arrays can be selected from the set  $\{0, \frac{1}{r}, \frac{2}{r}, \dots, 1\}$ .

Section 4 shows that  $r = 16$  is sufficient for realizing  $\Delta\Sigma$  ADCs of orders two and three, but  $r = 128$  is needed for fourth order ADCs. PSoC uses  $r = 32$  [15].

### 3 Reconfigurable $\Delta\Sigma$ ADC Design Method

This section presents the main parts of the proposed methodology for reconfigurable  $\Delta\Sigma$  modulator design: (1) the notation for expressing flexible performance requirements, (2) the technique for finding optimized modulator topologies, and (3) the overall methodology.

#### 3.1 Description of flexible performance requirements

Before presenting the proposed design methodology and the related design steps, we discussed the notation used for specifying the flexible performance requirements of reconfigurable  $\Delta\Sigma$  ADCs. This is important to identify the set of actual (punctual) performance requirements used in the design process. For example, typical embedded control applications might require ADCs with a variable conversion accuracy (e.g., going from 6 bits to 12 bits), an adjustable peak SNR ( $SNR_{max}$ ) (such as in the range 45dB to 90dB), and capable of converting signals in a bandwidth ranging from 50 KHz to 1 MHz.

Please note that implementing only one  $\Delta\Sigma$  modulator corresponding to the most constrained scenario is not a very efficient solution. The topology is likely to be of high order, with complex feedback and feed-forward structures, and requiring many reconfigurable analog blocks for its implementation. As explained in Section 2, the reconfigurable analog blocks are very valuable resources, and should be utilized with care. Utilizing less resources for simpler ADCs allows implementing more functionality on the reconfigurable AMS architecture. Also, the power consumption of complex modulators is higher, which leads to unnecessary waste of energy for less demanding applications. Third, high-order  $\Delta\Sigma$  ADCs tend to be unstable [9], which limits the range of the input signals that are converted. This justifies that it is more effective to design a set of  $\Delta\Sigma$  topologies (which are reconfigured for different specifications) than design the worst case topology only.

The variable (flexible) performance requirements are expressed as closed ranges  $[P_{min}, P_{max}]$ . For example, the variable DR is defined as the range [50 dB, 90 dB], the adjustable peak  $SNR_{max}$  as the range [50 dB, 90 dB], and the bandwidth as the range [50 KHz, 2 MHz]. Figure 2(a) shows the resulting *performance requirements region* (PRR) - if only two requirements are considered, bandwidth and DR. The concept can be easily extended for more metrics, like  $SNR_{max}$ , linearity, and power consumption.

**Definition:** Let's assume that the design point  $DP_k$  is characterized by the bandwidth  $BW_k$  and the dynamic range  $DR_k$ . We say that the point  $DP_k$  covers the rectangular PRR formed by the points  $\langle bw, DR \rangle$ , where  $bw < BW_k$  and  $DR < DR_k$ , as all possible requirements  $bw - DR$  are satisfied by the design point  $DP_k$ . The *hardware cost* of a point  $DP_k$  is equal to the number of reconfigurable SC blocks used to implement the point.

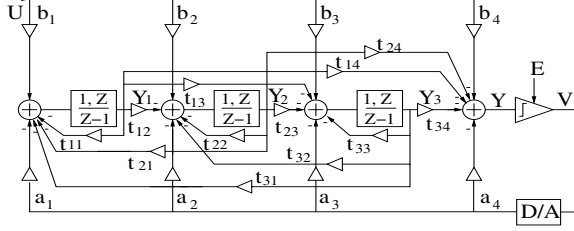
Figure 2(a) shows the PRR covered by the point  $DP_1$ .

**Definition:** A design point  $DP_k$  is called *basic* design point if its covered PRR is not contained in the PRR of another design point or the union of the PRRs of a set of points with lower or equal hardware cost as the point  $DP_k$ .

The set of basic design points with the same hardware cost define the Pareto curve for that hardware cost. For example, Figure 2(b) shows the Pareto curve defined by the set  $\{DP_1, DP_2, DP_3\}$  of basic points. Point  $DP_4$  is not basic, unless its hardware cost is lower than that of point  $DP_2$ .

**Problem statement:** The reconfigurable  $\Delta\Sigma$  modulator design problem can be formulated as that of finding for *successively increasing hardware costs*, (i) the sets  $SBDP_i$  of basic design points, and (ii) the corresponding  $\Delta\Sigma$  modulator topologies, such that each set  $SBDP_i$  covers a maximal PRR that is not also covered by the  $SBDP$  sets of smaller hardware cost.

Please note that the problem statement does not require us to find the sets  $SBDP_i$  of minimum cardinality, thus we



**Figure 3. Generic 3<sup>rd</sup> order  $\Delta\Sigma$  topology**

do not have to find the minimum number of basic design points that cover a PRR. The reason is that the configuration data required for implementing a modulator is minimal. It is equal to the number of control registers that have to be programmed, and is several bytes per topology.

### 3.2 Optimal $\Delta\Sigma$ ADC topology design

This subsection summarizes the method for synthesizing the optimal modulator topology for a given specification. The method is a refinement of the technique presented in [11]. The main parts of the method are (A) the generic topology, (B) the synthesis procedure based on MINLP, and (C) the cost function for topology synthesis.

**A. Generic  $\Delta\Sigma$  modulator topology.** The crux of the ADC topology synthesis method is a generic representation that describes all the possible topologies for single-bit single-loop  $\Delta\Sigma$  modulators. Figure 3 shows the representation for 3<sup>rd</sup> order  $\Delta\Sigma$  modulators, but similar representations exist for higher order modulators also. The generic representation includes all possible feedback and feed-forward signal paths.  $Y_i$  represents the output of the  $i^{th}$  integrator, and  $Y$  is the input to the quantizer.  $A_i$  stand for the feedback coefficients from the output to the  $i^{th}$  adder,  $b_i$  are the feed-forward coefficients from the input to the  $i^{th}$  adder, and  $t_{ji}$  are the coefficients from  $Y_j$  to the  $i^{th}$  adder in the modulator. There are negative signs for all  $t_{ji}$  and  $a_i$  coefficients.

Let  $N$  be the modulator order. Then, following expressions hold as a general rule:

$$t_{ji} \geq 0, \text{ if } j \geq i, j = 1, \dots, N, i = 1, \dots, N+1 \quad (1)$$

$$t_{ji} \leq 0, \text{ if } j < i, j = 1, \dots, N, i = 1, \dots, N+1 \quad (2)$$

$$a_i \geq 0, b_i \geq 0, i = 1, \dots, N+1 \quad (3)$$

There are  $(N+1) \times (N+2)$  coefficients in the generic topology. It can be seen that many of the “classic” topologies [9] can be derived from the generic topology by removing some of the signal paths. Note also that the integrators could be either delayed or delayless. For the generic topology of order  $N$ , we derived its noise transfer function (NTF) and signal transfer function (STF) in terms of the coefficients of all signal paths. We assumed that the quantization noise  $E$  is additive white-noise[9].

**B. Optimal topology generation using MINLP.** By equating the symbolic TFs to the desired TFs (desired STF

is assumed to be 1),  $3 \times (N+1)$  equations are obtained. Obviously, there are an infinite number of solutions considering that the number of unknowns -  $(N+1) \times (N+2)$ , is always larger than the number of equations -  $3 \times (N+1)$ . Also, in order to select any signal path in the generic topology, a corresponding binary 0/1 variable was defined to denote whether the signal path is present or not.

For a given a cost function  $f$ , the topology synthesis problem can be formulated as:

$$\begin{aligned} & \text{minimize cost } f(x_i, wx_i); \\ & \text{subject to : } g(x_i) = 0; \\ & \text{subject to : } h(x_i, wx_i) \leq 0; \\ & \text{subject to : } x_i \text{ satisfy (1), } wx_i \in \{0, 1\}; \end{aligned}$$

where  $x_i$  denotes any of the unknown coefficients  $a_i, b_i$  and  $t_{ji}$  defined in (1),  $g$  are the  $3 \times (N+1)$  equality constraints obtained from equating the symbolic NTF and STF to the desired NTF and STF, and  $h$  are the inequality constraints relating the coefficient variables to the binary variables, so that  $wx_i$  correctly identify whether the signal path with coefficient  $x_i$  is present or not.

The resulting problem can be optimally solved using mixed-integer nonlinear programming (MINLP) [1]. Thus, MINLP solving offers the best topology with respect to the cost function  $f$ . MINLP formulation is scalable, and it is easy to add additional constraints.

**C. Cost function formulation.** The cost function used in topology synthesis includes the following two terms: (1) one term for minimizing the hardware cost of a  $\Delta\Sigma$  modulator, and (2) one for minimizing its power consumption.

Since binary variables denote whether the corresponding signal paths are present or not, the hardware cost minimization was formulated as:

$$\text{Minimize } \sum_{i=1}^{(N+1)(N+2)} wx_i$$

Power consumption estimation was similar to [7].

### 3.3 Overall design flow

The overall design flow is presented in Figure 4. The first step finds the minimum-order  $\Delta\Sigma$  modulator topology with the least number of feedback and feed-forward paths. The topology is synthesized for the least demanding performance requirements of the PRR, the minimum bandwidth  $BW_{min}$  and the minimum dynamic range  $DR_{min}$ . The oversampling ratio is fixed to the maximum value  $OSR_{max}$ . Using the generic topology for that order, the optimal modulator topology is found for the requirements  $< bw_{min}, DR_{min} >$  by solving the MINLP equations.

The found topology is post-optimized using a simulated annealing (SA) algorithm that attempts to improve the DR of the modulator by performing localized changes of the topology coefficients. The signal flow of the topology remains unchanged during post-optimization. The performance of each solution analyzed by SA is estimated through MATLAB simulation of the behavioral models for SC  $\Delta\Sigma$  modulators, similar to the technique by Malcovati *et al.* [6].

- (1) for modulator orders  $N = 1, 2, 3, \dots$  do
- (2) for decreasing OSR values do
- (3) find the optimal modulator topology by solving the related MINLP equations for the given order  $N$  and OSR;
- (4) post-optimize the topology using SA guided by MATLAB simulation of the modulator behavioral models;
- (5) identify the stair-case Pareto curve and mark the PRR covered by the modulators of order  $N$ ;

**Figure 4. Overall design methodology**

Lets assume that the resulting design point  $DP_1$  is characterized by the performance attributes  $bw_1$  and  $DR_1$ . The point  $DP_1$  is the first basic point DP found by the method.

The next step finds more basic design points with the same hardware cost as the point  $DP_1$ . Therefore, the order of the modulator is kept the same as that of the point  $DP_1$ , but the OSR is modified. Lower OSRs are considered now. For example, if the modulator for  $DP_1$  uses  $OSR = 128$  then the methodology will consider  $OSR = 64$ , then  $OSR = 32$ , and so on. Repeating the steps that produced the topology for  $DP_1$ , the topologies for the successively decreasing OSR values are synthesized. Lets denote these design points as  $DP_2, DP_3, \dots$ , where the point  $DP_i$  corresponds to a larger OSR value than the point  $DP_{i+1}$ . This means that the topology for the point  $DP_i$  offers a higher DR, but converts signals of lower bandwidth.

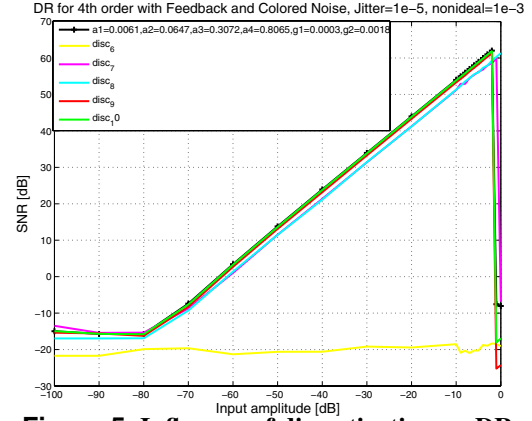
It is obvious that each of the design points  $DP_1, DP_2, DP_3, \dots$  are basic design points as they correspond to different bandwidth - DR trade-offs. It is impossible that the PRR covered by point  $DP_i$  is entirely included in the PRR of another point because all points have the same order, and are optimal for the specification they were synthesized for.

Also, the set of design points produces a maximal covering of the PRR as each of the points was synthesized for a maximum DR. For the given set of OSR values, it is impossible to generate topologies with higher DR than those produced through MINLP [11]. This is because the MINLP solving produces mathematically optimal topologies.

The methodology continues by considering  $\Delta\Sigma$  modulators of order higher by one. This corresponds to increasing the hardware cost of the design points by one SC block. Then, similar to the previous step, the OSR is set to the maximum value, and the optimal modulator topology is synthesized. More design points are produced for successively decreasing OSR values, similar to the previous case. This generates a new Pareto curve.

## 4 Case Study

The goal was to design reconfigurable  $\Delta\Sigma$  modulators that would cover the PRR defined by the bandwidth range



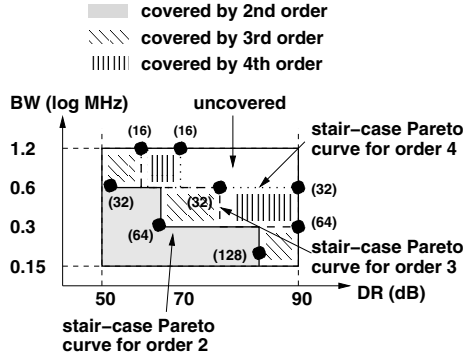
**Figure 5. Influence of discretization on DR**

$BW = [150\text{kHz}, 1.2\text{MHz}]$  and the DR range  $DR = [50\text{dB}, 90\text{dB}]$ . The PRR corresponds to typical communication standards, e.g., UMTS standard has  $BW = 1.2\text{ MHz}$  and  $DR = 70\text{ dB}$  requirements, CDMA2000 standard has  $BW = 615\text{ KHz}$  and  $DR = 80\text{ dB}$  requirements, etc. [12]. In addition, the topologies should cover the targeted PRR using the minimum number of reconfigurable SC blocks.

**A. Finding the discretization value for the SC block capacitor arrays.** Before synthesizing the reconfigurable topologies, a set of experiments was set-up for finding the discretization value  $r$  for the capacitor arrays. A capacitor array can implement the values  $\{0, \frac{1}{r}, \frac{2}{r}, \dots, 1\}$ . This experiment is important because the value  $r$  determines the precision of implementing the topology coefficients on the reconfigurable SC blocks. The larger the value of  $r$  the more precise the coefficient values can be implemented, but this increases the hardware overhead needed for programming the capacitor arrays.

A large number of topologies from the literature [9, 11] was analyzed, and simulated for different nonidealities [6]. For the fourth order modulator topology in [11], Figure 5 shows the resulting DR values for different discretizations  $r = 2^i, i = 6 - 10$ . For the value  $r = 64$  (and all lesser values), the topology did not operate as a  $\Delta\Sigma$  modulator. However, for values  $r$  larger than 7, the resulting DR was close enough to the ideal case. In general, for fourth order topologies, a discretization value of  $r = 7$  is needed for achieving good DR performance. For second and third order modulators a value  $r = 16$  provides a sufficiently good accuracy for implementing the modulator coefficients.

**B. Synthesizing flexible topologies.** The methodology was used to find the topologies that cover the defined PRR using a minimum amount of configurable SC blocks. First, a set of second order modulators was produced using the MINLP based topology synthesis procedure. Due to space limitations, the topologies are not shown in the paper. Topologies were generated for the OSR values 128, 64, 32, and 16. Figure 6 presents the stair-case Pareto curve that re-



**Figure 6. Pareto curves for different orders**

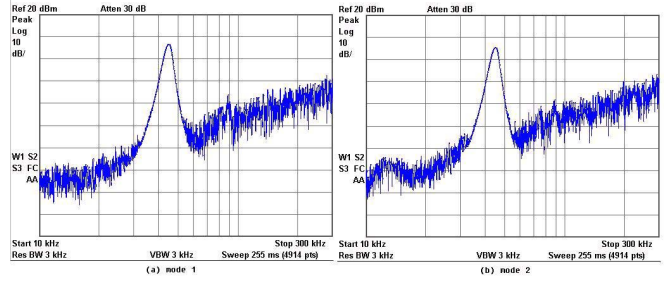
sulted for the second order topologies, and the PRR covered by these. The bullets correspond to basic design points. The corresponding OSR was shown in brackets. The architecture for OSR = 16 did not cover any portion of the PRR, as its DR = 47 is below the lower limit of the PRR. The topology was eliminated from the set. All second order topologies use two configurable SC blocks for implementation. Then, the modulator order was increased to three and then to four. Two new stair-case Pareto curves were produced as shown in Figure 6. All third order modulators require three SC blocks, and all fourth order modulators use four blocks. One third order and two fourth order topologies were also eliminated from the set because their covered PRRs were already covered by lower cost topologies.

The remaining 8 topologies offer a large covering of the PRR. The uncovered region corresponds to very demanding specifications that cannot be met by modulators of order lesser than 5 and with OSR up to 128. Please note that only a small fraction (14.5%) of the PRR requires modulators of fourth order. Assuming a uniform probability for having all specifications in the PRR, the proposed methodology saves in 17% of the cases one SC blocks, and in about 40% of the cases two SC block as compared to the straightforward solution (that implements one fourth order modulator for the worst case). Considering that all blocks have similar power consumption, this also results in power consumption going down by about 50% in 40% of the cases, and by 25% in 17% of the situations.

Figure 7 present the power spectrum density measured for two second order  $\Delta\Sigma$  modulator topologies implemented on the PSoC chip. The measurements are in good accordance with the simulation results.

## 5 Conclusion

This paper presents a systematic methodology for producing reconfigurable  $\Delta\Sigma$  modulator topologies with optimized flexibility. To increase their flexibility, topologies are optimized to meet performance attributes pertaining to ranges of values rather than singular values. As the amount of configurable SC blocks available in AMS architectures



**Figure 7. Measured power spectrum density**

is very limited, the methodology minimizes the number of SC blocks required by a topology.

The methodology is optimal, in the sense that it offers maximum covering of the performance ranges while minimizing the number of used programmable blocks. A case study addressing specifications for telecommunications shows that compared to traditional designs, the produced topologies use fewer configurable SC blocks, and might lower power consumption by 25%-50%.

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