System Level Power Optimization of Sigma-Delta Modulator

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Abstract

A new approach to power optimization of the sigma delta modulators was presented based on the modeling of noise performance while deciding its system functions and the sub-circuit specifications. And a system model of a 2nd order modulator with a Matlab algorithm to optimize its power specifications was developed. The system simulation results showed that all specifications were consistent with the expectations well. By using the proposed architecture, a resolution of 16-bit was achieved.

1. Introduction

In recent years, as the rapid development of modern communication systems and devices such as cellular phones, audio equipments and other PDA products, performance improvement of the signal processing system attracted more and more attentions since it is essential to their audio and image qualities. Thus, sigma-delta converters were widely adopted due to their superiority in non-ideality processing as well as a unique technology of noise modulation, both of which are of key importance to high precision and signal-to-noise ratio (SNR) of data converters.

However, since the using of over-sampling technology in sigma-delta converters, they usually consume more power than normal nyquist rate ones. As the total power consumption was reduced by advanced digital technology, the micro-power consumption and low voltage low power become the focuses of researchers while designing the analog module (sigma-delta modulators) in such a converter, especially in some applications like medical measurement. Unfortunately, the improvements are limited by the fact that most optimizations of the sigma-delta modulator are based on the advanced technology or some minor amelioration of the operational amplifiers. [1][2]

In this paper, a new optimization approach was proposed based on the noise performance analysis and the modeling of the non-ideality factors of sigma-delta modulators in the perspectives of the system design as well as the tradeoffs between power and resolution.

2. System architecture

In order to reduce power consumption, simple system architecture is preferred through minimizing the circuit area and parasitic capacitance. In the consideration of integrator saturation, a feed forward structure is always used in the system architecture.

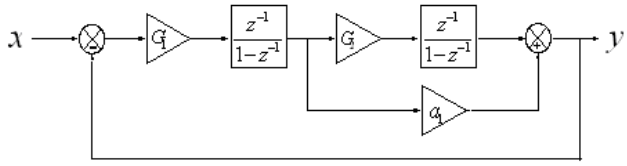

Figure 1. System architecture of the second order single loop feed forward modulator

Figure 1 shows the architecture of a second order single loop feed forward sigma-delta modulator. Here, the block z-1/1-z-1 represents the integrator block with a period's delay. The noise transfer function of the modulator can be described as equation (1), in which G1 and G2 are the gains of the integrators and a1 is the feed forward coefficient of the modulator. Those variables should be carefully chosen in order to avoid stability problems.

$$NTF = \frac{1}{1+\frac{G_1 z^{-1}}{1-z^{-1}} \bullet \left(\frac{G_2 z^{-1}}{1-z^{-1}} + a_1\right)} = \frac{\left(1-z^{-1}\right)^2}{(1+G_1G_2-G_1a_1)(1-z^{-1})^2+(G_1a_1-2G_1G_2)(1-z^{-1})+G_1G_2} \quad (1)$$

In the actual design, the NTF is designed first with a Pole-Zero optimization. Once the aiming NTF is fixed, it can be easy to get the optimized values of the variables from

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the noise transfer equations. For example, (0.75, 0.25, 1) can be one solution of (G1, G2, a1) of the modulation which realizes the objective NTF given in equation (2).

$$NTF = \frac{(z-1)^2}{z^2 - 1.225z + 0.4415} \tag{2}$$

However, the method mentioned before uses the ideal models of the modulator, which considers only the quantization error. In reality, there are many other factors, which might lead to a worse SNR ratio. Those factors make it knotty to design the masked blocks in the modulator and end up in the redundancy in the demanding of performance, which lowers the system's power efficiency. To minimize the specifications demands of the circuits, a practical way includes the modeling of these non-ideality factors and forming a reality transfer function.

3. Non-ideality modeling

The non-ideality factors of a sigma-delta modulator can be different, including the external noise accompanying with the input signal, the thermal noise, the clock jitter as well as the non-ideal operation of the integrator.

In the following part, a new approach of power optimization will be discussed by modeling of these non-ideality factors in SC sigma-delta modulators except the source noise, which is caused by factors out of the system.

3.1. Effect of jitter

The term jitter refers to the uncertainty of the time characteristics of a pulse, which are caused by the intrinsic noises generated by the pulse generating circuit[4]. In the consideration of the switch-capacitors (SC) sigma-delta modulators, the effects of the jitter are a main problem in the sampling stage when the signal is not sampled at the moment nTs but at nTs+Δt. We assume that the jitter Δt to be a Gaussian random process with its mean=0 and standard deviation $\sigma = |\Delta T|_{\max}/3$. Then the sampling error considering the clock jitter can be modeled as the equation (3) and (4).

$$e_1(n) = x\left(nT_s + \Delta t\right) - x\left(nT_s\right) = \sigma \times \frac{dx}{dt}(nT_s) \tag{3}$$

$$P_{e1} = E\left\{e_1^2\right\} = \frac{M^2}{2}\left(2\pi f_B\right)^2 \sigma^2 \tag{4}$$

3.2. The thermal noise

In the SC networks, the thermal noise is mainly displayed as the kind of switched capacitor KT/C noise, or the sampled thermal noise. Because the KT/C noise is introduced along with the signal at the most beginning, it might be the second most serious noise after the quantization noise and must be taken into consideration. Since the KT/C noise is random in nature, we describe the noise as in the equation (5) and (6), in which $\alpha(t)$ can also be modeled as a Gaussian random process with in the range between –1 and 1.

$$e_2(n) = \sum_C \alpha(t) \times \sqrt{\frac{KT}{C}} \tag{5}$$

$$P_{e1} = E\left\{e_2^2\right\} = \sum_c \frac{KT}{C} \tag{6}$$

Because the KT/C noises are generated from the SC function, every SC operation stage will lead to a unit of KT/C noise in the circuit. For example, in the integrator shown in Figure 2, four units of KT/C noises will be introduced because the fully-differential structure and the use of separate sampling and holding stages.

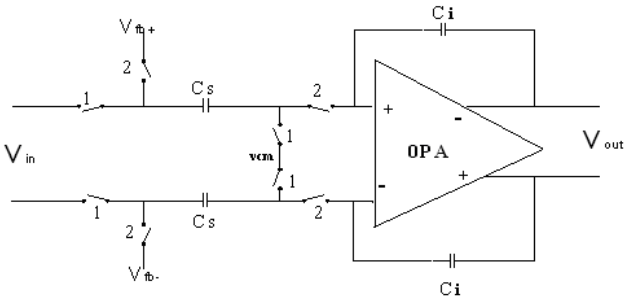

Figure 2. Switched capacitor integrator using the fully differential operational amplifier

3.3. Effect of finite gain

In an ideal integrator with infinite gain amplifier, the transfer function of an integrator can be written as equation (7), in which the ratio Cs/CI reflects the integrator gain.

$$H(z) = \frac{C_S}{C_I} \bullet \frac{1}{z-1} = \frac{C_S}{C_I} \bullet \frac{z^{-1}}{1-z^{-1}} \tag{7}$$

However, the equation (7) is only a abstract model because the gain is not infinite in actual, when considering the finite gain of the amplifier, the transfer function must be rewritten as equation (8).

$$H(z) = \left(\frac{C_S}{C_I} \bullet \frac{z^{-1}}{1-z^{-1}}\right) \bullet \frac{1}{1 - \frac{1}{A} - \frac{C_S}{A \bullet C_I(1-z^{-1})}} \tag{8}$$

From the above equation, it can be seen that the finite gain of the amplifier introduces magnitude and phase errors separately as equation (9)-(10).

$$e_m(jw) = \frac{1}{A} \bullet \left(1 + \frac{C_S}{2C_I}\right) \tag{9}$$

$$e_p(jw) = \frac{C_S}{C_I} \bullet \frac{1}{2A \bullet \tan\left(\frac{wT_s}{2}\right)} \quad (10)$$

3.4. The slew rate and finite gain bandwidth

In the integrator block, the slew rate and the finite gain bandwidth determine the signal's settling process. Supposing the initial voltage is 0, equation (11) models the limit of the amplifier's bandwidth in the settling process of the signal when $\left|\frac{d(G_i V_{in})}{dt}\right| \leq SR$, in which Vout and Vin are separately the output and input of the amplifier;$\tau$is the time constant of the integrator, whose value is related to the bandwidth (GBW) of the integrator as the equation (12) shows; Gi is the gain of the integrator.

$$V_{out}(t) = G_i V_{in} \bullet \left(1 - e^{-\frac{t}{\tau}}\right) \quad (11)$$

$$\tau = \frac{1 + G_i}{2\pi \bullet GBW} \quad (12)$$

If taking the influence of slew rate into consideration, especially when $\left|\frac{d(G_i V_{in})}{dt}\right|$ >SR, the settling process of the output signal should be described as equations (13). In this equation, t_0 is the slewing time of the integrator, the value of which is determined by equation (14) in consideration of the voltage continuity.

$$V_{out}(t) = \begin{cases} SR \times t & t < t_0 \\ V_{out}(t_0)e^{-\frac{t-t_0}{\tau}} + G_i V_{in}(1 - e^{-\frac{t-t_0}{\tau}}) & t > t_0 \\ G_i V_{in} & t \to \infty \end{cases} \quad (13)$$

$$t_0 = \frac{V_{ideal}}{SR} - \tau \quad (14)$$

In the actual design, it is necessary to make $\frac{\Delta v_{o\max}}{SR} < \frac{T_s}{2}$ to minimize the effect of finite slew rate. Then only the effect of finite bandwidth need to be molded, and the transfer function can be reformulated into the following equation.

$$H(z) = \frac{C_S}{C_I} \bullet \frac{z^{-1}}{1 - z^{-1}} \bullet \left[1 - e^{-\frac{T_s}{2\tau}} \bullet \frac{C_S}{C_S + C_I}\right] \quad (15)$$

After considering those above non-ideality factors, the sigma-delta modulator can be remolded as in Figure 3.

4. Optimizations

Note that in Figure 3, the non-ideality of the second integrator, the quantization error as well as the noise e21 and e22 are subject to second-order shaping and decreased by the gain of the first amplifier, the power spectral densities of

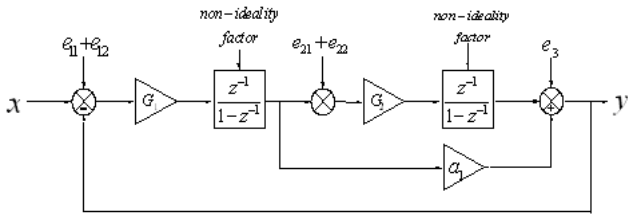

Figure 3. Practical architecture of the second order single loop feed forward modulator

those noises are usually much lower than that of the quantization error and can be neglected in order to simplify the transfer function. After this simplification and treating the quantization error as the white noise, we can reach at the z-domain transfer function considering the non-ideality of the first integrator as equation (16), in which the parameter NTF'can be calculated as in equation (17), G1' represents the non-ideality affects of the first integrator. Supposing M the magnitude of the input signal, the SNR of the 2nd order sigma-delta modulator can be reached as in equation (19).

$$Y(z) = X(z) + E_{11}(z) + E_{12}(z))(1 - NTF') + E_3(z)NTF' \quad (16)$$

$$NTF' = \frac{\left(1 - z^{-1}\right)^2}{(1 + G_1'G_2 - G_1'a_1)(1 - z^{-1})^2 + (G_1'a_1 - 2G_1'G_2)(1 - z^{-1}) + G_1'G_2} \quad (17)$$

$$G_1' = \frac{G_1}{1 - \frac{1}{A} - \frac{G_1}{A \bullet (1 - z^{-1})}} \bullet \left[1 - e^{-\frac{T_s}{2\tau}} \bullet \frac{G_1}{1 + G_1}\right] \quad (18)$$

$$SNR = \frac{\frac{M^2}{2}}{\frac{M^2}{4}\frac{\pi^2}{OSR^3}\frac{\sigma^2}{T_s^2} + \frac{KT}{2OSR \bullet C_s} + \int_0^{fs/2OSR} \left(\frac{\Delta}{2}\right)^2 \left(\frac{NTF}{STF}\left(e^{j2\pi f/fs}\right)\right)^2 df} \quad (19)$$

As discussed above, G1, G2 and a1 can be replaced by 0.75, 0.25, and 1. Assuming M=1 can simplify the above equations and make the final SNR after the filter process be related only to the variables mentioned above as in the equation (20). Once the OSR is determined, all of the other variables can be optimized to minimize the power because they are considered approximately proportional to power consumption.

$$SNR = \frac{10^8}{3.9478 \bullet \left(\frac{\sigma}{T_S}\right)^2 + \frac{8.2800 \times 10^{-16}}{Cs} + \frac{27.903 - 0.34817A + 1.1581 \times 10^{-3}A}{\left(1 - \frac{3}{7}e^{1.7943 \times 10^{-6} \bullet GBW}\right)A^2}} \quad (20)$$

In order to meet the SNR requirement and minimize the power at the same time, the specifications of the amplifiers should be properly designed. In other words, an optimized solution satisfies equation (21) should be fixed. The equation is described in the Matlab algorithm of optimization and the product of GBW and A indicates the power of the amplifier, Cs and $1/\sigma$ the power needed separately in the

sampling capacitors and the clock generators.

$$\begin{aligned} &min(GBW \bullet A + Cs + 1/\sigma) \\ &\quad sub \quad to \quad SNR\,(GBW, A, Cs, \sigma) \geq SNR_0 \end{aligned} \tag{21}$$

When using the function 'fmincon' in the optimization toolbox of Matlab with an initial values, the optimized specifications can be arrived. Table 1 shows the optimized solutions compared with the initial ones.

Table 1. Specifications of the sub-circuits before and after optimization

Specifications	σ/T_S	GBW	Cs	A
Before optimization	0.01	10^6	1pF	700
After optimization	0.08	600K	25fF	600

The analyzed system is the one mentioned before and a SNR requirement is about 16bit (100dB). Figure 4 and Figure 5 shows the simulated PSD before and after the optimization separately. From these figures, it can be seen that both systems achieve the desired SNR, but the optimized one can achieve the same demands at less demanding specifications and thus consumes less power.

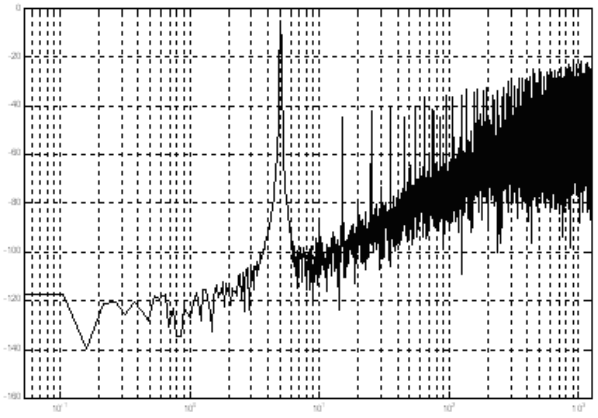

Figure 4. Simulated PSD before optimization

5. Conclusions

In this paper, a new approach subsisted by the optimization tools in Matlab to optimize sigma-delta modulator for low power consideration was proposed and analyzed. The methods were inclined to make the specifications of the sub circuit less demanding when an initial solution was proposed, based on the analysis of noise modeling

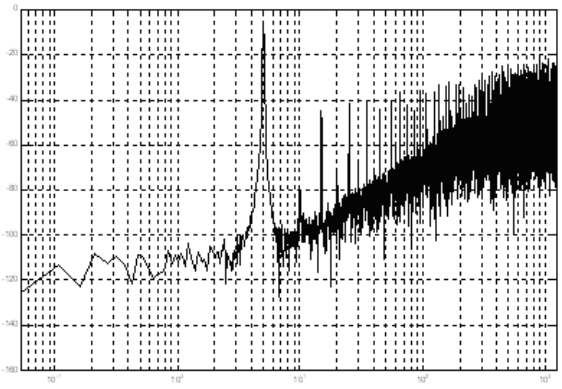

Figure 5. Simulated PSD after optimization

of the modulators. The design and optimization of a 16-bit second-order feed-forward sigma-delta modulator was also described with simulation results.

Acknowledgment

This work is sponsored by the National Natural Science Foundation of China under grant No.90207001.

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