An 0.9 x 1.2", Low Power, Energy-Harvesting System with Custom Multi-Channel Communication Interface

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Abstract

Presented is a self-powered computing system, Sunflower, that uses a novel combination of a PIN photodiode array, switching regulators, and a supercapacitor, to provide a small footprint renewable energy source. The design provides software-controlled power-adaptation facilities, for both the main processor and its peripherals. The system's power consumption is characterized, and its energy-scavenging efficiency is quantified with field measurements under a variety of weather conditions.

1 Introduction

The goal in developing the Sunflower hardware platform was to design a general purpose, miniature computing element, that could be used as the basis for evaluating ideas pertaining to the design of Macro-Sensor-Electro-Mechanical Systems (MSEMS). Like their *micro-scale* counterpart (MEMS), MSEMS combine electronics with mechanical actuation, and like *sensor networks*, involve multi-modal sensing on multiple computing nodes. Unlike MEMS, in which electric circuits and mechanical systems are integrated at the die-level, MSEMS incorporate computational devices (e.g., microcontrollers), sensors and mechanical actuators (e.g., *shape memory alloy strands*) over a large surface area, such as a sheet of plastic. Unlike sensor networks, which today typically involve *discrete* nodes manually placed in an environment, spanning a large area and thus necessarily communicating over *wireless* networks, MSEMS are *integrated* into the materials in which they control actuation, and thus can communicate over *wired* channels. With several nodes in proximity, a multi-channel wired interconnect can provide significantly reduced communication medium contention, as well as improved energy efficiency.

As an example, a microphone array application executing on an MSEMS substrate may utilize multiple sensors (microphones) and processing elements to implement a *beamforming* or speaker location algorithm. In order to improve the acoustic performance of the application, it may, under the control of software, change the physical shape of the substrate. One such conformational change might be, e.g., making the substrate concave towards the detected sound source, by activation of actuators embedded within the material. This is illustrated in Figure 1.

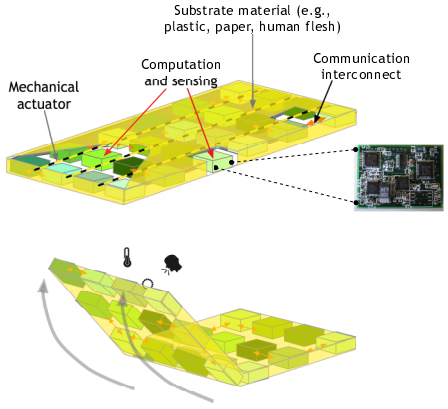

Figure 1. Illustration of the target application domain for the Sunflower platform.

This target application domain for the Sunflower hardware platform imposes constraints of (1) *low power consumption*, (2) the availability of *multiple wired communication interfaces*, and (3) *small overall size and weight*, including that of the energy source. The second constraint arises from the desire to interconnect multiple systems in topologies that enable *path diversity*. The constraints of small size and minimal weight arise from the need to use actuators to achieve mechanical control of the materials in which the nodes are embedded; the use of weighty energy sources (e.g., AAA or CR2032 batteries) is therefore undesirable. The desire to embed these hardware devices permanently in materials precludes the use of components whose performance may degrade significantly over time, further motivating the investigation of alternatives to the use of electrochemical batteries.

2 System Overview

These constraints guided the design of the system architecture, shown in Figure 2. Central to the design is an MSP430F1232 microcontroller from Texas Instruments (TI). The first of the aforementioned constraints is addressed by

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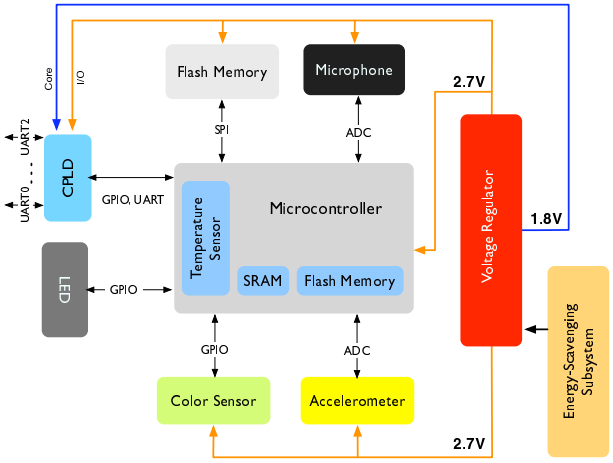


Figure 2. Sunflower system architecture.

incorporating hardware facilities to enable software to take advantage of all power saving modes of the microcontroller and other system components. The second design constraint listed above is addressed by implementing a custom communication interface for the microcontroller, within a Xilinx XC2C32A *complex programmable logic device* (CPLD). All components in the system were carefully chosen to minimize printed circuit board (PCB) area, device count, and weight, addressing the third design constraint listed above.

The Sunflower system incorporates an unconventional energy scavenging subsystem, composed of an array of PIN photodiodes, a boost switching regulator, and a miniature surface-mount supercapacitor, enabling a PCB implementation in less than $2cm^2$. In measurements performed on the prototype hardware, the photodiode array and boost converter can charge the supercapacitor to a potential sufficient to start the system's voltage regulators in approximately one hour. Under ideal lighting conditions, the supercapacitor can be charged to full potential in approximately five hours. In the absence of sunlight, it can power the system for up to four hours when executing a low-duty-cycle application, and longer if all the devices in the system are in their low-power states. The system can also be charged remotely, (and at much higher speed than by sunlight,) by illuminating the PIN photodiode array with a light source such as a laser, from a distance; this is demonstrated in Section 6.1.

The system incorporates a wealth of sensors: a programmable color detector, a microphone, a two-axis accelerometer and a temperature sensor, as well as up to 8MB of Flash memory and a software controllable LED. Due to the differing power rail requirements of these diverse devices, a dual-output high efficiency switching regulator is used to provide two voltage rails. The microcontroller takes advantage of features of this power regulation subsystem, as well as power-down features of the individual components in the system, to provide multiple opportunities for power saving.

A miniature 20-pin connector provides an interface for programming the microcontroller and loading designs into the CPLD, via their respective JTAG (Joint Test Action Group, IEEE standard 1149.1) interfaces. Since general purpose I/O pins of the microcontroller, as well as both voltage rails are available at this header, it can be used as an expansion connector for the connection of a daughter-card. For example, this interface is being used for a daughter card with an IEEE 802.15.4 radio, to enable the repurposing of the Sunflower hardware in applications such as wireless sensor networks. The devices used in the design, their manufacturer-specified operating voltage ranges, and power budgets, are listed in Table 2. In addition to the devices listed in the table, there are additionally over fifty surface-mount passive devices (resistors, capacitors, inductors) in the design.

The hardware design was carried out using Cadence CIS for schematic capture, and Orcad PCB for layout. To meet the goal of minimal size, the hardware is implemented in a six layer printed circuit board process, on 0.032" FR4 laminate, with four signal/routing layers and two plane layers (for ground and one of the voltage rails). The (unpopulated) printed circuit board size is 0.9" $\times$ 1.2" $\times$ 0.032", and was manufactured using a lead-free process. An annotated picture of the hardware platform is shown in Figure 3.

A comparison of the Sunflower hardware to several existing research and commercial sensor platforms is presented in Table 1. Even though the Sunflower hardware was designed *primarily* for use in investigation of the construction of high-density MSEMS platforms with multi-channel *wired* communication interfaces, such comparisons are relevant since they illustrate the state-of-the-art in the closest related application domain. Furthermore, due to its expansion interface, the Sunflower hardware may be repurposed as a wireless sensor node. The hardware platforms listed in Table 1 represent various points in a tradeoff space. For example, while the Econode platform [4] is smaller in volume than the Sunflower hardware, it contains a less energy-efficient microcontroller, fewer sensors, and has no capabilities for energy scavenging.

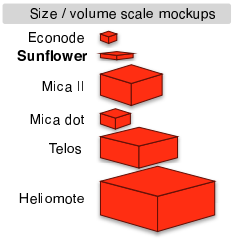
The following section describes the facilities for power adaptation in the Sunflower hardware. Section 4 briefly overviews the implementation of the system's communication interface, followed by a description of the design's power regulation system in Section 5. The energy-scavenging subsystem is described in Section 6, and Section 7 concludes.

3 Power-adaptive design

The heart of the system is a 16-bit MSP430 microcontroller (MSP430F1232) from Texas Instruments. The device features 8KB of on-chip flash memory for code and data storage, and 256 bytes of RAM. It operates at software-selectable clock speeds of up to 8MHz, with operating volt-

Table 1. Comparison of the Sunflower hardware platform to contemporary sensor platforms.

Platform	Size w/ battery (units are inches)	Energy scavenging	Min. current (CPU)	Max. system lifetime	Default # sensors	# comms interfaces
Sunflower	$1.2 \times 0.9 \times 0.2$	Yes	$0.7\mu A$	Unlimited	4	3, wired
Mica II mote	$2.0 \times 1.5 \times 1.2$	No	$5\mu A$	< 5 years	0	1, wireless
Mica dot	1.0 diam., 0.5 ht.	No	$2\mu A$	< 5 years	0	1, wireless
Econode	$0.5 \times 0.5 \times 0.3$	No	$2\mu A$	< 5 years	1	1, wireless
Telos mote	$1.3 \times 3.2 \times 1.1$	No	$1.1\mu A$	< 5 years	≤ 3	1, wireless
Heliomote	$\gg 2.0 \times 1.5 \times 1.2$	Yes	$5\mu A$	< 5 years	0	1, wireless



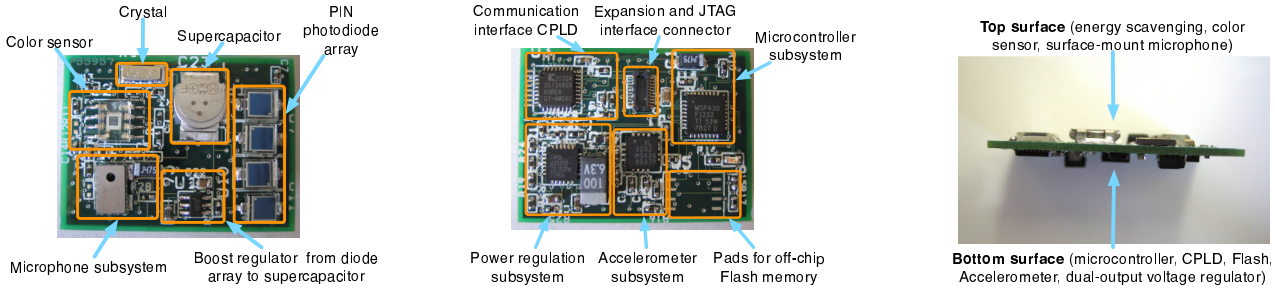


Figure 3. Pictures of a Sunflower hardware device (actual size on printed page). Top surface (left) and bottom surface (middle) and side/edge view (right).

age in the range of 1.8V to 3.6V; in the Sunflower hardware design, the operating voltage is fixed at 2.7V. This is the lowest voltage at which the microcontroller could be operated without resorting to voltage level converters for interfacing to the connected peripherals, as can be seen in Table 2. This design decision positively impacts the system's power consumption, as the leakage power of the microcontroller is lower at this reduced operating voltage, and dynamic power is also reduced (but dependent on workload). Furthermore, the power cost of additional level converter ICs (for interfacing to peripherals if they were operating at different voltages), which could be comparable to that of the microcontroller, is eliminated.

3.1 Microcontroller power adaptation

The MSP430 microcontroller features six different operating states: an *active mode* and five *low power modes* (referred to as *LPM0* through *LPM4*), which can be activated by setting appropriate bits in a system status register. In addition to these low power modes, the operating frequency can be set under software control. Such frequency scaling does not lead to *energy* reduction for compute-intensive applications — while the average power is reduced by frequency scaling, the overall time to complete a computation is increased, and the energy consumed remains the same. Even worse, if the computation involves communicating with peripherals, then since computation is progressing more slowly, the peripherals will need to be active longer, leading to an *increase* in energy consumption. The low power modes however provide the ability for reduction in energy consumption by deactivating components in the MSP430 microarchitecture.

Underlying the first four low power modes (LPM0 – LPM3) is the use of an appropriate clock source for the microcontroller's *timer unit*, which can be programmed to generate periodic interrupts, waking the CPU from sleep. The microcontroller can synthesize its own clock using an on-chip *digitally controlled oscillator (DCO)*, and this can be provided as the clock for the timer unit. The DCO is however disabled in power modes LPM1 to LPM4[1]. In LPM1 – LPM3, an external crystal may be used to provide a reference for an on-chip oscillator, however this source is also deactivated in the lowest power mode, LPM4.

The lowest-power sleep mode, LPM4 may be viewed as more of a *power-down-* or *stop-mode* than a sleep mode. In this sleep mode, while the power consumption is about 3000 times less than that in active mode, the processor can only by woken by an external interrupt source, e.g., as a result of a user pressing a button, as all clocks are disabled. In order to use this mode for *timed system sleep* functionality, a means of generating external interrupts after a time delay is required.

The Sunflower hardware design facilitates the use of all five low power modes, including LPM4. LPM1 – LPM3 are facilitated by the inclusion of an external 32.768kHz crystal to provide a clock reference. The microcontroller uses this reference to synthesize on-chip clock frequencies of up to 8MHz. LPM4, the lowest-power mode, is facilitated by the well known technique of using an external R-C circuit to generate a delayed interrupt trigger. Before entering LPM4,

[1]This description is a slight simplification.

Table 2. Operating voltage ranges and power budgets for the design's active components.

Device	Voltage Range	Power consumption at 2.7V (1.8V for CPLD core)
MSP430F1232 (microcontroller)	1.8V – 3.6V	0.270μW (LPM4), 0.540mW (active, 1MHz)
ADXL320 (accelerometer)	2.4V – 5.25V	0.945mW
TCS230 (color sensor)	2.7V – 5.5V	18.9 μW power down, 5.4mW active
XC2C32A (CPLD/comms. interface) core	1.7V – 1.9V	59.4μW (quiescent)
XC2C32A (CPLD/comms. interface) LVCMOS2.5 I/O	2.3V – 2.7V	—
AT45DBxx (off-chip Flash memory)	2.5V – 3.6V	0.025mW power-down, 0.063mW standby 18.9mW read
SP0103 (microphone)	1.5V – 5.5V	0.473mW
TPS61070 switching boost regulator	0.9V – 5.5V	0.051mW
TPS61100 dual-output boost/LDO	0.8V – 3.3V	0.175mW

software configures an I/O pin, connected to an R-C network, to generate interrupts on a rising edge. Another I/O pin, also connected to this R-C network, is subsequently driven high. After a delay dependent on the R-C time constant, the microcontroller receives an interrupt due to the rising edge at the R-C circuit; in our design, this delay is approximately 0.5s. Using this basic facility, we implemented a software routine to enable an LPM4 sleep of any duration (with 0.5s granularity). The power dissipated in the R-C circuit as well as the charge lost therein each cycle, negates some of the benefits of this sleep circuit approach. We are currently investigating more efficient means of enabling use of LPM4, and these are outlined in Section 7.

3.2 System-level power adaptation

The microcontroller is just one component of the system, and reduction of overall system energy consumption requires intelligent power control of all components, including the peripherals. The Sunflower hardware design enables the microcontroller to shutdown the color sensor and external Flash memory under the control of software to reduce their power dissipation. The accelerometer and microphone do not have facilities for device shutdown. Future directions for evolution of the platform include investigating techniques such as using FET switches to gate the voltage rails of peripherals, or even powering them directly from I/O pins of the microcontroller, providing further software-controlled power management.

Another source of power dissipation is the voltage regulator. A combined switching / LDO dual-output regulator, the TI TPS61100, is used to provide two voltage rails for the system, operating off the energy store (the energy scavenging subsystem, described in Section 6). It provides energy conversion efficiencies in the range of 65%–95%, depending on the output current. Poor efficiencies at low load currents necessitate the consideration of techniques to deactivate or bypass the voltage regulator while the system components are idle.

The Sunflower hardware takes advantage of a feature of the TPS61100 to deactivate the regulator's internal pulse-width modulation (PWM) engine, to improve conversion efficiency at low load currents. The design makes this facility available to software running on the MSP430, providing further opportunities for energy conservation. (This facility is described in detail in Section 5.)

4 Communication interface

One of the design goals of the Sunflower hardware platform was to endow the hardware with multiple, addressable, *wired* communication interfaces. This is desirable for the target hardware platform, MSEMS, (described in Section 1,) in which our goal is to construct systems comprising hundreds of devices in areas as small as a square foot. In such scenarios, wired communication interfaces become desirable over wireless ones — at such high spatial densities of devices, there could be significant interference in a shared wireless channel. A multi-link wired channel on the other hand enables efficient isolation of local communications, and also affords the possibility of significant reduction in communication power consumption.

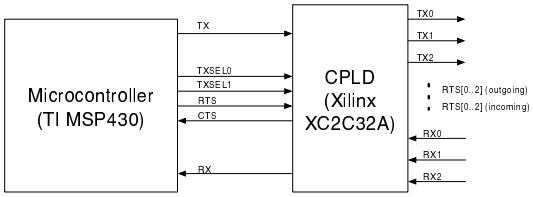


Figure 4. Interface between microcontroller and communication interface CPLD.

A multi-channel wired interface was implemented by multiplexing the MSP430's hardware UART using a circuit implemented within a Xilinx XC2C32A complex programmable logic device (CPLD). The XC2C32A provides programmable logic in the smallest available board space, and has very low power dissipation. The interface between the communication interface and microcontroller is shown in Figure 4. The microcontroller's UART is multiplexed into three communication interfaces which are software addressable, with added hardware flow control support. The design uses only 9 of the CPLD's 32 macrocells, and 16 of the 80 functional blocks in the CPLD. None of the CPLD's 32 registers are used since it is a completely combinational design.

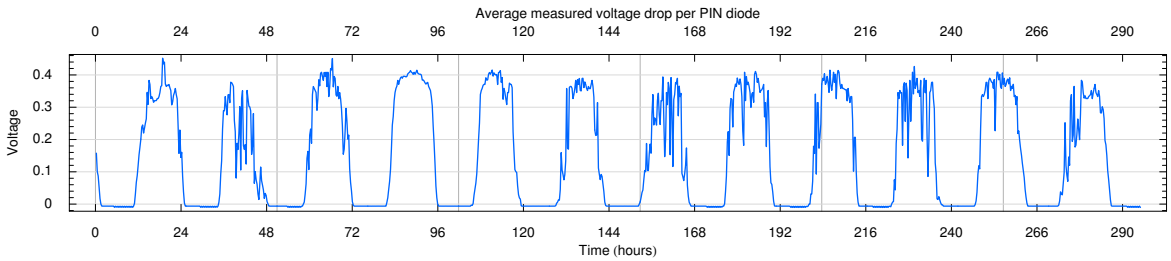


Figure 5. Average potential drop per PIN photodiode, across a 12 day period (May 6th 2006, 7:23pm – May 18th 2006). The measurements were taken at longitude $40.4422°N$ latitude $79.9464°W$, elevation 900ft, in an indoor environment, close to a window, but not in direct sunlight.

The left-over resources (71% unused macrocells, 80% unused functional blocks, 100% unused registers) can be utilized by users of the Sunflower hardware platform for other purposes.

5 Power Regulation Subsystem

The power regulation subsystem provides two regulated voltage rails of 1.8V (for the CPLD core voltage) and 2.7V (for the CPLD I/O voltage and all other devices). It is implemented with a TI TPS61100 dual-output regulator, which is composed internally of a switching boost converter and a low dropout voltage (LDO) regulator.

The power regulator may dissipate power even though all the devices in the system which it drives are in idle modes. This is exacerbated by the fact that, at low load currents, the regulator will typically have a *reduced* efficiency. In order to conserve the energy store of the system, it is possible to shut down the switching regulator (deactivating its internal pulse-width modulation (PWM) circuit), such that the output load runs directly off the regulator's output capacitor. In the Sunflower hardware design, after software running on the microcontroller shuts down unused peripherals, it can further conserve energy by enabling this mode in the voltage regulator. When the regulator output capacitor drops below a threshold, the TPS61100 automatically reactivates.

The TPS61100 provides two signals for monitoring its *input* supply voltage (i.e., the output voltage of the energy storage subsystem). These signals, which are connected to the microcontroller, provide four threshold alert signals about the condition of the system's energy store, and enable *adaptive power management* based on the state of the energy store. For example, software can change the microcontroller's operating frequency to reduce power consumption to that which is optimal for the efficiency of the voltage regulator, given the current level of the energy store.

6 Energy Scavenging Subsystem

Contemporary research has previously investigated forms of energy scavenging as varied as solar, piezoelectric, mechanical and thermal gradient approaches [2]. Compared to contemporary integrated self-powered platforms such as Everlast [6], Sunflower is over an order of magnitude smaller in volume, albeit intended for different purposes. In contrast to energy harvesting systems such as the Heliomote [5] add-on board for the Mica 2 platform, the Prometheus add-on for the Telos Mote hardware [1], and the AmbiMax energy scavenging hardware [3], the energy-harvesting circuit in Sunflower is completely integrated into the system's already miniature design. This integration is enabled by the use of a novel combination of an array of PIN photodiodes, a boost switching converter, and a miniature surface-mount supercapacitor, to provide a small footprint renewable energy source.

Although it is possible to use the photodiode array to directly charge an energy storage device (in this case an 0.2F supercapacitor), the potential drop across each photodiode is typically only 0.4V, in daylight. Figure 5 shows the measured average potential drop per photodiode, over the course of a 12 day period. Based on these measurements, using the array of four PIN photodiodes in the Sunflower platform to directly charge the supercapacitor would mean charging it to only one half of its capacity (i.e., approximately 1.6V versus its rated voltage of 3.4V), regardless of how long the system was exposed to sunlight. In order to make full use of periods of available sunshine, the four PIN photodiode array in the Sunflower platform is connected to the supercapacitor through a switching boost converter (TI TPS61070). The TPS61070 has a startup voltage of 0.8V, thus can fully charge the supercapacitor storage cell in lighting conditions which yield as little as 0.2V per diode. The additional circuit board overhead of the boost converter subsystem is approximately that of a single photodiode.

Figure 6 shows the charging curve for the system's energy store, the 0.2F supercapacitor, being driven by the energy-scavenging subsystem (PIN photodiode array and boost converter), in outdoor lighting conditions.

6.1 Remote charging via infrared laser

The energy scavenging subsystem affords opportunities for remote charging. This might be useful, for example, when extended periods of darkness have caused the energy store to be fully depleted. Although effective in terrestrial

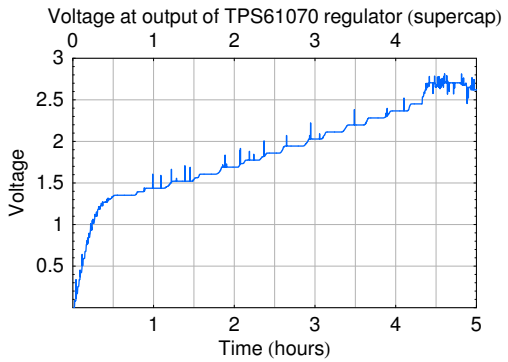


Figure 6. Performance evaluation of the boost converter subsystem.

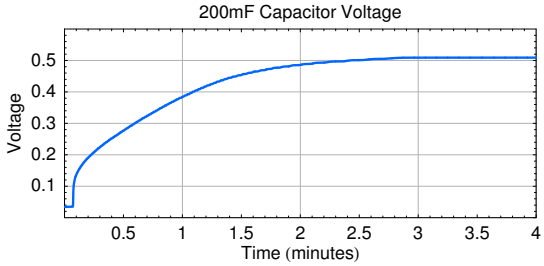


Figure 7. Charging of 0.2F supercapacitor with a single PIN photodiode, illuminated via a 5mW (optical output) infrared laser, operated off a 2.0V supply, and drawing 30mA.

sunlight, the PIN photodiode array employed in the scavenging circuit has a peak sensitivity at 850nm, in the infrared portion of the electromagnetic spectrum. While remote charging can be achieved via illumination with a bright spotlight (e.g., from an incandescent light source), the amount of energy needed to drive such a spotlight could be large, of the order of hundreds of Watts.

To investigate energy-efficient remote charging, we employed a collimated light source, an 850nm class IIIb infrared laser, whose wavelength matches the optimum sensitivity of the PIN photodiodes. Figure 7 shows the capacitor charging curve for a single photodiode (i.e., one-quarter of the full scavenging unit), illuminated with the laser, driving the 0.2F energy storage supercapacitor. Using this matched light source, the energy-scavenging subsystem can be fully charged in approximately five minutes compared to five hours in sunlight.

7 Summary and Future Work

The Sunflower platform is a miniature self-powered computing system that uses a novel combination of an array of PIN photodiodes, a switching regulator, and a supercapacitor, to provide a small footprint energy-scavenging power source. It was designed as a platform for the investigation of ideas related to the construction of Macro-scale Sensor Electro-Mechanical Systems (MSEMS).

The system incorporates several sensors into its tiny 1.2×0.9" six layer PCB — a programmable color detector, a microphone, an accelerometer and a temperature sensor, as well as up to 8MB of Flash memory and a software controllable LED. It facilitates multiple opportunities for dynamic power adaptation of the system's main microcontroller, its peripherals, as well as adaptation to the state of the energy store.

We are currently pursuing several directions for improvements in the design. The accelerometer and microphone peripherals may be power-managed by powering them directly off an I/O pin of the microcontroller (they consume sufficiently small current to make this feasible), or their operating voltage rails may be gated with a low-quiescent current FET switch. The utilization of the microcontrollers deep sleep mode may be made more efficient by the use of an external watchdog timer for waking the microcontroller from sleep in place of the currently-employed R-C sleep circuit. Other directions being pursued include the integration of additional sensors such as humidity sensors.

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