# Tutorials

**A1 Organic Computing**

Organiser: Rolf P Würtz, Bochum U, DE
Speakers: Rolf P Würtz, Bochum U, DE
Andreas Herkersdorf, TU Munich, DE
Falko Dresler, Erlangen-Nurnberg U, DE

The rapidly rising complexity in information processing systems calls for novel methods for designing and organising them, thus relieving the designer from the burden of planning all details, in short, to help artificial systems self-organise. This self-organisation of highly complex structures prevails in living systems, and "Organic Computing" is an attempt to uncover its principles and make them fruitful for design. In the tutorial, its methodology is exemplified on the application domains of artificial face recognition, system on chip design, and self-organisation of autonomous sensor/actuator networks.

The tutorial is geared towards system designers and computer scientists who wish to evaluate the potential of Organic Computing methods.

**B1 Model-Based Composition of Embedded Software and Systems**

Organiser: Joseph Sifakis, VERIMAG, FR
Speakers: Joseph Sifakis, VERIMAG, FR
Janos Sztipanovits, ISIS-Vanderbilt, US

Model-based design of embedded software and systems is founded on the *formal representation, composition, analysis and manipulation of models* in the design process. The tutorial focuses on state-of-the-art model-based design in two complementary directions: composition of domain-specific tool chains as well as composition of embedded software and systems. In the first part, we will discuss and demonstrate core elements of a technology infrastructure for composing domain-specific tool chains and its application to automotive using the open source Model-Integrated Computing (MIC) tool suite. In the second part, we will present a framework for the component-based design of embedded systems and its implementation, based on a general semantic model encompassing various models of computation. Lastly, we explore the relationship between the two composition directions.

**C1 Tackling Design and Circuit Marginalities during Test**

Organiser/
Speaker： Sandip Kundu, Massachusetts U, US

An increasing number of chip failures are caused by circuit marginalities. Circuit marginality encompasses failures due to unsafe design approximations, process variations, and failure to account for some electrical and thermal properties of a chip. In this tutorial, we will describe physical causes, modeling approaches for pattern generation and general discussion on avoidance techniques.

The tutorial is targeted to practicing Engineers, Students and University Faculty.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP).

**D1 Formal Verification – Today and in the Future**

Organiser: Rolf Drechsler, Bremen U, DE
Speakers: Rolf Drechsler, Bremen U, DE
Juergen Ruf, IBM, DE

With increasing design complexity, verification becomes a more and more important aspect of state-of-the-art design flows. Modern circuits contain up to several hundred million transistors. In the meantime it has been observed that verification becomes the major bottleneck, i.e. up to 80% of the overall design costs are due to verification. In this

tutorial, after a brief motivation of the overall topic and definition of the problem domain, the alternative verification approaches are explained and pro and cons are discussed. These approaches include simulation, emulation and formal methods. For the last one more details are discussed related to formal verification, symbolic simulation and assertions based verification. Then the verification scenarios for equivalence checking (EC) and property checking (PC) are presented and the underlying proof techniques are explained. We focus on several case studies to provide an in depth understanding of the techniques. Among the examples are the formal verification of a RISC CPU, system level verification using SystemC and verification in an industrial environment using commercially available tools using the property specification language PSL. Directions for future work and research challenges are pointed out.

**A2 Sensor Networks**

Organiser: Wayne Wolf, Princeton U, US
Speakers: Robert P Adler, Intel, US
Lothar Thiele, ETH Zuerich, CH
Janos Sztipanovits, Vanderbilt U, US
Wayne Wolf, Princeton U, US

Sensor networks are an important research area and a growing application area for VLSI systems. Sensor networks have been applied to environmental monitoring, civil engineering structures, and physical security. These systems represent a new and different computing platform that introduces challenges at all levels of abstraction, ranging from very low power design through algorithms. This tutorial will review basic concepts of wireless sensor networks, including: ad-hoc networking, programming models, power management, in-network processing, development environments and methodologies.

**B2 UML and Model-Driven Development for SoC**

Organiser Wolfgang Mueller, Paderborn U, DE
Speakers: Wolfgang Mueller, Paderborn U, DE
Yves Vanderperren, KU Leuven, BE
Wim Dehaene, KU Leuven, BE

This tutorial introduces the basic concepts of UML 2.0 and the key ideas of the Model Driven-Architecture (MDA) design process for application in SoC design. The first part starts with a self-contained, comprehensive overview of the UML 2.0 with focus on relevant parts for architectural and behavioural descriptions. Thereafter, we introduce the basic concepts of application-specific UML adaptations via UML profiles and recent developments in the definition of SysML (System Modelling Language) and the SoC profile. The second part of the tutorial presents the basic principles of Model-Driven Architecture (MDA) and its relevance and implications for tools. After an overview of current SoC design flows which integrate UML, the tutorial finally closes with a discussion of future perspectives beyond the question of languages and tools.

**C2 Scan-Based Debug and Diagnosis**

Organiser: Geir Eide, Mentor Graphics Corp, US
Speakers: Geir Eide, Mentor Graphics Corp, US
Al Crouch, Inovys Corp, US

Most digital IC designs today use DFT techniques like internal scan and BIST to increase the design's testability and automate the test generation process. This tutorial is an investigation into detecting and isolating design errors and logic problems using structural techniques and scan architectures. When implemented the right way, scan and other DFT techniques can be used to simplify debug and diagnosis of silicon during device bring-up on the tester, characterisation, and failure analysis. Some of the techniques also apply to debug of test vector simulation. The tutorial covers how to utilize existing DFT structures as well as how to explicitly design for debug (DFD). Prerequisites are basic DFT knowledge, particularly internal scan.

The tutorial is targeted designers of integrated circuits (ICs) and system-on-chips (SoCs), IP core providers and integrators, test engineers, researchers, and managers who are involved in silicon debug, have basic to intermediate DFT knowledge, and would like to learn how to leverage DFT and structural techniques in hunting design bugs observed in silicon.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP).

**D2 VHDL-AMS Tutorial Including Automotive and Zigbee Case Studies**

Organiser: Marius Sida, Mentor Graphics, DE
Speakers: Marius Sida, Mentor Graphics, DE
Juergen Schaefer, Infineon, DE
Khanh Tuan-Le, Chipcon

This tutorial will start with an introduction to the VHDL-AMS language and its use for mixed signal top down design methodology. After a short review of some syntax elements and some basic examples, we will continue with practical guidelines for effective model and library development. After that, the tutorial will focus on testbenchcreation and regression setup. The tutorial will continue with two industrial case studies: (1) Automotive Bus System Development using VHDL-AMS to model the bus transceiver as a mixed-signal model in a physical layer system level. (2) ZigBee wireless technology with focus on modeling the PHY layer in order to achieve feasible architectures for a cost-effective implementation of IEEE 802.15.4 and Zigbee compliant solutions. Both cases are using VHDL-AMS to describe and analyses the specific application area.

**E The CELL Processor**

Organiser: Dac Pham, STI Chief Engineer and Global Convergence Manager
Speakers: Jim Kahle, IBM Fellow and Chief Technologist for Custom Power System
Dac Pham, STI Chief Engineer and Global Convergence Manager

The Cell processor is a first instance of a new family of processors intended for the broadband era. Cell is a non-homogeneous multi-core processor, with one POWER processor core (two threads) dedicated to the operating system and other control functions, and eight synergistic processors optimised for compute-intensive applications. The Cell processor supports many of today's programming models by introducing the concept of heterogenous tasks or threads.

The first part of the tutorial focuses on the hardware and software architectures for the CELL processor. The second part reviews the design challenges that current and future processors must face, with stringent power limits and high frequency targets, and the design methods required to overcome the above challenges and address the continuing Giga-scale system integration trend. We describe the details behind the design methodology that was used to successfully implement a first-generation CELL processor - a multi-core SoC.

The tutorial is targeted researchers and developers of advanced system architecture, software, processor design, and VLSI design systems.

**F Four New Ways to Design a High Definition Video CODEC**

Organiser: Ahmed Jerraya, TIMA Laboratory, FR
Speakers: Youn-Long Steve Lin, National Tsing-Hua U/Global UniChip Corp, Taiwan, ROC
Chris Rowen, Founder and CEO, Tensilica, US
John Glossner, CTO, Stanbridge Technologies, US
Kees Vissers, Xilinx, US
Andreas Hoffmann, CoWare, DE

This tutorial compares the traditional RTL Design and Verification Methodology with four new ESL design technologies that feature full HW/SW integrated design flows. Innovative solutions are proposed to master SoC design complexity. These are: Multiple Extensible Processors; Combination of powerful platform and multithreading compiler; Combination of HW and SW programmability; System level EDA. In order to allow attendees to understand the capabilities, the advantages and performances of the different approaches, we show their application on a high definition Video Codec.

**G DFM Tools and Methodologies for 65nm and Below**

Organiser: Andrew B Kahng, UC San Diego and Blaze DFM Inc, US

Speakers: Andrew B Kahng, UC San Diego and Blaze DFM Inc, US
Louis K Scheffer, Cadence Design Systems Inc, US
Andrzej Strojwas, PDF Solutions Inc and CMU, US
Michael Orshansky, Univ. of Texas at Austin, US
N S Nagarai, Texas Instruments, US

This tutorial will present a view of key tool technologies and methodologies that are likely to become mainstream for the 65nm node and beyond. Topics include: (1) taxonomy of yield detractors and variability sources; (2) statistical extraction and performance analysis, (3) parametric yield optimisations for timing, power and reliability; (4) manufacturing simulations and analyses for shape (litho and etch), thickness (planarisation), and defectivity (critical area); (5) manufacturing-aware capabilities in placement, routing, and post-route optimisation tools; and (6) layout synthesis methodologies that range from restricted design rules to flexible layout and liquid libraries.