

	<b>DATE rep at DAC</b> Ahmed Jerraya TIMA Laboratory, FR		<b>DAC rep at DATE</b> Ellen M. Sentovich Cadence, US
	<b>EDAC Liaison Chair</b> Anne Cirkel Mentor Graphics, US		<b>EDAC Liaison Chair</b> Pamela Parrish EDA Consortium, US
	<b>ASPDAC rep at DATE</b> Masaharu Imai Osaka University, JP		<b>Audit Co-Chair</b> Robert Gardner EDA Consortium, US
	<b>Event Manager</b> Andrew Porter EDA Exhibitions Ltd, UK		<b>Exhibition Manager</b> Emma Norton EDA Exhibitions Ltd, UK
	<b>Conference Manager</b> Sue Menzies European Conferences, UK		

## technical programme topic chairs

	<b>System Design Methods &amp; Case Studies</b> Harry Hsieh UC Riverside, US		<b>System Design Methods &amp; Case Studies</b> Grant Martin Tensilica, US
	<b>Analogue &amp; Mixed AD Systems</b> Angel Rodriguez-Vazquez CNM/IMSE, ES		<b>Analogue &amp; Mixed AD Systems</b> Manfred Glesner TU Darmstadt, DE
	<b>Design of Low-Power Systems &amp; Case Studies</b> Christian Piguet CSEM, CH		<b>Design of Low-Power Systems &amp; Case Studies</b> Tajana Simunic UC San Diego, US
	<b>Microarchitectural &amp; Architectural Design</b> Todd Austin The University of Michigan, US		<b>Microarchitectural &amp; Architectural Design</b> Stamatios Vassiliadis TU Delft, NL
	<b>Reconfigurable Computing</b> Walid Najjar UC Riverside, US		<b>Reconfigurable Computing</b> Wayne Luk Imperial College London, UK
	<b>Innovative &amp; Emerging Technologies, Systems &amp; Applications</b> Vijaykrishnan Narayanan Pennsylvania State U, US		<b>Innovative &amp; Emerging Technologies, Systems &amp; Applications</b> Christian Paulus Siemens, DE
	<b>Multi-Processors &amp; Networks on Chip</b> Luca Benini DEIS - Bologna U, IT		<b>Multi-Processors &amp; Networks on Chip</b> Kees Goossens Philips, NL
	<b>System-Level Specification &amp; Modelling</b> Satnam Singh Microsoft, US		<b>System-Level Specification &amp; Modelling</b> Ian Oliver Nokia, FI
	<b>Simulation &amp; Emulation</b> Mostapha Aboulhamid Montreal U, CA		<b>Simulation &amp; Emulation</b> Franco Fummi Verona U, IT
	<b>System Synthesis &amp; Optimisation</b> Juergen Teich Erlangen-Nuremberg U, DE		<b>System Synthesis &amp; Optimisation</b> Nikil Dutt UC Irvine, US
	<b>Architectural Synthesis</b> Roman Hermida UC Madrid, ES		<b>Architectural Synthesis</b> Fabrizio Ferrandi Politecnico di Milano, IT
	<b>Logic &amp; Technology Dependent Synthesis for Deep Submicron Circuits</b> Tiziano Villa PARADES, IT		<b>Logic &amp; Technology Dependent Synthesis for Deep Submicron Circuits</b> Jordi Cortadella UP Catalunya, ES
	<b>Physical Design &amp; Verification</b> Andreas Kuehlmann Cadence, DE		<b>Physical Design &amp; Verification</b> Juergen Koehl IBM, DE