The Ultra Low-Power WiseNET System

A. El-Hoiydi, C. Arm, R. Caseiro, S. Cserveny, J.-D. Decotignie, C. Enz,
F. Giroud, S. Gyger, E. Leroux, T. Melly, V. Peiris, F. Pengg,
P.-D. Pfister, N. Raemy, A. Ribordy, D. Ruffieux, P. Volet
Swiss Center for Electronics and Microtechnology (CSEM), Neuchâtel, Switzerland *

Abstract

The WiseNET system includes an ultra low-power system-on-chip (SoC) hardware platform and WiseMAC, a low power medium access control protocol (MAC) dedicated to duty-cycled radios. Both elements have been designed to meet the specific requirements of wireless sensor networks and are particularly well suited to ad-hoc and hybrid networks. The WiseNET radio offers dual-band operation (434-MHz and 868-MHz) and runs from a single 1.5-V battery. It consumes only 2.5-mW in receive mode with a sensitivity smaller than -108*-dBm at a BER of* 10^{-3} *and for a 100-kb/s data rate. In addition to this low-power radio, the WiseNET system-on-chip (SoC) also includes all the functions required for data acquisition, processing and storage of the information provided by the sensors. Ultra-low power consumption with the WiseNET system is achieved thanks to the combination of the low power consumption of the transceiver and the high energy efficiency of the WiseMAC protocol. The WiseNET solution consumes more than 250 times less power than comparable solutions based on the IEEE 802.15.4 standard.*

1. Introduction

A network of wireless sensors consists of a large number of energy-autonomous microsensors distributed in an area of interest. Each node monitors its local environment, locally processes and stores the collected data so it can be used by other nodes. It shares this information with the other neighboring nodes by using a wireless link. Specific features of interest to the end-user can be extracted from the different information collected by several nodes by using data fusion while this information is propagated to some base station node by a multi-hop communication scheme [1, 2].

The objective of the WiseNET project at CSEM (Swiss Center for Microtechnology) [3] was to reach up to 10 years of battery life for the nodes of a multihop wireless sensor network (WSN) with limited latency (seconds to minutes). The objective has been tackled from two complementary perspectives, improving transceiver power consumption and reducing the duty cycle using innovative medium access control schemes. The basic design choices will be presented and justified in Section 2. The medium access control protocol will then be described in Section 3 and the system-on-a-chip (SoC) designed within the project is presented in Section 4. The performances resulting from the combination of the protocol and the SoC are presented in Section 5, followed by some conclusions in Section 6.

2. Design Choices

To reduce power consumption, nodes will sleep as long as there is no operation to perform. When time comes, a sensor node will wake up and perform the measurement. Note that this wake-up may also be triggered by an external event. The node may then decide to communicate the collected information to some neighbor(s) and send them a message. Unfortunately the neighbor(s) may be sleeping to save energy. The node must hence keep sending the information until the neighbor wakes up and acknowledges the correct receipt of the information.

On the other hand, a node may need information from a neighbor. It may then try to send him a request message and will have to wait until the neighbor wakes up as in the previous case. Alternately, it may stay up and wait until the neighbor decides to send the information.

These two simplistic examples show that, if not properly designed, communication will increase significantly the power consumption because listening and emitting through a wireless channel is very power hungry. The challenge is therefore to reduce the different sources of energy waste, namely:

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- idle listening, which occurs when a node waits listening until a message is emitted by another node;
- over-emitting, which happens when a node sends a message although the destination node is not ready to receive it;
- collisions that occur when two nodes emit at the same time with the consequence that the messages must be retransmitted later at different times;
- overhearing, which takes place when a node listens for a message that is sent to another node and for which it is not the destination.

In our project, the challenge was to reach the lowest possible consumption in both extreme cases of fully ad-hoc and infrastructure networks and hence also for hybrid networks. To further reduce the power consumption, a careful hardware-software co-design approach was chosen. Communication protocols are often designed for existing integrated circuits with predefined specs. They must then take into account the special features of these circuits. Here, we had the opportunity to design the RF circuits and the protocols concurrently from the start. An initial analysis allowed to identify a few important parameters of the circuits that have a clear impact on the higher protocol layers:

- the power consumption in receive (respectively transmit) mode;
- the wake-up time, which is the time necessary to switch from the idle mode to the receive or the transmit mode. During this time the node cannot receive while the power consumption is almost the same as in receive mode.
- the time necessary to switch from the receive mode to the transmit mode or vice-versa (turnaround time);
- the receiver sensitivity and the maximum transmit power that have an impact on the number of hops and the collision probability;
- the bit and frame synchronization time at reception. The frame synchronization pattern has an impact on the overhead (its length) but also on the frame error rate when frame starts are detected erroneously;
- the presence of an effective RSSI (Receive Signal Strength Indicator), which can be used to improve the reliability of the frame detection. It also reduces idle listening when it is used as a silence detector;
- some way to filter incoming packets to reduce overhearing;
- the power consumption in sleep mode with a sufficiently accurate clock running all the time. Note that, depending on the application, the latter can become a major part of the current consumed during the node's life;
- the capacity to adjust emission power and receiver sensitivity to reduce the frame error rate and the collision probability.

Taking into account the special context of WSN, a few basic choices have been made. First, a reasonably high emission power (actually the maximum allowed in the selected bands) was chosen instead of trying to optimize the emission efficiency. This choice is justified by the fact that nodes will emit rarely and hence emission efficiency is not a high priority parameter. Second, the effort was focused in reducing the energy consumption in receive mode as well as the wake-up and turn-around times. Since a form of preamble scanning is used at the MAC layer, waking-up and switching quickly has a clear impact on power consumption. For the same reasons, the RSSI information has been carefully elaborated. As a third level of optimization, robust bit synchronization and packet filtering based on a programmable pattern has been added. Both reduce frame losses while the former additionally reduces overhearing.

3. WiseMAC

WiseMAC is a low power MAC protocol specially developed for WSN [4] in combination with the SoC presented in the next Section. It is a single channel contention protocol based on non-persistent carrier sense multiple access (CSMA). Non-persistent CSMA has been combined with preamble sampling to mitigate idle listening. The preamble sampling technique consists in regularly sampling the medium to check for activity. All nodes in a network sample the medium with the same constant period. Their relative sampling schedule offsets are independent. If the medium is found busy, a node continues to listen until a data packet is received or until the medium becomes idle again. At the transmitter, a wake-up preamble of size equal to the sampling period is transmitted in front of every data packet to ensure that the receiver will be awake at the start of the data portion of the transmission. This technique enables very low power consumption when the traffic is very low as it is usually the case in WSN. It provides the lowest possible power consumption in the absence of traffic and for a given wake-up latency using a conventional receiver. The main disadvantage of this basic preamble sampling protocol is that the low power consumption in idle mode is coupled with a high power consumption overhead both in transmit and receive, due to the wake-up preamble. In an ad-hoc network, the cost of reception is not only paid by the intended destination, but also by all other nodes overhearing the transmission. The novel scheme introduced by WiseMAC reduces the length of this costly wake-up preamble. It consists in learning and exploiting the sampling schedule of the direct neighboring nodes.

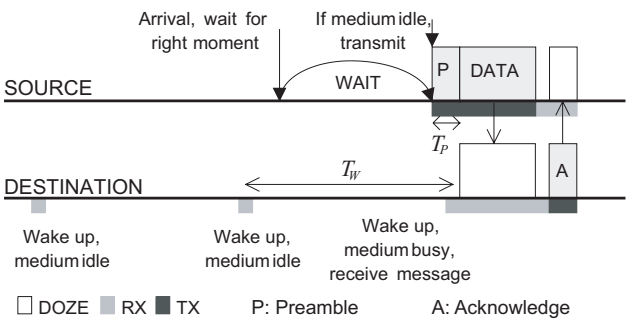

Figure 1. WiseMAC - Minimizing the wake-up preamble length.

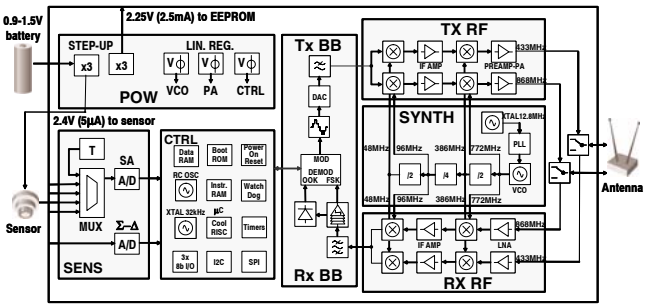

Figure 2. Block diagram of the WiseNET SoC.

To use a wake-up preamble of minimized size, as illustrated in Fig. 1, the sampling schedule of a neighbor is learned, or refreshed, during every data exchange by piggybacking in the acknowledgement messages the remaining time until the next sampling instant. Every node keeps a table of sampling time offsets of all its usual destinations up-to-date. Since a node will have only a few direct destinations, such a table is manageable even with very limited memory resources. The duration of the wake-up preamble must cover the potential clock drift between the clocks at the source and at the destination. This drift is proportional to the time since the last re-synchronization (i.e. the last time an acknowledgement was received). It can be shown that the required duration of the wake-up preamble is given by $T_P = \min(4\theta T_C, T_W)$, where θ is the frequency tolerance of the time-base quartz, T_W is the sampling period and T_C the interval between communications. A transmission is scheduled such that the middle of the wake-up preamble coincides with the expected sampling time of the destination. Systematic collision situations eventually introduced by this synchronization are mitigated using a wake-up preamble of randomized size.

4. The WiseNET SoC

The WiseNET SoC is the result of a major design effort to reduce power consumption to a minimum [5, 6, 7]. In addition to an ultra low-power dual-band transceiver, it also includes a sensor interface with a signal conditioner and two analog-to-digital converters (ADCs) (labelled SENS in Fig. 2), a digital control unit (labelled CTRL in Fig. 2) based on a Cool-RISC microcontroller (μC) with on-chip low-leakage memory (i.e. RAM) and several time basis (real-time clock,...) and digital interfaces (SPI, I2C, ...), and finally an important power management block (labelled POW in Fig. 2). Although all these blocks contribute to power consumption, the most critical one, as of today, remains the RF transceiver. The most important design objectives were:

- to keep the power consumption in receive mode within the mW range, like in the 1^{st}-generation of WiseNET transceiver [8, 9], while extending the operation to a dual-band operation by adding the 868-MHz SRD band;
- to operate from a single 1.5-V AA alkaline battery with a supply voltage as low as 0.9-V (corresponding to the battery end-of-life voltage) and achieve several years of autonomy;
- to use a 0.18-μm standard digital CMOS process (i.e. without any precision analog components such as capacitors and resistors nor dedicated RF technology options such as substrate isolation);
- to minimize the number of external components and the cost.

The dual-band operation combined with the use of several channels allows for frequency diversity to solve the difficult problem of rejecting strong nearby interferers. The choice of staying in the 434-MHz and 868-MHz bands instead of moving to the popular and worldwide available 2.4-GHz band is mainly related to power consumption. Indeed, an important part of the power consumption (about 50%) of a receiver is directly related to the circuits operating at or close to the RF frequency, such as the frequency synthesizer and the RF frontend (i.e. low-noise amplifier (LNA) and power amplifier (PA)) [5, 7]. Since the power consumption of these blocks is approximately proportional to frequency, choosing sub-GHz bands allows to limit the power consumption in the mW range. Also, it turns out that operating at 2.4-GHz with the chosen 0.18-μm CMOS process would require a supply voltage in the order of 1.8-V, which is incompatible with the target 0.9-V minimum supply voltage [5, 7].

Among the key radio parameters identified in Section 2, the power in receive mode has been minimized by first

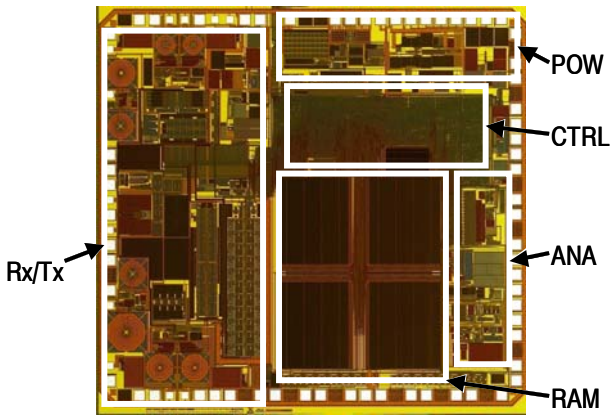

Figure 3. Microphotograph of the WiseNET SoC.

choosing a 0.18-μm CMOS standard digital process. This allows for the selected sub-GHz frequency bands to trade the high frequency capability of minimum length transistors with lower current consumption, by biasing the devices at a lower current densities (i.e. moving the operating points to the moderate and weak inversion regions), even for the devices working at RF. Biasing the devices in the moderate inversion also offers a good tradeoff between high current efficiency, low-voltage operation and reasonable linearity [5, 7].

Power consumption is also strongly conditioned by the selected radio architecture [5, 7]. Although a highly integrated solution is targeted, implementing the rejection of strong nearby interferers on-chip would have required a prohibitive dynamic range and power consumption due to the low-voltage requirement. This problem was circumvented by using an external RF filter such as a SAW device. The chosen radio architecture is a superheterodyne with a high-IF followed by a direct conversion to dc, similar to the on presented in [10]. This architecture has the advantage that a significant gain can be achieved at the IF without prohibitive power consumption, while the channel selection is performed around dc. Having sufficient gain at the IF also reduces the SNR degradation due to the strong 1/f noise present in deep-submicron CMOS processes and strongly affecting the analog baseband [5, 7].

Other external devices are a high-Q inductor used for the LC-tank in order to achieve the desired low phase noise and a few capacitors for the impedance matching to the antenna. Note that a special on-chip varactor had to be designed in the chosen process to operate at such a low voltage while still offering a sufficient tuning range and a high quality factor in order not to degrade the tank overall Q-factor. The WiseNET transceiver also offers a digital RSSI, which is

Supply voltage	$0.9 - 1.5$ V (Rx and Tx)
Operating frequency	433 and 862 MHz
Data rate	12.5/25/100 kb/s (FSK)
	2 kb/s (OOK)
Sleep current	$< 3.5\,\mu$A
Receiver (Rx) ($V_{DD} = 1.2$ V and at 25 °C)	
Supply current (433/868)	2.1 /2.1 mA
Sensitivity (FSK) (433/868)	-111 / -108 dBm
@ BER = 10^{-3} and 100 kb/s	
Sensitivity (OOK) (433/868)	-117 / -114 dBm
@ BER = 10^{-3} and 2 kb/s	
Transmitter (Tx) ($V_{DD} = 1.2$ V and at 25 °C)	
Supply current	27.6 / 32.3 mA
@ 10 dBm (433/868)	
FSK output power	10.5 / 9.5 dBm

Table 1. Main measured results for the Rx and Tx of the WiseNET transceiver [6].

used by the WiseMAC protocol for preamble sampling and carrier sense activities.

If all contributors within the receive chain are turned on, the total current drain is too prohibitive to enable long duration operation on a single battery. When analyzing the individual contributions, the current consumption happens to be obviously larger for the RF blocks and significantly smaller for the baseband blocks. This is because the current is directly related to the frequency of operation or the required bandwidth. On the other hand, turn-on times will vary inversely with the frequency of operation, baseband blocks requiring much more time to settle than RF blocks. Therefore, significant energy can be saved by waking up the lower power baseband blocks before the power consuming RF circuits that wake up very fast. The WiseNET chip offers a high degree of flexibility in controlling the individual operation of each blocks. A typical example of wake-up sequence that could be implemented is: first power-on the low-frequency reference clock, then the baseband path (channel filters, limiters, RSSI), followed by the frequency synthesizer and eventually the IF amplifiers and the RF front-end (LNA and down-conversion mixers). In addition, the sampling nature of WiseMAC can be efficiently exploited in the baseband part by turning on only the required block. For example, once the receiver chain down to the baseband channel filter has been activated, the RSSI can then measure the signal strength. If the activity is detected as sufficient by the RSSI, the demodulation blocks may then

be turned on for further symbol and frame analysis and error correction. In the case the power level is lower than an acceptable threshold, either the other channels or bands are probed in accordance with the MAC, or the complete receiver is turned off, thus optimizing power burned during both idle listening and receiving. The same power sequencing techniques can be used for the transmit path.

The second most important parameter to be optimized is the wake-up time. This has been achieved by carefully defining the activation sequence of the different transceiver blocks. It is then mandatory to use proper circuit design techniques in order to minimize the wake-up times of the slower blocks. For RF blocks, this delay is not an issue because of the larger currents as well as the small parasitic capacitances required to achieve RF performance, that will allow very quick settling. Optimization of the setup delay is worth investigating for IF (IF amplification, IF to baseband mixers) and baseband blocks, because significant energy can be gained. A clear advantage of deep-submicron CMOS is that operation within the order of 100-MHz is feasible with proper biasing of the transistors in the signal path in weak or moderate inversion regions. The chosen high-IF architecture allows the IF blocks to be operated at frequencies where setup time is easy to minimize, without degrading the power consumption. Concerning baseband blocks, there is an obvious limitation due to the low-frequency poles inherent to these blocks. Nonetheless, the settling times have been reduced with techniques such as storing the bias points between channel sampling, or by boosting the startup-currents momentarily at wake-up, or else by switching the internal poles to higher frequencies for fast settling, then setting them back to the nominal frequency.

The third key parameters are the receive-to-transmit and transmit-to-receive switching times. During these turnaround delays, all the blocks that remain ”on” will burn power that is not useful for the communication. The architecture of the WiseNET SoC has thus been thought with respect to this particular MAC need. As an example, the same synthesizer and the same LO signals are used for both the receive and the transmit paths. This is made possible because the receiver and the transmitter are implemented according to the same high-IF super-heterodyne architecture. In this way, the synthesizer remains ”on” and is working around the same operating points, yielding fast turnaround times.

A microphotograph of the complete WiseNET SoC is shown in Fig. 3 and some results measured on the transceiver are presented in Table 1 [6].

Parameter	XE1203	WiseNET
Rx wake-up time	1.14 ms	1.7 ms
Rx→Tx/Tx→Rx times	0.5/0.5 ms	0.1/0.1 ms
Idle power cons.	5 μW	2 μW
Rx power cons.	45 mW	2.1 mW
Tx power cons.	124 mW	32.3 mW

Table 2. Simulation radio parameters.

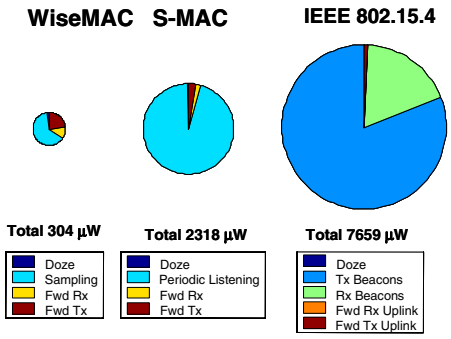

Figure 4. Comparison of WiseMAC performances for the XE1203 radio.

5. Theoretical and Experimental Results

To assess its performances, WiseNET has first been compared to a few existing solutions. To distinguish between the impact of the SoC and the results of the WiseMAC protocol, the comparison has been done in two steps. In a first step, WiseMAC has been compared theoretically with two other protocols, namely the IEEE 802.15.4 protocol used in Zigbee and the well know S-MAC WSN protocol [11]. The simulations have been carried out using the radio parameters shown in Table 2 corresponding to the off-the-shelf XE 1203 transceiver manufactured by Semtech (formerly Xemics) [12]. The average power consumption of a node receiving a 32-byte data packet every 30 seconds and forwarding it to the next node in a multihop network has been calculated. It is assumed that routing is fixed and that no energy is spent in the routing protocol. For S-MAC, we assume a 10% duty cycle. For IEEE 802.15.4, the node is a ZigBee router and thus that node is coordinator of a beacon enabled PAN and is also associated to its parent PAN. The 250-ms wake-up interval is identical for all three protocols.

The results are illustrated in Fig. 4. They show that all protocols use little energy to actually receive the message and forward it. However, S-MAC spends most of its energy in idle listening and overhearing, whereas IEEE 802.15.4

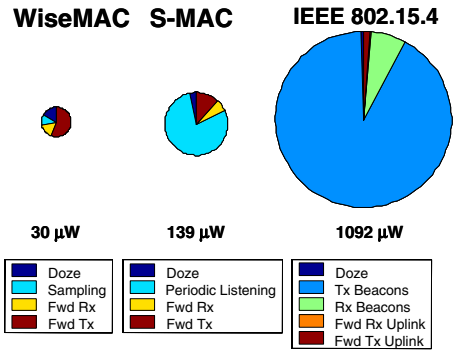

Figure 5. Comparison of WiseMAC performances for the WiseNET SoC radio.

exhibits a large overhead due to the combination of the periodic emission of the beacon, the necessity to listen for potential slave emissions and to listen its parent beacon. WiseMAC incurs little overhead because the time necessary to sense the medium is very small. As a result, WiseMAC is about 7 times more efficient than S-MAC and 25 times more efficient than IEEE 802.15.4.

The same simulations have been performed using the parameters of the WiseNET SoC given in Table 2. Because IEEE 802.15.4 spends more time emitting than the other protocols, the consumption ratio degrades. On the other hand, S-MAC that spends most of its overhead listening is favorably impacted by the SoC low receiving energy. WiseMAC is also favorably impacted but to a lesser extent. As a result, WiseMAC uses about 36 times less energy than IEEE 802.15.4 and only a little less than 5 times less energy than S-MAC.

In order to validate the simulation results, an experimental network of 14 nodes has been setup. Each node is built around the XE1203 transceiver operating at 868 MHz with a XE88LC06A CoolRISC micro-controller (actually the same than the one used in the SoC). The measurements over an extended period of time have shown an average power consumption of around 400-μW for nodes that forward packets. This is slightly above the simulation results. The discrepancy is due to processor energy consumption and also to retries in case of transmission error due to bad channel conditions (collisions were included in the simulations). The use of the WiseNET SoC transceiver should reduce this average power consumption by at least one order of magnitude.

6. Conclusions

Reaching years of autonomy was the objective of the WiseNET project. Impressive energy savings have been reached: 250 times lower than a conventional implementation using off-the-shelf low-power components if we consider IEEE 802.14.5 as a reference, 75 times when compared to S-MAC. This was achieved by a combined optimization of the integrated transceiver hardware and the dedicated medium access control protocol. Additionally, the SoC includes all the basic functions such as data acquisition, processing, storage and communication, that are required by a sensor node and can be powered on low cost alkaline batteries. With an average power consumption of 30-μW to forward a 32 byte data packet every 30 seconds with an average of 125-ms delay per hop, the lifetime is limited by the battery lifetime (around 7 years).

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