On Test Conditions for the Detection of Open Defects

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Abstract

The impact of test conditions on the detectability of open defects is investigated. We performed an inductive fault analysis on representative standard gates. The simulation results show that open-like defects result in a wide range of different voltage-delay dependencies, ranging from a strongly increasing to a strongly decreasing delay as a function of voltage. The behaviour is not only determined by the defect location but also by the test pattern. Knowing the expected behaviour of a certain defect location helps failure localisation. The detectability of a defect is strongly determined by the behaviour of the affected path as well as that of the longest path. Our simulations and measurements show that in general elevated supply voltages give a better detectability of open-like defects.

1 Introduction

An open defect typically causes an additional delay in a transition. To detect these defects requires an 'at-speed' test such as delay-fault/transition-fault testing. Although delay-fault testing is now a mainstream test technique [1]-[5] the optimal set of test conditions are not clear yet. For example on the one hand, Gilles *et al.* [4] are suggesting that delay-fault testing should be done at a supply voltage below nominal. On the other hand, Kruseman *et al.* [6] suggest that a supply voltage above nominal is better.

The purpose of this paper is to obtain a better understanding of the impact of test conditions on delay-fault testing in general and for the class of non-speed-binned ICs in special. For this class the main purpose of delay-fault testing is to catch manufacturing defects. These defects have in general a point-like origin, e.g. salicidation issues [7] or incomplete filled vias [8], and cause an increase in resistance which affects the propagation time of a transition. To analyse the impact we performed an inductive fault analysis (IFA) [9] on a set of representative gates. The defect simulations enable us to construct Shmoo plots and to determine the optimal test conditions. Moreover, we show that the actual behaviour not only depends on the defect location but also on the test patterns which are applied to detect the defect. This knowledge helps to improve physical failure localisation.

The remainder of this paper is organised as follows. Section 2 gives an overview of the three test conditions, speed, supply voltage and temperature. In Section 3 the impact of open defects is investigated and the paper is concluded in Section 4.

2 Test conditions

2.1 Speed

The main target of delay-fault testing is to catch defects that create an additional delay and thereby cause a malfunction of the IC. It is clear that at least the specification speed should be met. The class of non-speed-binned chips, however, is designed in such a way that this speed is met for the worst process and working conditions. Hence, performing the delay-fault test at the specification speed and at the nominal supply voltage, severely underestimates the capabilities of the silicon. This has the risk of missing gross delay-faults which can be detected. Although one could argue that these ICs could still work in an application it is clear that they do pose a reliability risk. Moreover, we have the risk that the defect is activated along a longer path in the application and therefore causes a malfunction. One way to cope with this is to use adaptive delay-fault testing [3]. Instead of having a fixed limit for all chips, one first determines the capabilities of the silicon, e.g. by measuring a ring-oscillator, and based on this set the test limit. This method ensures that all defects that cause a total delay which is longer than the longest path are detectable. More subtle delays require more advanced test methods, such as fine delay-fault testing [3].

2.2 Supply voltage

The second test condition one can influence is the supply voltage. For the detection of shorts it is well known that reducing the supply voltage during testing improves the detectability of defects which are missed at the nominal supply voltage [6][10]. In Section 3 we will show that this is not necessarily true for opens. Some opens have a larger impact at elevated supply voltages

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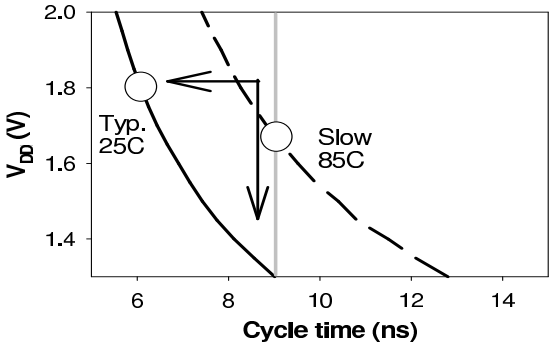

Figure 1 Capabilities of a 180 nm design (nominal supply voltage 1.8 V) for typical and worst case conditions.

while others have a larger impact at reduced supply voltages.

A reduced supply voltage can also be used as another method to cope with the fact that the speed of an IC can be well above the specification speed. Instead of testing at a higher speed at the nominal supply voltage, as was proposed in Section 2.1, one uses the specification speed but reduce the supply voltage below the minimum specification. Figure 1 shows the relation between these two approaches. The black drawn line denotes the pass/fail boundary of an IC with typical processing as a function of supply voltage at 25°C. These pass/fail boundaries are an abstracted version of a Shmoo plot. In a Shmoo plot this line would divide the failing lower left-hand side from the passing upper right-hand side. We will use these pass/fail boundaries instead of Shmoo plots because it allows one to show multiple Shmoo plots (either based on simulations or on measurements) in one figure. For typical manufacturing conditions the IC in Figure 1 can run at 6 ns but the specification speed of this 'right by design' IC is determined by the worst case processing conditions at the minimal supply voltage. The pass/fail boundary for these conditions (slow processing and 85°C) are marked with the dashed line. The speed for these conditions at 1.65 V is the specification speed which is only 9 ns. At typical conditions this design can run much faster than the specification speed. Hence, only testing it at the application speed means that delay-faults of 3 ns are missed. We can improve the detectability of delay faults by either run the test faster (horizontal arrow) or apply the test at a reduced supply voltage (vertical arrow). A practical reason why this second option could be preferred is that the slower test speed reduces the requirements on the test system.

2.3 Temperature

The third condition one can control is the test temperature. Cold testing improves the detectability for opens because it makes defect-free silicon faster (0.1-0.2%/K) while defective paths in general become slower. Usually

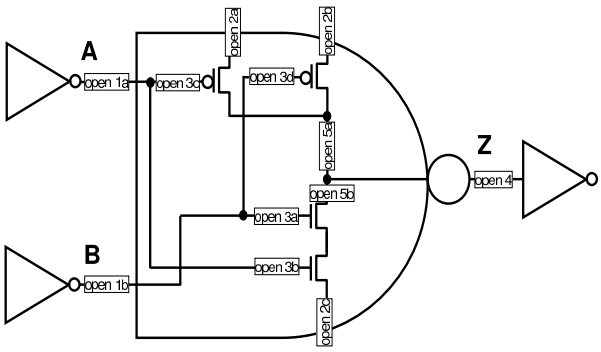

Figure 2 Investigated open defects for a NAND gate.

this increase in delay of the affected path is only due to an increase of the resistance of the open itself (typically 0.4%/K for opens in metal). Sometimes a stronger temperature dependency is observed. This can be explained by a change in the contact resistance caused by thermal contractions.

To include the effect of the temperature in our simulations would require us to make certain assumptions about the root cause of the defect. While we can make these assumptions it basically translates in a temperature dependency of the resistance. This translates in a scaling factor and does not have a strong effect on the shape of the Shmoo plots for supply voltage above $2V_T$. Therefore, the temperature impact is considered as just a modification of resistance and not further covered in our present investigations.

3 Simulations for opens

3.1 Introduction

The impact of specific defect locations is investigated with spice-like simulations. In these simulations extracted versions of standard gates are used that include parasitic components. All input and output signals are fed through inverters to mimic realistic signal behaviour. We will compare the simulation results with experimental results for designs made in a 0.18 µm technology. Therefore the same technology is used in the presented simulations. Simulations for 130 nm and 90 nm technologies showed similar characteristics.

We show results of a NAND gate since this gate covers issues such as multiple driving transistors and stacked transistors. Analysis of other gates shows similar behaviour for comparable conditions. Figure 2 shows a schematic version with the investigated resistive open defects. These opens represent both intra-gate as well as inter-gate opens. The not investigated opens are physically unlikely to occur on silicon. In the simulations the NAND gate is tested with the six patterns that result in a transition (see Table 1).

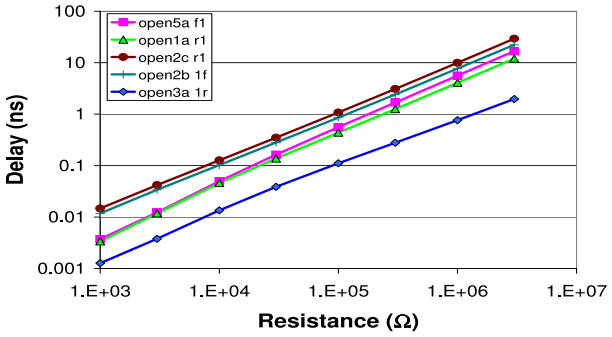

Figure 3 Additional delay as a function of resistance for a selection of defect locations and test patterns.

The opens are simulated as a resistor. This is a simplification of the actual defect impact. The defect itself could/should include capacitive and inductive components. However, simulations showed that the impact of these other components is typically small for realistic values. Hence, limiting ourselves to a resistive component is in general sufficient to get realistic defect behaviour.

Code	A	B	Z - NAND
1r	static 1	rising	falling
r1	rising	static 1	falling
rr	rising	rising	falling
1f	static 1	falling	rising
f1	falling	static 1	rising
ff	falling	falling	rising

Table 1 Applied test patterns for the NAND gate

3.2 Typical resistance of an open

We calculated the additional delay as a function of voltage for all defect locations for resistances between 1 kΩ and 3 MΩ. A selection is plotted on a log-log scale in Figure 3. The delay scales roughly linearly with the defect's resistance over a long interval for most of the locations. The actual delay due to a certain resistance depends on the drive strength of the involved transistors and the load of the affected nodes. Hence, the delay strongly depends on the location of the defect and can easily vary with a factor of 10.

From Figure 3 we can determine the minimum resistance of an open we can expect to detect. An open of a few kΩ gives an additional delay in the order of a gate delay. In non-speed binned chips with typical logic depths of 30-70 gates this delay is simply too small to be detectable, even if this delay would occur in the longest path. Moreover, designs with these deep logical paths typically have a wide distribution in path lengths. In [3] more than half of the tested paths had a delay of less than a third of the delay of the longest path. Hence, a defect becomes in general only detectable if the additional delay due to the defect becomes of the same order as the delay of the longest path. For designs that run at a few hundred MHz we can only expect to detect defects with a resistance of 100 kΩ or more. Montanes *et al.* [11] showed that these (and much larger as well as smaller) resistances commonly occur for open defects.

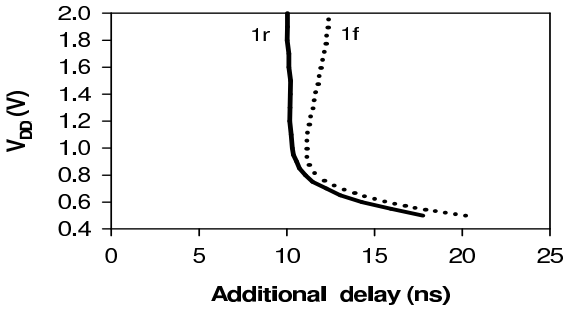

Figure 4 Additional delay due to a 3MΩ resistive open at location open1b for pattern 1r (black line) and 1f (dotted line).

One could improve the detectability by using dedicated ATPG tools that always target the longest path. Nevertheless, one still has the problem that even the longest path through a gate can be a lot shorter that the longest path on a chip. While a defect in such a short path will not cause a direct malfunction it is still a reliability risk, since resistance values of 100 kΩ require almost complete open vias or broken lines.

3.3 Open1

Not completely filled vias are one of the main root causes for 'open' defects. Location *open1* represents, among others, this class of defects. A defect at this location will affect rising as well as falling transitions. By performing a series of simulations at different supply voltages and using different resistances we determined the additional delay for each of the patterns in Table 1. An example of these results is shown in Figure 4 for a 3 MΩ resistance. An interesting aspect is that the behaviour for rising and falling transitions is different. The additional delay for the 1f-pattern shows first a decrease in delay from 2.0 V to 0.8 V and then again an increase, while the 1r-pattern has an almost constant additional delay between 2.0 V to 0.8 V. A break in an input of a gate in general shows this behaviour. Both rising and falling transitions have a bump like feature close to $V_{DD}/2$ owing to the switching of the receiving gates. Differences in the response of the receiving n and p transistors and the exact voltage at which this bumps occur result in the difference in voltage dependency. The exact behaviour depends on the design of the standard gate libraries but it is expected to occur in most general-purpose libraries for modern technologies.

Based on Figure 4 the impression could be that one

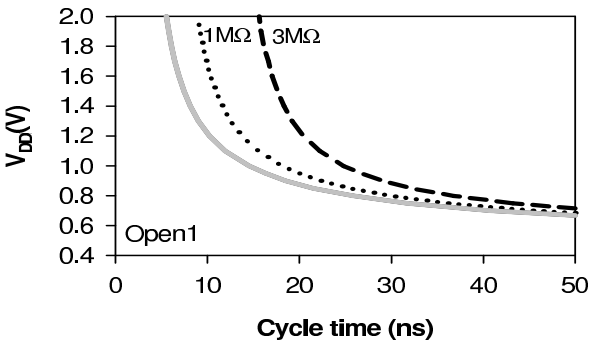

Figure 5 Pass/fail boundary (Shmoo plot) for defect-free silicon (grey line) and with a 1 MΩ (dotted line) and 3 MΩ (dashed line) resistor at location open1b.

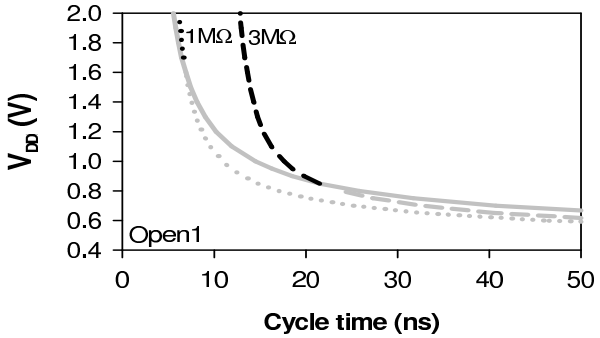

Figure 6 Pass/fail boundary for defect-free silicon (grey line) and with a 1 MΩ (dotted line) and 3 MΩ (dashed line) open1 defect in a intermediate length path.

either should use supply voltages above nominal, e.g. 2.0 V, or well below nominal, e.g. 0.7 V, since for these conditions the additional delay is larger than the delay at the nominal supply voltage. However, to really determine the impact on the detectability of the defect we should include the behaviour of the affected path as well as that of the longest path. Let us first assume that the defect occurs in the longest path itself and is tested with pattern *1r*. The pass/fail boundary for the defect-free longest path is given by the grey line in Figure 5 (identical to the one in Figure 1) and follows a typical transistor delay curve which is well known from Shmoo plots [12]. The dotted and dashed lines in Figure 5 mark the behaviour of this path with open defects. Despite the fact that the absolute impact of the defect is larger below 0.7 V, the relative impact is less. Hence, in practice it becomes harder to distinguish defective from defect-free behaviour. Moreover, one has to use larger safety margins at these low voltages to handle process variation, which reduces the detectability even more.

In reality the chance is small that the defect occurs in the longest path. More common would be a defect in a shorter path. Therefore, a more realistic case is that during test the defect is activated in a path with only half the

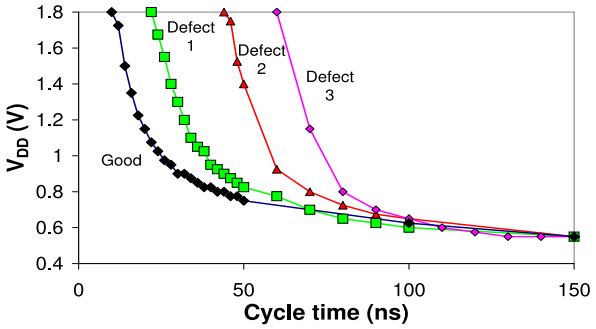

Figure 7 Experimental pass/fail boundaries derived from Shmoo plots. The diamond symbols are for a defect-free devices while the other three curves are for devices with a delay defect.

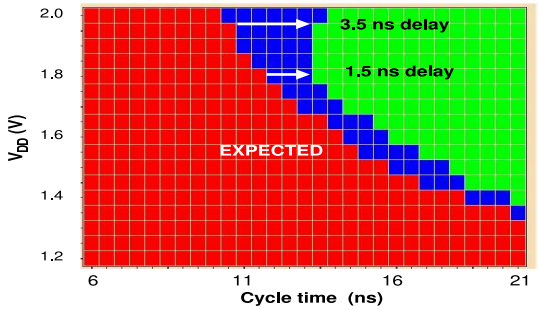

Figure 8 Example of a delay fault with an increased impact at elevated supply voltages.

delay of the longest path. If we simulate the impact of the same 1 MΩ and 3 MΩ resistances in this shorter path we obtain the results shown in Figure 6. The grey line shows the behaviour of the longest path (identical to Figure 5), while the dashed and dotted black lines are the new curves for the 1MΩ and 3MΩ defect. At reduced supply voltages the defect becomes undetectable since the total delay is less than that of the longest path. Hence, testing at a strongly reduced voltage is only effective for defect types for which the delay due to the defect increases faster at reduced supply voltages than the transistor delay. Defects at location *open1* do not show this super-transistor delay behaviour and therefore the best conditions to detect these defects are at elevated supply voltages.

The behaviour as shown in Figure 6, i.e. the delays are detectable at elevated supply voltages and undetectable at reduced supply voltages, is also the most common behaviour we observe on silicon. Some of these experimental results for a 0.18 µm 60k gate design [6] are shown in Figure 7. These measurements show the same behaviour as what is expected based on Figure 6.

Figure 8 shows an example for a 0.18 µm 1 cm^2 design in which the actual additional delay is the largest at elevated supply voltages. This chip fails in an application although it would pass a delay-fault test based on the specification speed. If we use adaptive delay-fault testing

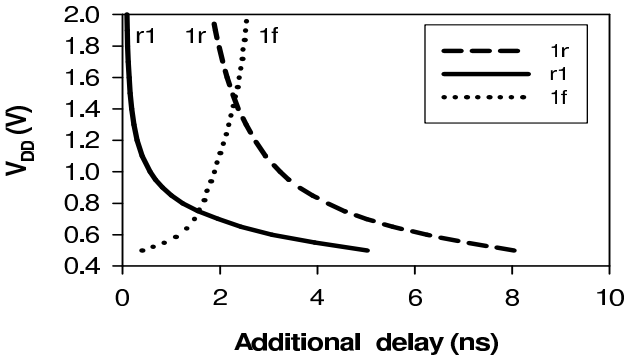

Figure 9 Additional delay for patterns 1r, r1,and 1f for a 3 MΩ open at open3a.

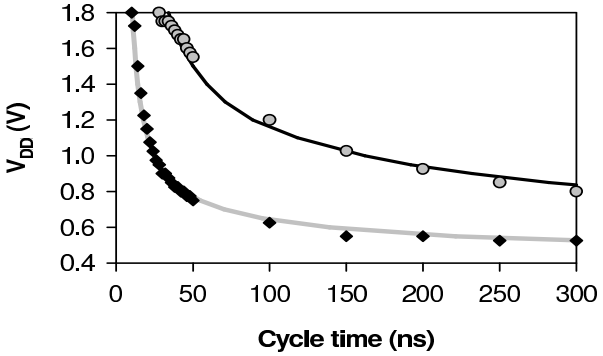

Figure 10 Experimental (symbols) and simulation (lines) results for a defect-free IC and one with a defect with a super transistor-delay behaviour (see also text).

and compare the speed with the expected speed it would be a marginal detect at 1.8 V; depending on the amount of margin it fails (10%) or passes (20%). At 2.0 V, however, the 30% additional delay is sufficient to detect it.

3.4 Open3

The *open3* defect locations represent a partial break in the poly of a transistor, e.g. owing to a salicidation issue [7]. Figure 9 shows the additional delay for *open3a* for three test patterns. The impact of the defect is very different for these patterns, this has the following implications:

First, for fault localisation it is important to use the 'right' test conditions. Fault localisation requires a fail vector log. Depending on the test conditions this log has either information for the *1r* pattern or the *1f* pattern or both of them. This can affect fault localisation.

Second, it makes classification of defects based only on Shmoo plots tricky: we now have one defect location for which we have quite diverse Shmoo plots depending on the test pattern.

Third, pattern *r1* shows a case for which a reduction in supply voltage always enhances the detectability of the delay. The *r1* pattern has almost no impact at the nominal supply voltage but shows a very strong increase in delay

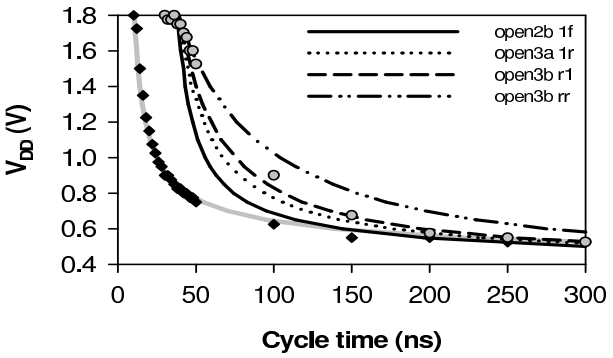

Figure 11 Experimental (symbols) and simulation (lines) results for a defect-free IC and one with a defect with a sub transistor delay behaviour.

when reducing the supply voltage. The additional delay increases faster than the transistor delay and therefore enhances the detectability at (very) low supply voltages. For a NAND-gate this situation is only relevant if the *1r* and *1f* cannot be applied since these patterns will otherwise dominate the delay. Moreover, it is the only case of this behaviour for a NAND-gate. Nevertheless, it does indicate that some open-like defects can be better detectable at reduced supply voltage.

We have indeed observed a few cases that match this behaviour and an example is shown in Figure 10. The diamond symbols represent the measured pass/fail boundary of a good device (same as Figure 7). The grey line represents simulation results for a good device and is a scaled version of the defect-free curve in Figure 5. This simulation matches the experimental results reasonably well. The grey circles are experimental results of a delay-fault which shows an increase for reduced supply voltages. The black line denotes the simulated impact of an *open3a* defect which is only tested with pattern *r1*. The match is not perfect but we do see similar behaviour.

3.5 Remaining faults

In previous paragraphs we highlighted the impact of opens at two defect locations because they cover most of the main classes of behaviour. The remaining behaviours are covered in Table 2. 'identical' indicates that the impact is the same (which is typically the case for equivalent defect locations), while 'similar' indicates that some differences exist but that the general behaviour is the same, e.g. they have only 0.7× the delay at the nominal supply voltage. For the shape several classifications are used: 'constant' indicates an almost constant delay between 1.0 and 2.0V such as shown in Figure 4 for pattern *1r*, 'constant inv.' means a decrease in delay for reduced V_{DD}, see Figure 4 pattern *1f*, 'increasing' means an increasing delay for reduced V_{DD}. Two special cases are the extreme increase for *open3a* with pattern *r1* and a 'bump' in the additional delay for *open3c*, which is not discussed in the

present paper.

What we can conclude from Table 2 is that similar behaviour can be observed for a lot of different defect locations. The 'constant' delay of a broken interconnect is also encountered in all classes of intra-gate defects. Therefore, the difference some authors make between inter-gate and intra-gate is artificial. Nevertheless, Shmoo plots can provide valuable insight and exclude certain defect locations. For example, the behaviour as shown in Figure 4 can distinguish falling and rising transitions, which can improve the fault localisation. Also comparing simulated behaviours with the actual behaviour can help to enhance or reduce the confidence in specific defect locations. For example, in Figure 11 the grey symbols show the measured response while the black lines denote simulations for some defect locations. The best match is obtained for *open3b* in combination with pattern *r1*. If the same pattern should emerge from the fault localisation then the confidence is greatly enhanced. Although these comparisons will not work in general they can certainly help in specific cases.

defect			**identical**	**similar**	**shape**
open1a	r1	f	open1b 1r		constant
	f1	r	open1b 1f		constant inv
open2a	f1	r	open2b 1f		increasing
open2c	r1	f			constant
	1r	f		0.7×open2c r1	constant
open3a	r1	f			ext. increasing
	1f	r			constant inv.
	1r	f			increasing
open3b	f1	r			constant inv.
	r1	f			increasing
	rr	f		0.5×open3b r1	increasing
open3c	f1	r	open3d 1f	open3a 1r	increasing
	r1	f	open3d 1r		bump midV
open4	1r	f	open4 r1 rr	open1a f1	constant inv.
	1f	r	open4 f1 ff	open1a r1	constant
open5a	1r	f			constant inv.
	r1	f		open5a 1r	constant inv.
open5b	1f	r		0.7×open5b f1	constant
	f1	r			constant
	ff	r		0.7×open5b f1	constant

Table 2 Characteristics of open defects.

4 Conclusions

According to our simulations as well as our experimental observations open-like defects are in general better detectable at elevated supply voltages than at reduced supply voltages. For the analysis of the detectability it is important to include the behaviour of the affected path as well as the longest path. Although often the additional delay does increase at low supply voltages it rarely increases faster than the transistor delay. Hence, the detectability is reduced instead of improved. Therefore, delay-fault testing is more effective at elevated supply voltages.

Furthermore, we observed a wide range of different voltage-delay dependencies, ranging from a strongly increasing to a strongly decreasing delay as a function of voltage. The behaviour depends not only on the defect location but also on the applied pattern. Our experimental results show that these simulated behaviours indeed occur on silicon. Using this knowledge improves failure localisation.

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