

# **Embedded Tutorial: 4G Applications, Architectures, Design Methodology and Tools for MPSoC**

## **1 Motivation**

The telecommunications and semiconductor industry are inseparably linked. More than sixty percent of the revenue of the semiconductor industry is attributed to communications and multimedia applications. On the other hand wireless communications (and multimedia) applications demand ultrahigh computational performance and therefore have become technology drivers for the semiconductor industry. The single most important aspect of designing and, successfully deploying 4G, is its cross-disciplinary character, ranging from semiconductors to services to deployment to business.

## **2 Who should attend?**

In this tutorial the various issues involved in defining, designing, and deploying 4G are addressed and their interdependency are discussed. Particular attention will be paid to the system level design of complex SoC's.

The tutorial should be primarily of interest to engineers involved in the design of products and to managers responsible for product development or marketing.

## **3 Table of content**

### **3.1 *Facts and Trends***

We discuss the growth law of the semiconductor and telecommunication industry and observe that we can no longer assume that the exponentially increasing number of transistors (Moore's law) leads to a corresponding increase in computing performance. In order to economically use the transistors the design of the SoC needs to be moved to a higher level of abstraction. We need to think in processors and interconnects rather than gates and wires. We discuss the need for a system level design methodology and the corresponding design environment and outline the properties of the new system level design paradigm

### **3.2 *Future Telecommunication Systems***

We discuss the architecture of 4G and potential applications. We introduce the concepts of software defined and cognitive radio.

### **3.3 *MPSoC for wireless applications***

We argue that future system-on-chips (SoCs) will be viewed as heterogeneous multiprocessor systems (MPSoC). They will contain an increasing number of application specific instruction-set processors (ASIPs) combined with complex memory hierarchies and on-chip communication networks. These heterogeneous architectures promise enormous

potential to jointly optimize flexibility and area/energy-efficiency. We discuss the fundamental trade-off between flexibility and energy efficiency and demonstrate how the tasks of a digital receiver can be naturally mapped onto a heterogeneous MPSoC.

### ***3.4 Design Methodology and system level tools***

We discuss the need for a proper design methodology and give an overview of existing system level tools.

### ***3.5 Energy efficient digital signal processors: Principles, applications and design of application specific processors***

We first discuss the architectural fundamentals to achieve energy efficiency in digital signal processing. We then discuss application and design of ASIPs (application specific or synonymously called configurable) processors. We give an overview of the various concepts, the pros and cons of commercial solutions. We show that the design of an ASIP is a cross-disciplinary task involving disciplines ranging from algorithm all the way to hardware design. Lessons learned from state-of-the art designs shows that this cross-disciplinary approach is a very challenging, but highly efficient endeavour.

### ***3.6 Interconnect: From busses to network-on-chip***

An SoC comprises of two basic elements: the processing elements and their interconnect. Traditional bus structures do not scale with the rapidly increasing number of processing elements. We give an overview of the emerging concept of network-on-chip.

### ***3.7 The business equation***

Last, but not least, we address a number of economical issues. For example, what are the implications for the industry if the shrinking of the physical dimensions, contrary to the past, contributes only a small portion to the performance gain of future SoCs? If performance gain will be the result of an multi-disciplinary, integrated approach involving application how is such a business process managed?