Performance Optimization for Energy-Aware Adaptive Checkpointing in Embedded Real-Time Systems^{*}

Zhongwen Li, Information Science and Technology College, Xiamen University, China <u>lizw@xmu.edu.cn</u> Hong Chen, Information Science and Technology College, Xiamen University, China <u>chenhon103@hotmail.com</u> Shui Yu School of Information Technology, Deakin University, Australia <u>syu@deakin.edu.au</u>

Abstract

Using additional store-checkpoinsts (SCPs) and compare-checkpoints (CCPs), we present an adaptive checkpointing for double modular redundancy (DMR) in this paper. The proposed approach can dynamically adjust the checkpoint intervals. We also design methods to calculate the optimal numbers of checkpoints, which can minimize the average execution time of tasks. Further, the adaptive checkpointing is combined with the DVS (dynamic voltage scaling) scheme to achieve energy reduction. Simulation results show that, compared with the previous methods, the proposed approach significantly increases the likelihood of timely task completion and reduces energy consumption in the presence of faults.

1. Introduction

Checkpointing is an important method for fault-tolerance in real-time systems in the condition of harsh environment. The following three types of checkpoints are well known: CSCP, SCP and CCP^[1-3]. CCPs are used to compare the states of the processors without storing them, while, the processors store their states without comparison in SCPs. If the two operations are used together in the same checkpoint, we call it CSCP. Using CCP and SCP, Ziv and Bruck have shown numerically that the task execution time is significantly reduced^[1,4]. Using additional CCPs and SCPs, Nakagawa and Fukumoto have used a triple modular redundancy and double modular redundancy to analyze the optimal checkpoint intervals that can minimize a task execution time, respectively^[5].

In addition, many real-time systems are often en-

ergy-constrained since system lifetime is determined to a large extent by the battery lifetime ^[2]. For example, autonomous airborne and sea-borne systems working on limited battery supply, space systems working on a limited combination of solar and battery power supply, time-sensitive systems deployed in remote locations where a steady power supply is not available ^[3,6]. DVS has emerged as a popular solution to the problem of reducing power consumption during system operations. The DVS become possible on the availability of embedded processors that can dynamically scale the frequency by adjusting the operation voltage ^[2,3]. Many embedded processors have the ability to dynamically scale the operation voltage currently. Such as, the mobile processors from Intel with its SpeedStep^[7] technology. In the realm of real-time systems, the DVS techniques focuse on minimizing energy consumption of the system under the condition of meeting the deadlines. The DVS and fault tolerance for real-time systems have been studied as separate problems. It is only recently that an attempt has been made to combine fault tolerance with the DVS $^{[3]}$.

The combination of DVS, CSCPs (CCPs or SCPs) can be used to satisfy system's DVS requirement and improve the performance of real-time systems. However, none of the mentioned papers addressed these issues in terms of conjunction. Using additional SCPs and CCPs, we modify the methods of [3] in the double modular redundancy (DMR) in this paper. Different from the existing methods, our approach is to tune the scheme to the specific system which it is implemented on, and use both the comparison and storage operations efficiently, the performance of checkpoint schemes is improved.

Some notations used in our paper are listed below:

t_s: the time to store the states of processors.

 t_{cp} : the time to compare processors' states.

 t_r : the time to roll back the processors to a consistent state.

 R_t : remaining execution time.

 R_d : time left before the deadline.

^{*} This work is supported in part of Fujian natural science grant (A0410004), Fujian young science & technology innovation grant (2003J020), NCETXMU 2004 program, Program of 985 Innovation on Information in Xiamen Univ.(2004-2007) and Xiamen Univ. research grant (0630-E23011).

 R_{ϵ} : upper boundary on the remaining number of faults that can be tolerated by the system.

2 Adaptive checkpointing scheme

Assume task τ has a period T, a deadline D, a worst-case computation time N when there are no fault in the system. An upper boundary k represents the number of fault occurrences that have to be tolerated. C is the overhead of a checkpoint. Faults arrive as a Poisson process with parameter λ , the average execution time for the task is minimum, if a constant checkpoint interval of $\sqrt{2C/\lambda}$ is used^[8]. We refer to this as the Poisson-arrival approach. If the Poisson-arrival scheme is used, the effective task execution time in the absence of faults must be less than the deadline D. Assume the fault-free execution time for a task is N, the worst-case execution time for up to k faults is minimum, if the constant checkpoint interval is set to $\sqrt{NC/k}$ ^[9]. This is the k-fault-tolerant approach.

In addition, we assume that task τ is divided equally into *n* intervals of length $T = \left\lceil \frac{N}{n} \right\rceil$, and at the end of each interval, CSCP is always placed.

2.1 Additional SCPs

Each CSCP interval is divided equally into m intervals of length $T_1 = \left[\frac{T}{m}\right]$ (figure 1). The SCPs are placed

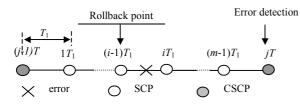


Fig. 1 Task execution with SCPs

between the CSCPs, the states of two processors are stored at iT_1 and jT (i=1,2,...,m-1). If two states do not get an agreement at time jT, then, we need to find the most recent SCP with identical states and roll back to it. As shown in figure 1, two processors are rolled back to $(i-1)T_1$ because some errors have occurred during $((i-1)T_1,$ iT_1), and repeat the execution from $(i-1)T_1$. The average execution time $R_1(m)$ for a CSCP interval ((j-1)T, jT) is given by a renewal-equation^[4, 10]:

$$R_{1}(m) = (mT_{1} + mt_{s} + t_{cp})e^{-2\lambda mT_{1}}$$

+ $\sum_{i=1}^{m} \int_{(i-1)T_{1}}^{iT_{1}} [mT_{1} + mt_{s} + t_{cp} + t_{r} + R_{1}(m - (i-1))]d(1 - e^{-2\lambda t})$
= $mT_{1} + mt_{s} + t_{cp} + [\frac{1}{2}m(m+1)(T_{1} + t_{s}) + m(t_{cp} + t_{r})](e^{2\lambda T_{1}} - 1)$

Therefore, the average execution time of a task $R_{SCP}(n)=nR_1(m).$

Replace $m = T / T_1$, we have

 $R_{1}(T_{1}) = T + \frac{T}{T_{1}}t_{s} + t_{cp} + \left[\left(T + \frac{T}{T_{1}}t_{s}\right)\frac{(T+T_{1})}{2T_{1}} + \frac{T}{T_{1}}t_{cp}\right](e^{2\lambda T_{1}} - 1)\dots(1)$ If $T_1 \to 0^+$, then $R_1(T_1) = +\infty$. Let $T_1 = T$, we have $R_1(T_1) = (T + t_s + t_{cn})e^{2\lambda T}$. Thus, there exists a finite $\widetilde{T}_1 \in ((j-1)T, jT]$ which minimizes $R_1(T_1)$. Differentiating equation (1) with respect to T_1 and setting it equal to zero, we get T_1 . Procedure num_SCP(T) for calculating \tilde{m} which minimize $R_1(\tilde{m})$ is described in Figure 2.

The adaptive checkpointing with SCPs, adapchp-SCP (D,E,C,k,λ) , is described in Figure 3. A check is per-

> Procedure num SCP(T){ Find \widetilde{T}_1 which minimizes $R_1(m)$; 1. 2. if $(\widetilde{T}_1 \leq T)$ { 3. $\mathbf{m} = \left[T / \widetilde{T}_1 \right];$ 4. if $(R_1(m) \leq R_1(m+1))$ then 5. $\widetilde{m} = m;$ else $\widetilde{m} = m + 1$; 6. 7. } else $\widetilde{m} = 1$; 8. return \widetilde{m} ; }

Fig. 2 Procedure for calculating the \tilde{m}

```
Procedure adapchp-SCP (D, N, C, k, \lambda)
```

- 1. $R_t = N; R_d = D; R_f = k;$
- 2.
- $Itv=interval(R_d, R_b, C, R_f, \lambda);$ m=num_SCP(Itv); itv=[Itv/m];3.
- 4. while $(R_t > 0)$ do {
- 5. if $(R_t > R_d)$ break with task failure;
- 6. Insert SCP with interval length *itv*;
- 7. Insert CSCP with interval length Itv;
- 8. Update R_t, R_d ;
- 9. if (no error has been detected at CSCP)
- 10. Resume execution;
- 11. else{
- 12. Rollback to the most recent SCP with identical states:
- 13. $R_f = R_f - 1;$
- $Itv = interval(R_d, R_t, C, R_f, \lambda);$ 14.
- $m = \text{num}_SCP(Itv); itv = [Itv/m];$ 15.
- 16. Resume execution;}}

Fig. 3 Adaptive checkpointing with SCPs

formed to see if the task has been completed in line 4, and line 5 checks for the deadline constraint. The length of SCP and CSCP interval is set in line 6 and line 7, respectively. In line 9, a check is performed to see if fault is detected. If there is no fault, then continue to run task, otherwise, roll back to previous SCP with identical states and continues execution, which are described from line 12 to

line 16. In line 2 and 14, we use procedure interval $(R_d, R_t, C, R_{f, \lambda})^{[3]}$ (figure 4) to calculate the checkpoint interval.

In figure 4, $I_1(C,\lambda) = \sqrt{2C/\lambda}$ is the checkpoint interval of the Poisson-arrival approach.

Procedure interval(R_d , R_t , C, R_f , λ) .exp error= λR_t ; 1 2. if $(exp \ error \leq R_f)$ { 3. if $(R_t > Th_{\lambda}(R_d, \lambda, C))$ then 4. chk interval= $I_3(R_t, R_d, C)$; 5. else if $(R_t > Th(R_d, R_f, C))$ then 6. $chk_interval = I_2(R_t, exp_error, C);$ 7. else $chk_interval = I_2(R_t, R_f, C);$ else{ if $(R_t > Th_{\lambda}(R_d, \lambda, C))$ then 8. 9. $chk_interval=I_3(R_t, R_d, C);$ 10. else *chk_interval=I*₁(C, λ);} 11 return *chk* interval; }

Fig. 4 Calculating checkpointing interval

 $I_2(N,k,C) = \sqrt{NC/k}$ is the checkpoint interval of the k-fault-tolerant approach. In addition, [3] defined some quations:

$$Th_{\lambda}(R_{d}, \lambda, C) = (R_{d} + C)/(1 + \sqrt{\lambda C/2})$$

$$Th(R_{d}, R_{f}, C) = R_{d} + C + 2R_{f}C - 2\sqrt{R_{f}C(R_{d} + C) + (R_{f}C)^{2}}$$

$$I_{3}(N, D, C) = 2NC/(D + C - N)$$

Line 1 of figure 4 calculates the number of faults *Exp-fault* that are expected to occur in the remaining time R_t . If *Exp-fault* is less than or equal to R_f , the *k*-fault-tolerant requirement is deemed to be more stringent than the Poisson-arrival criterion. In line 3, a check is performed to see if R_t exceeds the threshold $Th_{\lambda}(R_d, \lambda, C)$. If this condition is satisfied, the checkpoint interval is set to $I_3(R_t, R_d, C)$. In line5, a check is performed to see if R_t exceeds threshold $Th(R_d, R_f, C)$ but is below $Th_{\lambda}(R_d, \lambda, C)$. If this condition is satisfied, the checkpoint is set to $I_2(R_t, Exp-fault, C)$. If the *k*-fault-tolerant threshold is met, the checkpoint interval is set to $I_2(R_t, Exp-fault, C)$. If the *k*-fault-tolerant threshold is met, the checkpoint interval is set to $I_2(R_t, R_f, C)$ in line 7. Line 8-10 handle the case when the *k*-fault-tolerant requirement is deemed to be less stringent than the Poisson-arrival criterion.

2.2 Additional CCPs

Each CSCP interval is divided equally into *m* intervals of length $T_2 = \left[\frac{T}{m}\right]$. The CCPs are placed between CSCPs, and the states of the two processors are compared at *iT*₂ and *jT* (*i*=1,2,..., *m*-1). If two states do not reach to an agreement at *iT*₂ and *jT*, that means some errors have occurred during this interval, the two processors will be rolled back to (*j*-1)*T* (Figure 5).

The average execution time $R_2(m)$ for an interval

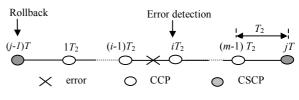
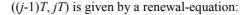


Fig. 5 Task execution with ICCPs



$$R_{2}(m) = (mT_{2} + mt_{cp} + t_{s})e^{-2\lambda mT_{2}}$$

+
$$\sum_{i=1}^{m} \int_{(i-1)T_{2}}^{iT_{2}} [iT_{2} + it_{cp} + t_{r} + R_{2}(m)]d(1 - e^{-2\lambda t})$$

+
$$\int_{(m-1)T_{2}}^{mT_{2}} t_{s}d(1 - e^{-2\lambda t})$$

=
$$t_{s}e^{2\lambda T_{2}} + (e^{2\lambda mT_{2}} - 1)\frac{T_{2} + t_{cp}}{1 - e^{2\lambda T_{2}}}$$

Therefore, the average execution time $R_{CCP}(n)=nR_2(m)$.

Replacing $m = T / T_2$, we have:

 $\begin{aligned} R_2(T_2) &= t_s e^{2\lambda_0 T_2} + (e^{2\lambda_0 T} - 1) \frac{T_2 + t_{cp}}{1 - e^{-2\lambda_0 T_2}} \dots (2) \\ \text{If } T_2 &\to 0^+ \text{, then } R_2(T_2) = +\infty \text{. If } T_2 = T, \\ \text{then } R_2(T_2) &= (T + t_s + t_{cp}) e^{2\lambda T} \text{. Therefore, there exists a} \\ \text{finite } \widetilde{T}_2 &\in ((j-1)T, jT], \text{ which minimizes } R_2(T_2). \text{ Differentiating equation (2) with respect to } T_2 \text{ and setting it to zero,} \\ \text{we can get } \widetilde{T}_2 \text{. We can use the similar approach described in figure 2 to calculate } \widetilde{m} \text{ which minimize } R_2(\widetilde{m}) . \end{aligned}$

3 Adaptive checkpointing with DVS

With additional SCPs and CCPs, we show how adaptive checkpointing scheme can be combined with the DVS to obtain fault tolerance and power savings in real-time systems. In the one hand, our approach is to maximize the probability that the task meets its deadline in the presence of faults. In another hand, our approach is to reduce energy consumption through the DVS.

Assume that task τ has a fixed quantity of computation cycles N in the fault-free condition. Because the variable voltage CPUs are available, the time to execute task τ depends on the processor speed. We therefore characterize τ by a fixed quantity N, namely, its worst-case number of CPU cycles, needed to execute the task at the minimum processor speed. For the rest of this paper, we normalize the units of N such that the minimum processor speed is 1. That is, if the minimum processor speed is S cycles per second, then we express the number of cycles in units of S cycles and thus normalize the minimum processor speed to $S_{min}=1$. Of course, period T and deadline D are expressed in terms of the number of CPU cycles at the minimum processor speed.

To simplify the analysis and to allow for the derivation of analytical formulas, we would like to assume that a single processor with two speeds f_1 and f_2 , and f_1 is the minimum processor speed, namely, $f_1 = S_{min} = 1$. Moreover, the processor can switch its speed in a negligible amount of time.

Additional notations we use is below:

 $R_{\rm c}$: the number of instructions of the task that remain to be executed at the time of the voltage scaling decision.

c: the numbe of clock cycles that a single checkpoint takes.

 t_{est} : an estimate of the time that the task has to execute in the presence of faults and with checkpointing. The expected number of faults for the duration t_{est} is λt_{est} .

The checkpointing cost C at frequency f is given by C=c/f.

To ensure λt_{est} fault tolerance during task execution, the checkpointing interval must be set to $\sqrt{t_{est}C/(\lambda t_{est})} = \sqrt{C/\lambda} = \sqrt{c/(\lambda f)}$. In addition, we have $t_{est} = \frac{R_c (1 + \sqrt{\lambda c / f})}{f (1 - \sqrt{\lambda c / f})}$ ^[3].

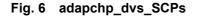
We consider the voltage scaling to be feasible if $t_{est} \le R_d$. This forms the basis of the energy-aware adaptive checkpointing that are described in procedure

adapchp_dvs_SCPs and adapchp_dvs_CCPs (Figure 6 and Figure 7).

Procedure adapchp_dvs_SCP(D, N, c, k, λ){

 $R_{c} = N; R_{d} = D; R_{f} = k;$ 1. 2. if $(t_{est}(R_c, f_1) \le R_d) f = f_1$; else $f = f_2$; 3. It = interval(R_d , R_c/f , c/f, R_f , λ); 4. m = num SCP(Itv); itv = Itv/m;while $(R_t = R_c / f) > 0$) do{ 5. if $(R_t > R_d)$ break with task failure; 6. 7. Insert SCP with interval length itv; Insert CSCP with interval length Itv; 8. 9. Update R_c , R_d according to speed f; if(no error has been detected at CSCP) 10 11. Resume execution; 12. else { Roll back to the most recent SCP/CSCP with identical states; 13. 14. $R_f = R_f - 1;$ if $(t_{est}(R_c, f_1) \le R_d) f = f_1$; else $f = f_2$; 15. $Itv = interval(R_d, R_c / f, c / f, R_f, \lambda);$ 16. 17. m = num SCP(Itv); itv = Itv/m;Resume execution;} 18

}}



Procedure adapchp_dvs_CCP(D, E, C, k, λ){

1.	$R_t = E; R_d = D; R_f = k;$
2.	if($t_{est}(R_c, f_1) \le R_d$) $f = f_1$; else $f = f_2$;
3.	$Itv = interval(R_d, R_c / f, c / f, R_f, \lambda);$

- 4. $m = \text{num}_{CCP}(Itv); itv = Itv/m;$
- 5. while $(R_t = R_c / f) > 0$) do {
- 6. $if(R_t > R_d)$ break with task failure;
- 7. Insert CCP with interval length *itv*;
 - Insert CSCP with interval length Itv;
- 9. Update R_c , R_d according to speed f;

```
10. if(no error has been detected at CCP/CSCP)
```

11. Resume execution;

```
12. else{
```

8.

- 13. Roll back to the last CSCP;
- 14. $R_f = R_f 1;$
- 15. $if(t_{est}(R_c, f_1) \le R_d)f = f_1; else f = f_2;$
- 16. $Itv = interval(R_d, R_c / f, c / f, R_f, \lambda);$
- 17. $m = \text{num}_{CCP}(Itv); itv = Itv/m;$
- 18. Resume execution;}

}}

Fig. 7 adapchp_dvs_CCPs

4 Simulation results

We carried out a set of simulation experiments to checkpointing evaluate our adaptive schemes adapchp dvs CCPs and adapchp dvs SCPs (referred to as A D C and A D S) and to compare it with the Poisson-arrival (referred to as Poisson), the k-fault-tolerant (referred to as k-f-t) checkpointing schemes and ADT_DVS^[3] (referred to as A_D). Faults are injected into system using a Poisson process with various values for the arrival rate λ . Due to the stochastic nature of the fault arrival process, the experiment is repeated 10,000 times for the same task and the results are averaged over these runs. We are interested here in the probability that the task completes on time, and the energy consumption. Energy consumption is measured by summing the product of the square of the voltage and the number of computation cycles over all the segments of the task ^[3]. As in [3], we use the term task utilization U to refer to the ratio N/D. In order to compare with results of ADT DVS scheme, we let $t_r=0$ and $f_2=2f_1$. Moreover, let P and E represent the probability of timely completion of tasks and energy consumption, respectively.

4.1 Additional SCPs

As mentioned previously, additional SCPs scheme fits systems, in which time overhead is determined mainly by the time to compare processor's states. Therefore, the parameters are as following: D=10000, $t_s=2$, $t_{cp}=20$, c=22.

First, we let the Poisson-arrival and the k-fault-tolerant schemes use the lower speed f_1 . The task

utilization *U* in this case is $N/(f_1D)$. Our experimental results are shown in table 1. In table 1(a), for $\lambda > 0.001$ and 0.7 < U < 0.9 (high fault arrival rate and relatively high task utilization), the experimental results show that adapchp-dvs-SCPs scheme clearly outperforms the ADT_DVS scheme. Although Poisson-arrival and the *k*-fault-tolerant schemes have lower energy consumption, their probability of timely completion of the task are lower that 0.2. In table 1(b), for $\lambda < 0.001$ and $0.9 < U \leq 1$ (low fault arrival rate and high task utilization), we draw the similar conclusions described above.

We assume that both Poisson-arrival and the *k*-fault-tolerant schemes use the higher speed f_2 . Then the task utilization *U* in this case is $N/(f_2D)$. Our experimental results are shown in table 2. We also can draw a conclusion that our scheme outperforms the other three schemes.

Tab. 1 The comparison between adapchp-dvs-SCPs and other algorithms, both the Poisson-arrival and the k-fault-tolerant schemes use the lower speed f_i .

		Р				
U	λ	Ε				
	(×10 ⁻²)	Poisson	<i>k</i> -f-t	A_D	A_D_S	
0.76	0.14	0.1185	0.1115	0.9991	0.9999	
		39015	38940	57564	52863	
	0.16	0.0489	0.0466	0.9992	0.9999	
		39183	39153	59765	54176	
0.78	0.14	0.0504	0.0496	0.9990	0.9999	
		39358	39350	60441	55520	
	0.16	0.0181	0.0182	0.9993	0.9999	
		39443	39396	62687	56814	
0.80	0.14	0.0091	0.0204	0.9993	0.9999	
		38951	39507	63039	58079	
	0.16	0.0021	0.0062	0.9990	0.9998	
		39217	39684	65233	59344	
0.82	0.14	0.0013	0.0018	0.9995	1.0000	
		39161	39122	65778	60731	
	0.16	0.0005	0.0003	0.9990	0.9999	
		39290	39200	67987	62091	

k = 5(a) Uλ F A_D *k*-f-t A D S Poisson $(\times 10^{-4})$ 0.92 1.0 0.3914 0.3965 0.9229 0.9549 38032 74193 72862 38665 2.0 0.1650 0.1628 0.9793 0.9985 38623 38681 76444 72566 0.95 1.0 0.3851 0.3852 0.9188 0.9516 39844 75743 39316 77097 2.0 0.1520 0.1510 0.9462 0.9944 39844 39844 80414 76841 1.00 1.0 0.0000 0.0000 0.9146 0.9557 NaN NaN 81572 81047 2.0 0.0000 0.00000.9204 0.9892 NaN NaN 84371 82499

(b) k = 1

Tab. 2	The comparison between
adapchp-dvs-	SCPs and other algorithms, both
the Poisson	-arrival and the k-fault-tolerant
scheme	s use the higher speed f_2 .

		Р				
U	λ	E				
	(10^{-2})	Poisson	<i>k</i> -f-t	A_D	A_D_S	
	$(\times 10^{-2})$					
0.76	0.14	0.6159	0.6121	0.6486	0.9462	
		149458	149682	149599	146097	
	0.16	0.5369	0.4258	0.5451	0.9006	
		151339	150911	151264	147873	
0.78	0.14	0.4659	0.3593	0.4699	0.8385	
		151964	150851	151935	149415	
	0.16	0.3007	0.2055	0.3227	0.7389	
		152371	151581	152552	150742	
0.80	0.14	0.2355	0.2305	0.2672	0.6491	
		152698	152918	153124	151905	
	0.16	0.1264	0.1207	0.1617	0.4864	
		153007	153495	153695	152742	
0.82	0.14	0.0921	0.0838	0.0992	0.3843	
		153077	153103	153320	153562	
	0.16	0.0285	0.0271	0.0388	0.2242	
		153494	153619	154288	154279	
		(a) k	- 5			

(a) k = 5

		() 1	-		
U	λ		-	D E	
	(×10 ⁻⁴)	Poisson	<i>k</i> -f-t	A_D	A_D_S
0.92	1.0	0.7609	0.7638	0.7640	0.7776
		151255	151722	150583	150583
	2.0	0.4365	0.4384	0.4737	0.5334
		152453	152554	152444	152452
0.95	1.0	0.3847	0.3924	0.3799	0.3941
		152589	154140	149117	150259
	2.0	0.1498	0.1498	0.2816	0.2842
		153946	154167	155147	155612
		(b)	k = 1		

4.2 Additional CCPs

Additional CCPs scheme fits systems which overhead time is determined mainly by the time to store processor' states. Therefore, the parameters is as following: D=10000, $t_s=20$, $t_{cp}=2$, c=22.

Tab. 3 The comparison between adapchp-dvs-CCPs and other algorithms, both the Poisson-arrival and the k-fault-tolerant schemes use the lower speed f_1 .

U	х	P E				
	(×10 ⁻²)	Poisson	<i>k</i> -f-t	A_D	A_D_S	
0.76	0.14	0.1104	0.1070	0.9990	1.0000	
		38942	38953	57662	52862	
	0.16	0.0505	0.0479	0.9989	0.9999	
		39141	39128	59736	54036	
0.78	0.14	0.0530	0.0534	0.9989	1.0000	
		39374	39345	60435	55520	
	0.16	0.0190	0.0210	0.9989	0.9998	
		39422	39362	62477	56719	

0.80	0.14	0.0085	0.0209	0.9989	1.0000
		39030	39500	63040	58042
	0.16	0.0022	0.0057	0.9992	1.0000
		39103	39530	65230	59274
0.82	0.14	0.0021	0.0020	0.9990	1.0000
		39266	39031	65731	60573
	0.16	0.0005	0.0005	0.9989	1.0000
		39658	39350	68038	61935
		(a)	<i>k</i> = 5		
			1	D	
U	λ		1	Ξ	
		Poisson	<i>k</i> -f-t	A D	A D S
	$(\times 10^{-4})$			_	
0.92	1.0	0.3887	0.3984	0.9241	0.9800
		38032	38667	74350	73547
	2.0	0.1634	0.1635	0.9783	0.9994
		38619	38685	77021	72669
		0.0000	0 0 7 7 7 0	0.011(0.0012
0.95	1.0	0.3775	0.3772	0.9116	0.9812

2.0	0.1498	0.1480	0.9519	0.9978
	39844	39844	80540	76614
1.0	0.0000	0.0000	0.9074	0.9831
	NaN	NaN	81397	81675
2.0	0.0000	0.0000	0.9202	0.9959
	NaN	NaN	84379	82254

k = 1(b)

1.00

The comparison between Tab. 4 adapchp-dvs-CCPs and other algorithms, both the Poisson-arrival and the k-fault-tolerant schemes use the higher speed f_{1} .

		Р				
U	λ	Ε				
	(×10 ⁻²)	Poisson	<i>k</i> -f-t	A_D	A_D_S	
	(×10)					
0.76	0.14	0.6130	0.6063	0.6456	0.9544	
		149575	149738	149694	146237	
	0.16	0.5252	0.4147	0.5336	0.9104	
		151286	150869	151206	148058	
0.78	0.14	0.4731	0.3641	0.4804	0.8519	
		151926	150860	151917	149493	
	0.16	0.3016	0.2061	0.3277	0.7546	
		152389	151610	152618	150926	
0.80	0.14	0.2356	0.2283	0.2664	0.6540	
		152662	152988	153111	152034	
	0.16	0.1279	0.1195	0.1629	0.4942	
		153171	153558	153834	152927	
0.82	0.14	0.0873	0.0849	0.0950	0.3758	
		153081	153118	153365	153731	
	0.16	0.0321	0.0319	0.0418	0.2115	
		153207	153394	153946	154400	

(a) $K = \mathfrak{I}$						
			I	0		
U	λ		I	E		
	(10-4)	Poisson	<i>k</i> -f-t	A_D	A_D_S	
	$(\times 10^{-4})$			_		
0.92	1.0	0.7559	0.7570	0.7583	0.7657	
		151220	151703	150564	150564	
	2.0	0.4409	0.4398	0.4715	0.5327	
		152537	152623	152479	152546	
0.95	1.0	0.3946	0.3984	0.3878	0.3995	
		152591	154155	149117	150239	
	2.0	0.1479	0.1488	0.2775	0.2850	
		153946	154171	155132	155597	
		(b)	k = 1			

k = 1

Our experimental results are shown in table 3 and table 4. Similar to section 4.1, simulation results show that compared to ADT DVS scheme, the proposed scheme significantly increases the likelihood of timely task completion and reduces power consumption in the present of faults.

5. Conclusion

In this paper, we presented an adaptive checkpointing, using a DMR with two processors, and tuning the scheme to the specific system which it is implemented on. The proposed scheme is done by inserting two types of checkpoints (CCP and SCP) between CSCP. Separating the comparison and store operations enables choosing the optimal interval for each operation, without concerning about the other. We also discussed the optimal numbers of checkpoints that minimize the average times. Based on that, we combined the adaptive checkpoiting with the DVS schemes to achieve energy reduction. We presented simulation results which showed the advantages of our scheme. We will extend the proposed scheme to other task duplication systems with security needs as a future work.

References

- [1] Ziv A. Analysis of checkpointing schemes with task duplication, IEEE Trans. Computers, 1998,47(2):222-227
- [2] Ying Z, Crishnendu C. Task feasibility analysis and dynamic voltage scaling in fault-tolerant real-time embedded systems, Proc. Of the design, automation and test in Europe conference and exhibition (DATE'04)
- [3] Ying Z, Crishnendu C. Energy-Aware Adaptive Checkpointing in Embedded Real-Time Systems, Proc. of the design, automation and test in Europe conference and exhibition (DATE'03), 2003
- [4] Ziv A, Bruck J. Performance Optimization of Checkpointing Schemes with Task Duplication IEEE Transactions on Computers, 1997, 46(2):1381-1386
- [5] Sayori N, Satoshi F, Naohiro I. Optimal Checkpointing Intervals of Three Error Detection Schemes by a Double Modular Redundancy, Mathematical and Computer Modelling, 2003,38:1357-1363
- [6] Melhem R, Mosse D, Elnozahy E. The interplay of power management and fault recovery in real-time systems, IEEE Tran. On computers, 2004, 53(2):217-231
- [7] Intel Corp. speedstep. http://developer.inte.com/mobile/pentiumIII, 2003
- [8] Duda A. The effects of checkpointing on program execution time, Information Processing Letters, 1983 (16):221-229
- [9] Lee H, Shin H, Min S. Worst case timing requirement of real-time tasks with time redundancy, Processing Real-Time computing systems and Applications, 1999: 410-414
- [10] Osaki Applied stochastic system modeling, S. Springer-Verlag, 1992