Online RF Checkers for Diagnosing Multi-Gigahertz Automatic Test Boards on Low Cost ATE Platforms

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Abstract[1]

Digital and analog centric load boards have well established board check methodologies as part of their "release to production requirements", while for RF load boards this is still an open research issue. Potential faults on RF load can be caused by mechanical/electrical defects of components and sockets used on the board. Hence, we propose a novel methodology to accurately check/diagnose the RF path using only reflection measurements with suitable terminations of these paths. These reflection measurements and derived 'checker equations' are used to accurately diagnose the RF path on the load board during production test at no extra test cost. A pilot test vehicle is used to demonstrate the practical implementation and production worthiness of the proposed board check and diagnosis methodology.

1. Motivation and Introduction

During high volume production, *automatic test* (AT) sites often run into production problems with low yielding lots. More often than not, the low test yields are associated with problems related to the tester load board itself rather than low IC manufacturing quality. Poor storage conditions, improper handling and, the short lifetime of the components used on the *performance evaluation boards* (hereafter referred to as 'load *boards*') can cause mechanical/ electrical defects which serve as potential reasons for low test yield. For digital and analog circuits, a board check methodology is standard in the *release to production* (RTP) process. However, in the RF area, board checking algorithms and their failure diagnosis is very much an open research issue. Due to the requirement of high degree of precision in multi-parameter production test of RF devices, it is necessary to first check and diagnose problems with any component used in the RF path of the load board that is used to deliver the test stimulus to the RF DUT and relay the test response back to the external tester. Magnitude and phase calibration of this RF path has to be done periodically to avoid measurement errors and low yielding lots. Due to the absence of expensive RF bench equipment at the automatic test site to probe the RF signal path, it becomes difficult if not impossible for initial path loss calibration and to find the root cause for low yielding lots.

Typically, vector network analyzers are used to characterize RF paths on the bench set-up. But this approach cannot be directly applied to automatic load boards. Since, often only a single RF port is available for the purpose of input/output to/from the DUT (one good example will be the integrated RF transceiver). This RF port is connected to the trace of the die through the RF path. The RF signal available at the RF port is already well characterized by the automatic test equipment (ATE) vendor. But the loss in the RF path of the load board needs to be accounted for before the commencement of automatic tests. It becomes impossible to add directional couplers and RF ports near the DUT trace pins due to real estate requirements and high losses incurred on the RF path when placed near the DUT. Accurate die level wafer probe stations that could be used to diagnose the load board are very expensive to develop and maintain at automatic test sites.

Hence, we propose an *alternate test/checking methodology* to *check/diagnose* the RF load boards *"on-line"* and hence extend the range of board checkers from digital and analog centric boards to RF boards also. In the proposed approach only reflection measurements are used to check/diagnose the RF signal path. The other end of the RF path, which leads to the die trace is terminated using suitable standards. These termination standards can be easily fabricated on special *"dummy"* ICs with the same wafer material as the RF DUT to improve accuracy [1]. During load board check and diagnosis, these ICs are inserted into the board sockets instead of the RF DUTs.

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Four termination standards (implemented in the same or different *"dummy"* IC) are used in this methodology namely, (1) Open, (2) Short, (3) Characteristic 50-ohm and, (4) Known good die (KGD) or any other impedance termination (other than characteristic impedance). The final goals of the proposed checker are:

(1) Calculation of all network S-parameters

(2) Calculation of reflection coefficients at intermediate in-accessible nodes

(3) Calculation of the magnitude and phase loss in the RF signal path

The above goals are established through only reflection measurements and the derived 'checker equations'. Goals (1) and (2) are used for diagnosis of the RF boards and Goal (3) is used to check for the performance of the RF signal path and initial calibration purposes. Since it is more beneficial to evaluate the performance and coverage of a fault checker using circuit simulators, we have provided simulation results and hardware validation of the proposed checkers on a pilot test vehicle to demonstrate the production worthiness.

2. State of the art

The board check methodology is a well established concept in the analog and digital test fields. However, in the RF area, little [2] or no work has been done towards establishing an on-line production ready methodology to completely check/diagnose the RF signal paths on a load board. In [2], a methodology to test matching networks for RF attenuation using harmonics of the frequency response of lower frequency AC square waves is proposed. Often due to driver loading, it is difficult to generate very high frequency harmonic signals using lower frequency AC square waves. Even if this is possible, the power level of the resulting signal is generally incompatible with the power level requirements of the RF path being tested. Also, it is often required to calculate more than the just power attenuation to enable correct diagnosis of the RF board.

In this work, we propose to diagnose the RF load boards through calculation of complex network S-parameters and intermediate reflection coefficients. Also, the RF path loss is calculated to enable initial board check and calibration routines of the RF signal path.

3. Computation of Network Parameters

In this section, the checker equations used in the proposed methodology are derived and explained for 2 cases (1) a passive two-port network and (2) a passive three-port network.

3.1 Fault checker equations for passive 2-port networks

A two-port network with the direction of the incident and reflected powers at each port is shown in Figure 1. S-parameter equations for this network are shown in equation 1&2 respectively.

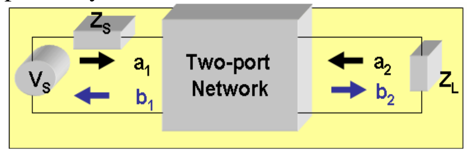

Figure 1 Two -port network

$$b1 = S11\ a1 + S12\ a2 \qquad \textbf{Equation 1}$$

$$b2 = S21\ a1 + S22\ a2 \qquad \textbf{Equation 2}$$

Terminating the two-port network with a suitable termination yields a2= Γb2 [3], where Γ is the complex reflection coefficient. Substituting this in the S-parameter equations yields,

$$\frac{b1}{a1} = S11 + \frac{\Gamma * S12 * S21}{1 - \Gamma * S22} \qquad \textbf{Equation 3}$$

- When the above two-port network is terminated with the characteristic impedance, Γ=0 i.e.

$$\Gamma(load) = \frac{b1}{a1} = \overline{S11} \qquad \textbf{Equation 4}$$

Where,

Γ*(load)* is the measured complex reflection coefficient with the characteristic50-ohm termination.

$\overline{S11}$ is the derived S11 parameter

- For an open termination Γ=1 ,

$$\Gamma(open) = \frac{b1}{a1} = S11 + \frac{S21 * S12}{1 - S22} \qquad \textbf{Equation 5}$$

- For short load Γ= -1,

$$\Gamma(short) = \frac{b1}{a1} = S11 - \frac{S21 * S12}{1 + S22} \qquad \textbf{Equation 6}$$

Where,

Γ*(open)* is the measured complex reflection coefficient with an open termination.

Γ*(short)* is the measured complex reflection coefficient with an short termination.

Terminating the network with the characteristic impedance standard (50 ohm) yields the complex S11-parameter. Using this S11 measurement and the reflection measurements with the open and short standards, S22 can be calculated as follows:

From equations 5 &6,

$$\overline{S22} = \frac{\Gamma(open) - \Gamma(short) - 2\overline{S11}}{\Gamma(open) - \Gamma(short)} \qquad \textbf{Equation 7}$$

Where, $\overline{S22}$ is the derived S22 parameter

For a passive network, *S12=S21*. Substituting in equation 5 yields,

$$\overline{S12} = \overline{S21} = \sqrt{\frac{1 - \overline{S22}}{\Gamma(open) - \overline{S11}}} \qquad \textbf{Equation 8}$$

Where, $\overline{S12}$ & $\overline{S21}$ are the derived S12 & S21 parameters respectively.

Hence, using only reflection measurements and equations 4, 7 &8 it is possible to completely characterize the two port network. This satisfies Goal (1) of the checker mentioned in Section 1. Also, it is required to calculate the loss of the network for a complex load (die during high volume test). This could be done either using another impedance termination (other than characteristic impedance like 200ohm) or terminating with a known good die (KGD).

- When the two-port network is terminated with a KGD,

$$a2 = \Gamma(KGD)\, b2 \qquad \textbf{Equation 9}$$

Where,
Γ*(KGD)* is the unknown complex reflection coefficient of the network when loaded with a KGD or any other termination used.

Substituting Equation 9 in the S-parameter equations yields,

$$\Gamma(KGD) = \frac{b1}{a1} = \frac{\Gamma(in) - \overline{S11}}{2*\overline{S12}*\overline{S21} + \Gamma(in)*\overline{S22} - \overline{S11}*\overline{S22}}$$

Equation 10

Where,
Γ*(in)* is the measured complex reflection coefficient with the KGD terminating the network.
Calculation of Γ(KGD) satisfies Goal (2) of the checker mentioned in Section 1.

3.1.1 RF path loss calculation for a two port networks

The gain/loss on the RF path for a complex load is defined as the ratio of the power delivered from the network and the power supplied to the network. From Figure 1 the 'loss' can be represented as,

$$Loss = \frac{|b2|^2 - |a2|^2}{|a1|^2} \qquad \textbf{Equation 11}$$

Since,

$$a2 = \Gamma(KGD)\, b2 \qquad \text{and,}$$

$$\frac{b2}{a1} = \frac{S21}{1 - S22*\Gamma(KGD)}$$

$$Loss = \frac{|S21|^2 (1 - |\Gamma(KGD)|)^2}{|1 - S22*\Gamma(KGD)|^2} \qquad \textbf{Equation 12}$$

Calculation of the RF path loss satisfies Goal (3) of the checker mentioned in Section 1.

3.2 Extension to 3-port passive networks

A three-port network with the direction of the incident and reflected powers at each port is shown in Figure 2. S-parameter equations for this network are shown in equations 13, 14 & 15.

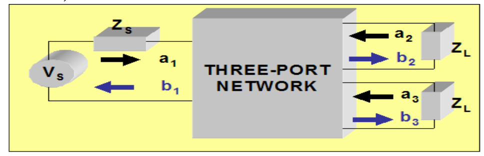

Figure 2 Three-port network

$$b1 = S11\ a1 + S12\ a2 + S13\ a3 \qquad \textbf{Equation 13}$$

$$b2 = S21\ a1 + S22\ a2 + S23\ a3 \qquad \textbf{Equation 14}$$

$$b3 = S31\ a1 + S32\ a2 + S33\ a3 \qquad \textbf{Equation 15}$$

For a three-port passive network there are 6–unknown network S-parameters including S11 which can be measured using reflection measurement with the characteristic impedance termination on both output ports (Since for passive networks, S12=S21 & S13=S31 & S23=S32)[3]. Using 5 different terminations standards in each port it is possible to determine these parameters. For each termination standard we would end up with a reflection measurement and a corresponding equation similar to equations 5 & 6. Using linear systems of equations it is possible to calculate these five unknown parameters with five equations. These calculations are quite lengthy and require the use of a math tool like MATLAB.

One possible approach to simplify the network parameter calculation of a three-port network would be to short the two output ports. This would satisfy the condition that the current entering the output port will be equal to the current leaving the output port. Hence, these could ports could treated as a single port and the calculations could be done as explained as in Section 3.1. But one down-side of this approach is that the location of a fault, if any, in the output port cannot be backtracked to a particular port. But as a first cut solution this possibly is the simplest approach to implement.

4.0 Production deployment of RF checkers

In the paper, a novel *'board check methodology'* is presented to check/diagnose the RF path on the test boards used for high volume tests. High volume tests require multi-parameter analysis to be performed on multiple ICs. Hence, the load boards are provided with die traces and sockets to enable the above. The RF pin in the die trace is connected to the RF port through a RF signal path on the load board. It is required to periodically test these paths for electrical/mechanical defects which can cause magnitude and phase losses. Since only a single RF port is available for this purpose, it becomes difficult if not impossible, to characterize these paths in the AT sites.

The proposed online board checker uses the VNA or the MVNA module in the RF ATE to make reflection measurements. The reflection measurements are made using suitable termination standards. Four termination standards are used in this methodology namely, (1) Open, (2) Short, (3) Characteristic 50-ohm and, (4) Known good die (KGD) or 200-ohm termination. These terminations can be fabricated as dummy ICs on the same wafer material as the RF DUT and hence these ICs could be directly placed in the die socket[1]. Fabricating the termination standards on the same material helps to improve the accuracy of the calculations. Based on the dimensions of the die these terminations could be fabricated on the same die or on different dies.

These measurements are fitted in the derived '*checker equations*' online by the mainframe of the tester. The clear highlight of this checker is its ability to calculate all network S-parameters and complex reflection coefficients at intermediate test points using the reflection measurements made at the input port. This data is used to diagnose the network on the board. The RF faults in a particular part of the network will reflect in the calculated S-parameter values. Also the checker calculates the RF path loss to qualify the board and to calibrate out the path loss during production test. This approach is clearly the first of its kind to provide accurate diagnosis information of RF load boards. The block diagram of the proposed methodology is shown in Figure 3.

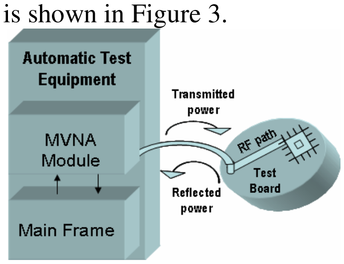

Figure 3 Block diagram of proposed methodology

5.0 Validation of proposed approach through simulation of modeled blocks

Since it is more beneficial to evaluate the performance and coverage of the fault checkers using circuit simulators, we have provided simulations results to validate the approach. Also, it is highly impractical to inject multiple RF faults on expensive production load boards. The simulations where performed using Agilent's ADS tool. The pilot vehicle used to demonstrate the production worthiness of the proposed methodology was a typical RF signal path used in RF WLAN load boards (2GHz). Figure 4 shows the schematic of the RF signal path, which consists of an RF transmission line in the unbalanced side, followed by the balun, followed by RF lines on each balanced lines with suitable DC blocking capacitors. Usually, matching circuits are used on the balanced side to compensate for any mismatch between the die tracers and the balun. But this was omitted in this work, since the goal of this work was to evaluate the checker performance and not to design an ideal load board circuit. Also, the balun is the most critical component on the load board. The behavioral model of the balun was used in the simulations. This model gives us freedom to inject gain and phase imbalances in the two balanced lines to mimic the real case. The transmission lines were designed using the passive circuit design tool in Agilent's ADS tool. The parameters of the balun and the transmission lines were optimized to operate in the 2 GHz range.

Though the signal path is a three-port network, it can be treated as a two-port network by shorting the two output ports. This enables two-port equations to be used to check/diagnose the circuit. The termination standards used by the checker were set-up in simulation as follows:

(1) The open-termination standard on both output ports were zero length open terminations

(2) The short-termination was obtained by shorting the two output terminals through a zero ohm resistance.

(3) The characteristic impedance was a 100-ohm termination used between the output ports (similar to using 50-ohm impedances on each output port).

(4) The fourth standard used to calculate the path loss was a 200-ohm termination between the output ports instead of the KGD.

Due to the difficulty in fabricating accurate termination standards on wafer a 5% random Gaussian distribution of the resistance values was used in the termination standards to mimic the real case. Also, a 5% random Gaussian distribution of the phase balance of the balun and the transmission line parameters was used to mimic the real case. The 'checker equations' were also set up in ADS to verify the proposed methodology. Equations 4, 7, 8 &10 in Section 3 were used to the purpose of diagnosis of the RF signal path. Equation 12 in Section 3 was used to check the performance of the RF signal path. Table 1 compares the actual measurement values and the calculated values using the proposed approach for a 'no fault' case. From the table it can be noted that the developed checker accurately calculates the network parameters and the path loss.

Table 1 Checker performance for a 'no-fault' case

	Actual Measurement	'RF checker' Measurement
S11(Mag/Phase)	0.182/-10.555	0.177/-10.574
S12,S21(Mag/Phase)	0.629/-94.971	0.632/-94.918
S22(Mag/Phase)	0.235/17.559	0.220/19
RF path loss(dB)	-3.870	-3.840

5.1 Fault analysis

To perform the fault analysis of the proposed checker methodology, commonly occurring RF faults on load boards were injected in the signal path. The faults included the following:

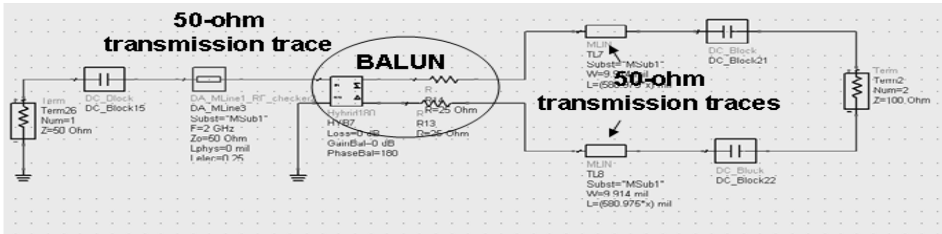

Figure 4 RF-path on load board

(1) Short on unbalanced line
(2) Open on unbalanced line
(3) Open on each of the balanced lines
(4) Short on each of the balanced lines
(5) Short between the balanced lines

These open and short faults were modeled using 1uH inductors and 1nF capacitors respectively. Figure 5 shows the schematic of the signal path highlighting the injected fault models. Table 3 summarizes the results for the above mentioned fault cases. The computed values of S12, S21, S22, Γ (200 ohm) and the RF path loss using the reflection measurements and derived 'checker equations' are compared to the actual measured values. Γ (200 ohm) is the reflection coefficient of the network to a 200 ohm impedance standard between the output ports. This measurement is required to compute the RF path loss of the network as explained in Section 3.1.1. The numbers in the above mentioned fault list directly correspond to the numbers in the fault condition column of the table. Since the output ports of the balun have a symmetric structure, the open and short faults on each of the balanced lines will have the same effect. Hence, only the open and short fault on one of the lines is shown in the table. Also since the RF signal path was a passive structure (S21=S12), S12 and S21 are displayed the same column. The checker results for the network S-parameters clearly indicate the location of the fault and the calculated path loss accurate tracks the actual path loss for each injected fault.

5.1.1 Multiple-Fault Analysis

The performance of the checker was also evaluated for multiple faults injected in the RF path simultaneously. The faults injected were an open and a short in the balanced lines. Table 2 summarizes the results obtained for the multiple faults case. The results show a high degree of accuracy in tracking the measured parameters for multiple faults too.

Table 2 Checker performance for multiple fault case

	Actual Measurement	'RF checker' Measurement
S11(Mag/Phase)	0.286/-29.70	0.286/-29.69
S12,S21(Mag/Phase)	0.001/-179.73	0.001/-179.66
S22(Mag/Phase)	1/4.84	1/4.99
Γ(200 ohm)	0.333/0.0	0.308/-8.27e-8
RF path loss(dB)	-53.83	-53.93

5.2 Fault Coverage

Different instances of the faults were generated by sweeping the capacitance and inductance values of the fault model to establish the fault coverage. The capacitance value ranged from 0(no fault) to 1 uF (near short fault). Also, the inductance was ranged from 0(no fault) to 1 mH (near open fault). Only the RF path loss measurements are shown in this section to qualify the proposed approach due to the space limitation in the paper and also since the path loss employs all the parameters that are calculated by the checker as shown in equation 12 of section 3. The path loss will be calculated accurately only if the intermediate parameters are accurate too. The distribution of the actual

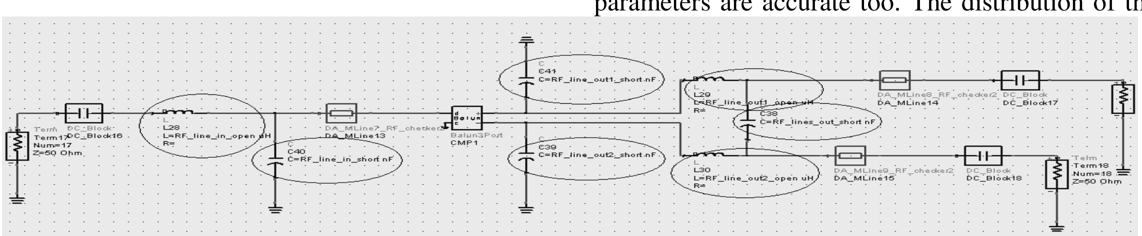

Figure 5 Schematic with various fault models

Table 3 Checker evaluation for typical RF faults

Fault Condition	S12,S21(mag/phase)		S22(mag/phase)		Γ(200 ohm) (mag/phase)		RF path loss in dB	
	Measured	Calculated	Measured	Calculated	Measured	Calculated	Measured	Calculated
(1)	0.002/176.8	0.002/176.82	0.56/2.40	0.55//2.50	0.333	0.31/8e-10	-54.14	-54.16
(2)	0.006/173.26	0.006/173.39	0.30/145.68	0.31/147.62	0.333	0.31/7.8e-11	-45.52	-45.44
(3)	0.310/-85.74	0.31/-85.77	0.39/-175.57	0.41/-175.78	0.333	0.308/1e-13	-11.77	-11.68
(4)	0.04/-174.47	0.04/-174.4	0.1/4.83	0.1/4.98	0.333	0.308/1e-11	-25.66	-25.77
(5)	0.001/179.75	0.001/179.78	1/2.33	1/2.40	0.333	0.308/1.4e-8	-54.470	-54.577

measured path loss for 130 different faults injected in the signal path is shown Figure 6 (left). The distribution of the calculated path loss using the checker for the same faulty instances is also shown in Figure 6 (right). The distributions show the range of the path losses for the different faults injected and the accuracy of the checker.

The key highlights of this experiment were:

- **Max error in path loss calculation for 130 different faults=0.1dB**
- **100 % RF fault coverage**

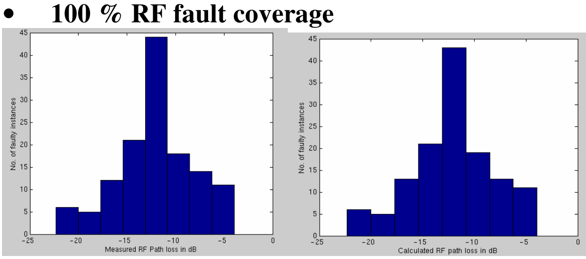

Figure 6 Distribution of measured and calculated path loss for multiple faulty instances

6.0 Hardware Validation

Hardware validation of the proposed approach was performed on a WLAN RF transceiver load board. The RF path on the load board is used for sourcing and receiving RF signals to or from the ATE to the transceiver IC. The schematic of the path is shown in Figure 7. This passive (S12=S21) RF path contains (from the right) a RF port, a matching network and a balun with biasing circuitry. The balanced output of the balun is connected to the die trace on the board. This path is optimized to operate in the 2-2.2 GHz band. This is a three port network and to simplify the calculation the two output ports were shorted to convert it to a two-port network. This would satisfy the condition that the current entering the output port will be equal to the current leaving the output port. Hence, the two output ports could be treated as a single port.

Resistor terminations were soldered down on the die trace to provide the reflection measurements. The following termination standards were used

(1) OPEN→Ideal open
(2) SHORT→Zero ohm resistance between the traces
(3) LOAD→ One hundred ohm resistance between the traces (similar to a 50 ohm resistance from each individual trace to ground)

Reflection measurements were made using a vector network analyzer (VNA). The VNA measurements were fit into the derived checker equations to calculate the S-parameters of the network. The blue line in Figure 8, corresponds to the calculated S12 and S22 of the RF path. Verifying these results poses the same problem as the motivation for this work. The absence of a physical port makes it impossible to make all S-parameter measurements. To overcome this problem, small pieces of coaxial cable ('SNIFFER') were soldered on to the two balanced die traces. All the three-port S-parameters were measured using a VNA. The S12 and S22 measured using this procedure are compared to the corresponding S-parameters measured using the resistor terminations in Figure 8. As shown in the plots, the values will not be the same since we are comparing S-parameters of two-port network with S-parameters of the 3-port network and also there is some additional losses added by the co-axial cable and the mismatch in the sniffer junction. For an ideal balun the three-port parameters will be ~3dB below the corresponding two-port parameters. But due to the variations in the balun parameters 3-3.5dB is more realistic. In this work, we compare the trend of the calculated parameters and measured parameters to provide proof of concept.

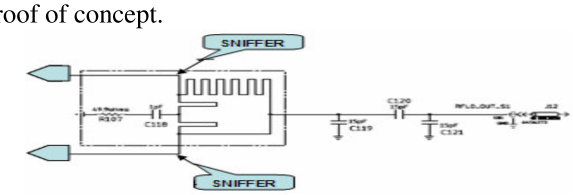

Figure 7 Schematic of the RF path used for validation

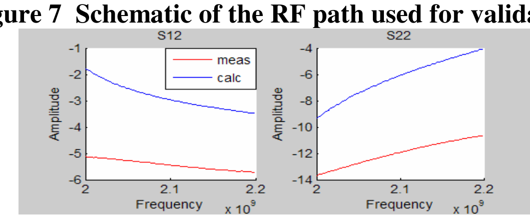

Figure 8 Comparison of calculated and measured S-parameters

7.0 Conclusion

An accurate RF checker for diagnosing and qualifying multi-giga hertz RF boards is presented. This approach is used for the purposes of initial calibration and diagnosing the RF signal path on a load bard periodically with a high level of accuracy to avoid low yielding lots in high volume tests. The methodology is simple to implement and no extra test cost is incurred. Simulations of the proposed approach show the robustness of the proposed approach for many commonly occurring RF catastrophic and parametric fault cases. Hardware validation for the proposed approach is also presented in this work. This approach could also be extended to three port and active networks by increasing the number of terminations standards and corresponding reflection measurements.

7.0 References

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