An Improved RF Loopback for Test Time Reduction

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Abstract

In this work a method to improve the loopback test used in RF analog circuits is described. The approach is targeted to the SoC environment, being able to reuse system resources in order to minimize the test overhead. An RF sampler is used to observe spectral characteristics of the RF signal path during loopback operation. While able to improve the observability of the signal path, the method also allows faster diagnosis than conventional loopback tests, as the number of transmitted symbols can be greatly reduced. Practical results for a prototyped RF link at 860MHz are presented in order to demonstrate the relevance of the method.

1. Introduction

As wireless communications are becoming widespread nowadays, they are also a requirement for new designs of electronic devices. In the SoC environment, the design of such devices is able to benefit from new sub-micron technology developments. IP-based design also allows a reduction in the time to market of new electronic products [1].

The use of wireless communications in low-cost devices also requires low cost test solutions to be competitive in the market. Unfortunately, RF testers are costly, because they must generate high-quality RF signals and measure RF parameters. This way, analog RF generators and receivers should be added to a digital tester, increasing the total cost of the tester.

A popular method for testing RF analog circuits is the loopback approach. Among its advantages, loopback test has a low cost of implementation and enables the measurement of bit error rate (BER), a key parameter for accessing the performance of a transceiver [2,3]. Also, loopback allows go/no go tests.

However, the loopback method suffers from reduced observability of the signal path, as the transceiver is tested as a whole, and some faults may be masked. Also, loopback requires the transmission of a large number of bits in order to estimate the BER.

In this work an approach to improve standard loopback tests is presented, being based on a low-cost single-bit digitizer. The digitizer allows simultaneous monitoring of several analog test points in the RF signal path, increasing the observability and fault detection capabilities in loopback tests.

By processing the output of the digitizer, it is possible to analyze spectral characteristics of the RF signal path while the conventional loopback method is being applied. This way, a faulty signal path can be revealed before the completion of a standard loopback test. The approach is able to achieve considerable test time reduction by simply interrupting the bit transmission, since diagnosis can be made through the use of spectral analysis of the already transmitted bits.

The paper is organized as follows: in section 2 a brief review of other approaches is presented. In section 3, the conventional method for BER estimation is reviewed, and the improved loopback method is presented. Practical results are presented in section 4. Analysis is provided in section 5 and the paper finishes with conclusions and further work in section 6.

2. Related work

Loopback test techniques are based on the idea of routing the output of a system directly back to its input, without using the wireless link (see figure 1).

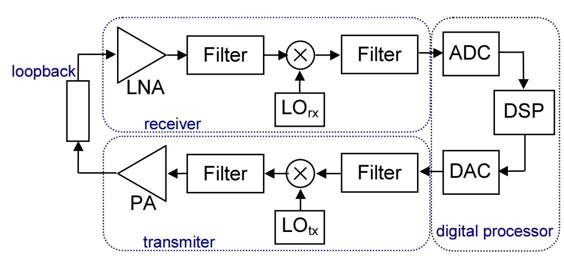

Fig. 1 Loopback test structure

For integrated transceivers in the SoC environment, the loopback test technique can reuse DSP and memory resources already available in the system for the test response analyzer and signal generation. This approach may be able to reach the lowest test cost possible, if only switches and attenuators are needed. Another advantage is the lower effort in order to implement the test and high flexibility, as the test is implemented in software and does not depend on the technology of the transceiver.

The disadvantages of the loopback technique are mainly related to the fact that the transceiver is tested as whole, without access to important internal points. This way, faults in the transmitter could be masked by the receiver, reducing fault coverage and making fault diagnosis not possible [4]. For example, a defect in the transmitter could be masked by the use of an excellent receiver that filters the out-of-band distortion. Also, a weak transmitter could be compensated by a strong receiver. Another issue is that the signal level at the output of the transmitter may not be the signal level that is desirable or possible to measure with the receiver. Also, test time is long if a low bit error rate (BER) should be evaluated.

There are some attempts in order to increase observability and controllability of the signal path. In [5] additional single-bit DA converter is used. In [4,6] additional AD converter and frequency translation elements are used. The test overhead in this case may be considerable, as practically another receiver needs to be implemented.

In [7] optimized periodic bit streams are used in a loopback configuration and functional parameters like IP3 are estimated. However, the approach suffers from loopback reduced observability. In [8], embedded sensors are used in the transceiver to get maximum accuracy in prediction of a set of target specifications. In [9] a CMOS RF RMS detector aimed at RF testing is introduced. However, the use of RF sensors with dc output require additional AD converters for BIST implementation, which may increase test cost and area overhead.

In [10], a detailed loopback analysis is presented and it is suggested the use of EVM in order to reduce test time, in opposition to BER (SER). However, the necessity of an ADC+DSP to acquire baseband data in order to evaluate EVM restricts the applicability of the approach. In [11], a technique to reduce the need for long bit sequences called Q-factor is presented. However, the implementation of the technique also needs knowledge of the baseband signal, requiring an ADC+DSP structure.

In a loopback test, if one could insert several digitizers (like the one in [12]) in key test points, one should expect better diagnosis capability. Furthermore, while loopback test allows the application of a test stimulus, data obtained from the additional digitizers can be used to evaluate the signal path performance, and is not restricted to an ADC+DSP receiver architecture.

An approach to accomplish this is proposed in the next section.

3. Loopback test

In this section BER evaluation in loopback tests is discussed, and the improved loopback method is presented.

3.1 BER evaluation in loopback tests

BER is the average number of erroneous bits observed at the output of the detector divided by the total number of bits received in a unit time [2]. Data bits are provided by the use of a pseudo random binary sequence (PRBS). For example, a PN9 sequence uses 511 bits and a PN15 sequence uses 32767 bits, which are commonly used in the test of receivers.

In [10], 2000 symbols are used for the evaluation of a receiver using a conventional approach. Generally, however, the evaluation of BER for a given system would be based on the expected performance of the receiver. The BER (P(e)) can be related to the SNR of a receiver, as shown in figure 2. It also depends on the modulation type.

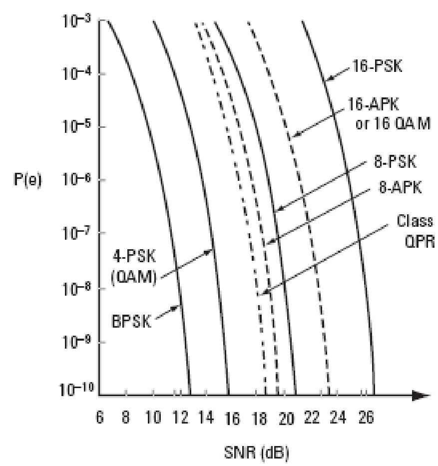

Fig. 2 Probability of error versus SNR [3]

For example, the evaluation of a BER of 10^{-3} or 0.1% using Binary PSK (BPSK) would require at least 1000 bits to be transmitted. However, as shown in figure 2, the number of required bits for the evaluation of lower BER can easily reach 1e6 ($P(e)=10^{-6}$) or 1e9 ($P(e)=10^{-9}$). The requirements for a large number of transmitted bits can make the approach unsuited for BIST or production tests, since test time is greatly increased. Averaging may also be required for improving the BER measurement, increasing test time even further.

The real operation conditions of a receiver may not match the ideal case used in constructing figure 2. For example, noise may not be gaussian but may have a strong spectral component. This may limit the evaluation of BER from SNR data in practical situations.

3.2 Improved loopback

The improved loopback diagram is shown in figure 3. The transceiver is redrawn in order to enable the entire block diagram to be shown: the circuit under test (transmitter and receiver blocks), digitizers and memory and processing resources from the SoC environment.

Because of the low cost and low analog area overhead, several digitizers can be built in the signal path. As the sampler is always connected, it presents a constant load to the RF circuit that could be adequately accounted for in the design stage of the RF system. The digitizer can be constructed using a simple voltage comparator as illustrated in figure 4. This sampler allows the observation of the spectral characteristics of the signal (see [13] for details).

Through the analysis of the spectrum of the RF signal, it is possible to verify the current behavior of the circuits against a previously recorded model, without having to wait for the long loopback bit sequence to be transmitted.

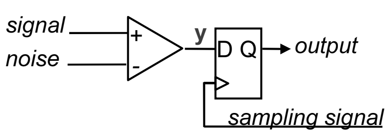

Fig. 4 Digitizer

In order to illustrate the approach, the loopback structure in figure 3 was simulated in Matlab. The simulation implemented a QPSK modulator and demodulator [2] and an RF link where a statistical sampler was included. The functional model for the mixer and amplifiers followed the implementation examples from [14]. Typical values for parameters like intermodulation distortion and gain were taken from [2].

The simulation consisted in transmitting 30,000 bits through the loopback connection and observing the BER. Then, the signal path is modified and the fault detection using conventional BER and using the results from the statistical sampler are compared.

The modulated QPSK signal is at 20MHz. This is the input signal to the first mixer in figure 3. The local oscillator frequency in the transmitter is 200MHz. At the output of the mixer, there is a component at 220 MHz and a component at 180MHz. The TX filter was designed to filter out the 180MHz component. In figure 5 the power spectrum density (PSD) of the input signal to the power amplifier is shown, being evaluated using 1-bit data from the sampler.

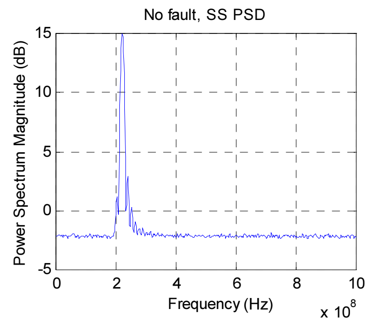

Fig. 5 PSD of PA input for nominal conditions

Faults were simulated by changing the cutoff frequency of the TX filter, thus impacting the signal at the power amplifier input. The digitizer used in the simulation is shown in the marked zone in figure 3.

For -10% deviations in the cutoff frequency of the TX filter, no bit error was detected using the conventional loopback approach. However, one can easily observe the image signal resulting from the faulty filter in the marked area of figure 6, as the attenuation is reduced. This is an example of a fault being masked by the signal path and that would not be detected by a

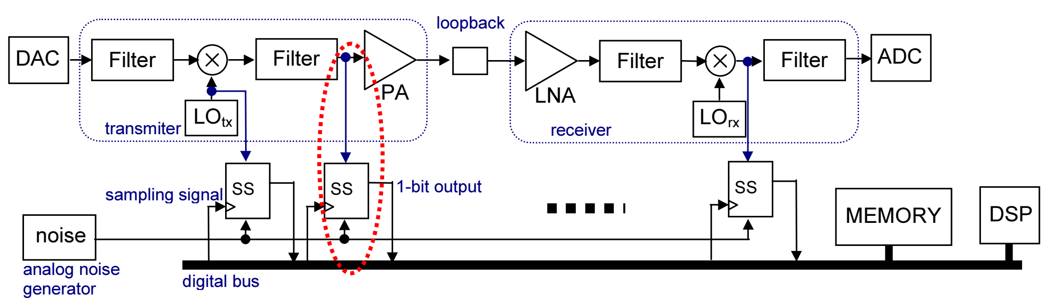

Fig. 3 Improved loopback structure (marked zone shows the sampler used in the simulation example)

standard loopback test. The improved loopback approach is able to detect this fault because of the enhanced observability provided by an additional sampler.

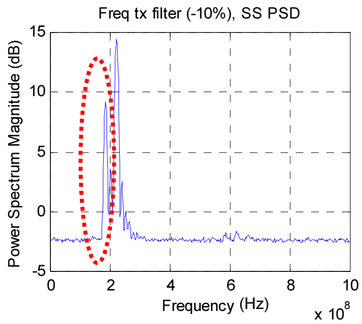

Fig. 6 PSD of PA input for -10% deviation in TX filter cutoff frequency

Another simulation using a +10% deviation in the cutoff frequency of the same TX filter was also performed. In this case, a BER of 6.9% was obtained, indicating the fault. Although the standard loopback test is able to detect this problem, one is not able to locate this fault, as the whole transceiver is tested. By inspecting the PSD plot from the statistical sampler (marked area in figure 7), however, one is able to compare to figure 5 and verify the lower amplitude of the signal, thus locating the problem in the transmitter.

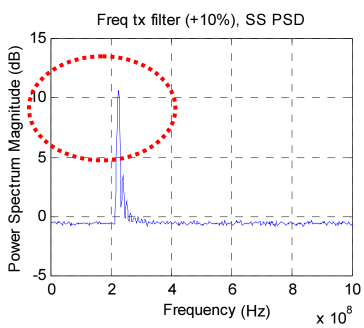

Fig. 7 PSD of PA input for +10% deviation in TX filter cutoff frequency

4. Practical results

In this section the prototyped loopback circuit and instrumentation used are described in detail. Loopback operation for PSK signals under several conditions of operation is then analyzed using a spectrum analyzer and data from the statistical sampler.

A prototype RF loopback has been built using discrete components, and the block diagram is shown in figure 8. The loopback RF section was implemented using two mixers modules prototyped using parts from Analog Devices (AD8343), and a saw filter from Epcos (B4122) was used to center the channel around 836.5 MHz, with a 25 MHz bandwidth. The RF oscillator is an RF generator from Rohde&Schwarz (SM300).

The base band transmitter used an arbitrary waveform generator from Rohde&Schwarz (AM300), which is able to generate PSK signals from an external reference. A LFSR was implemented in an external FPGA board in order to provide data for the PSK modulator (a PRBS sequence of length 2047). The generator frequency is set to 20MHz and the external LFSR clock frequency is 5MHz.

The base band demodulator is implemented in software using Matlab. Data acquisition is performed using a high-speed (100 MS/s) digitizer from National Instruments (NI 5112).

The statistical sampler was implemented using an ultra fast voltage comparator from Analog Devices (ADCMP565). The noise generator is the HP33120A arbitrary waveform generator. In order to sample the high frequency signals from the comparator output, a high speed (4GS/s) scope from Agilent (Infiniium 54833D) was used. A photograph of the prototyped experimental setup is shown in figure 9.

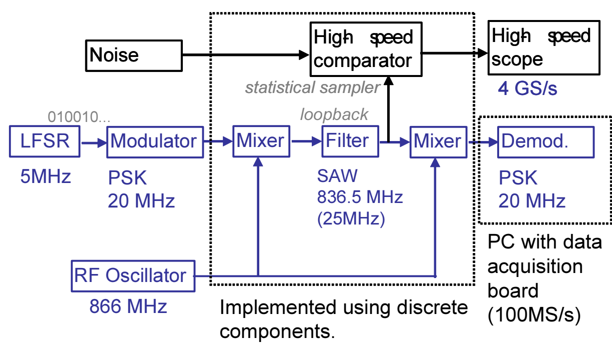

Fig. 8 Block diagram of the experimental setup

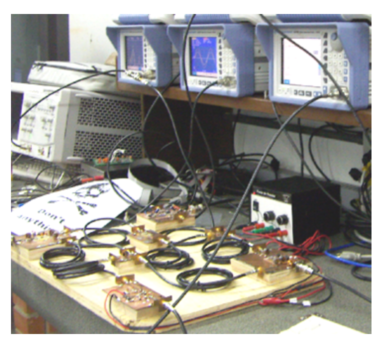

Fig. 9 Photograph of the experimental setup

Under normal operation a series of bits are transmitted and received over the channel. Nominal conditions are a 866MHz carrier with 12mV amplitude. This selects the lower PSK signal band. In order to evaluate the BER of the prototyped transceiver, the amplitude of the PSK generator was changed and the

BER has been evaluated. The results for different acquisition times are shown in table 1.

Table 1 BER and bit errors for amplitude variation of PSK signal versus number of received bits (N)

BER (%)

input (mV)	N=6e3	N=2e4	N=2e5	N=1e6
50.0	0	0	0	0
45.0	0	0	0	.0002
40.0	0.1833	0.0600	0.0110	0.0042
38.0	0.0333	0.0450	0.0320	0.0269
35.0	16.0500	4.8650	38.9240	41.8120
30.0	49.2085	12.4094	36.6108	44.6114

Bit Errors

input (mV)	N=6e3	N=2e4	N=2e5	N=1e6
50.0	0	0	0	0
45.0(*)	0	0	0	2
40.0(*)	11	12	22	42
38.0	2	9	64	269
35.0(*)	963	973	77848	418120
30.0	2953	2482	73222	446114

By analyzing the results in table 1, one should note that minimizing the amplitude of the PSK signal is equivalent to lower the SNR. As discussed in section 3, the BER is expected to increase as the SNR decreases.

In figure 10, the PSD at the SAW filter output is presented, being evaluated using an FFT of length 10K and 2e6 1-bit data samples total from the sampler.

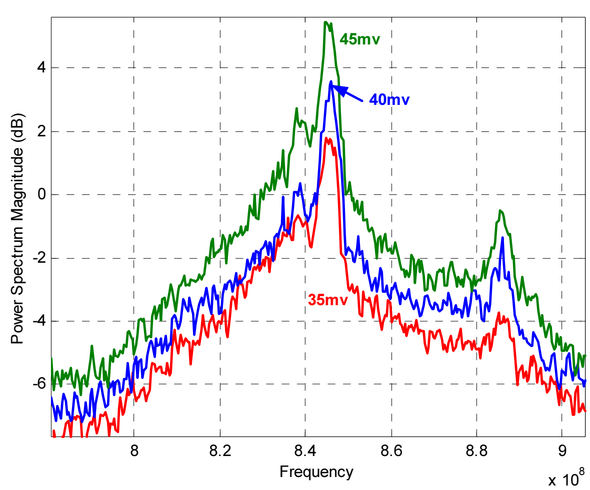

Fig. 10 Spectrum at saw filter output using PSD of statistical sampler data (1-bit)

As the sampler data is acquired at RF, even a large data set has a short acquisition time when compared to the base band needs. Table 2 illustrates the time needed for both approaches (considering only the acquisition time).

Table 2 Acquisition time needed

Loopback	N=6e3	N=2e4	N=2e5	N=1e6
	1.2 ms	4.0 ms	40 ms	200 ms
Spectral analysis	2.05e6[S]/4e9[S/s]= 0.5 ms			

Table 3 BER for RF carrier frequency variation

Carrier frequency (MHz)	Bit errors	Bits received	BER (%)
866.0(*)	0	5000039	0
868.0	0	5000039	0
870.0	0	5000039	0
880.0(*)	0	5000040	0
890.0(*)	533	5000036	0.0107

One of the main concerns in using loopback tests is its inability to provide a good indication of physical characteristics of the RF signal path and its integrity. The use of digital modulation schemes like BPSK (intrinsically robust to noise, as shown in figure 2), makes the use of BER as a poor estimate of channel quality.

In order to illustrate this point, the BER for carrier frequency variation is shown in table 3. This variation would be similar to different filter cutoff frequencies, as the PSK signal suffers increased attenuation from the filter as the carrier frequency is increased. The loopback approach takes 1s in this case because of the larger number of bits received.

The effect of RF carrier frequency variation on the modulated PSK signal in RF is shown in figure 11, using data from the spectrum analyzer. The same analysis is performed using data from the statistical sampler, and the results are presented in figure 12. One should notice that loopback errors were not detected for a carrier frequency of 880MHz, which suffers attenuation from the filter. This attenuation can be easily noticed in the spectrum plots of figures 11 and 12.

5. Analysis

Experimental data provided in section 4 has demonstrated that, although BER tests provide usefull information for the channel, they may not be able to detect a large number of faults.

In the previous section, analysis of amplitude variation produced BER that were estimated using bit sequences up to 1Mbits, and BER estimation time of from 1 to 200ms. Data acquisition for needed for PSD evaluation took only 0.5 ms because of the higher sampling frequencies involved, enabling a speedup in analysis of the RF signal path from 2 to 400.

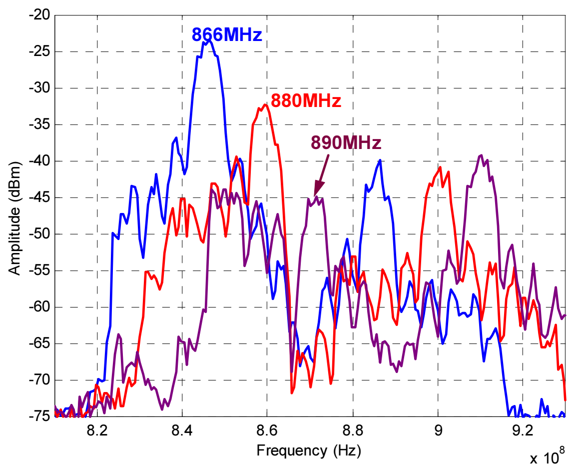

Fig. 11 Spectrum at saw filter output for several RF carrier frequencies using Spectrum Analyzer

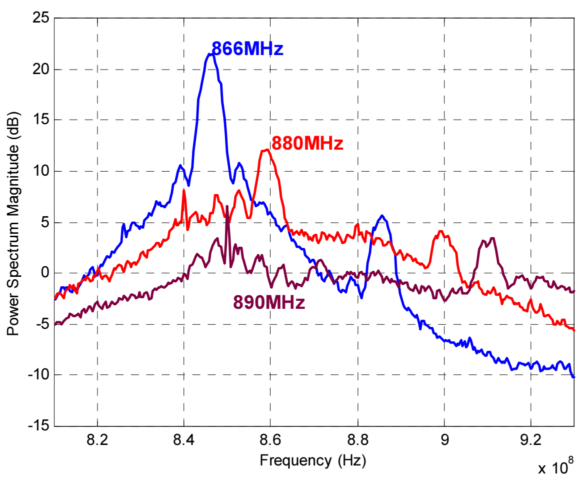

Fig. 12 Spectrum at saw filter output for several RF carrier frequencies using PSD of statistical sampler data (1-bit)

Another problem with BER was demonstrated in the carrier frequency sweep example: no bit error detected in a significant change in the RF channel. This may be explained by the robustness of digital modulation schemes, but it also impacts the capabilities of using BER as a measure of channel quality. Spectral analysis of statistical sampler data, on the other hand, can provide relevant channel information even if no BER is detected.

6. Conclusions

Simulation and practical results on a prototyped circuit were presented, and it has been noted that a great reduction in test time (from 2 to 400) could be achieved over a standard loopback approach, if only acquisition time is considered. Also, some limitations in using BER as a quality measurement for analyzing the RF signal path have been pointed out in an example.

Further work includes the analysis and generation of quality measures from the PSD data obtained in loopback tests using the proposed approach.

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