A Signal Theory Based Approach to the Statistical Analysis of Combinatorial Nanoelectronic Circuits

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Abstract

In this paper we present a method which allows the statistical analysis of nanoelectronic Boolean networks with respect to timing uncertainty and noise. All signals are considered to be instationary random processes which is the most general signal representation. As one cannot deal with random processes per se, we focus on certain statistical properties which are propagated through networks of Boolean gates yielding the instationary probability density function (pdf) of each signal in the network. Finally, several values of interest as the error probability, the average path delay or the average signal trace over time can be extracted from these pdf.

1. Introduction

Emerging device technologies are expected to enable the design of digital systems with a much higher density of devices than today, allowing unprecedented new products and services. Therefore, there is a great attention to the research of this kind of new nanoelectronic devices, which will lead to a massive use of components, orders of magnitude higher than today, with component reliabilities orders of magnitude lower than today.

Several approaches have been proposed throughout the years in order to build reliable systems out of unreliable components which go back to the ideas of von Neumann [6]. An interesting approach for future systems may be the concept of *error tolerance* as discussed in [2], i.e. for many applications it is not necessary to get 100% error free results but to achieve a certain level of reliability. The most popular example here may be a video processing unit where a single pixel error is not recognized by the user but many of them certainly are. That is the *average error* has to be kept below a certain level.

Statistical analysis is perfectly suited for this kind of approach. This has already been exploited for the statistical static timing analysis (statistical STA) as e.g. discussed in [3, 4] and a design methodology based on Markov Random Fields is proposed in [1] dealing also with the probability of logic values.

Logic values become increasingly critical when the supply voltages further decrease and the logic thresholds approach the thermal noise floor.

Nevertheless, each of these approaches consider either timing or logic levels but not both. Within this paper we propose a method which allows one to deal with the timing and the logic levels at a time within a single simulation environment.

We use the notation from [5] for probabilities, random variables, random processes etc. We do not use any units for logic levels, time instances or noise power because they are simply not important for the principle of the proposed approach. Thus, the physical values can be considered to be *normalized*.

The remaining paper is organised as follows: In Sec. 2 the signal description and the gate models which are used throughout this work are introduced followed by a simplified consideration in Sec. 3. Experimental results are presented in Sec. 4 and the paper is concluded with Sec. 5.

2. Theoretical Analysis

Within this section we introduce the signal representation which is used throughout this work. Then, we present how these signals are affected by the models of the Boolean gates.

In order to be as general as possible, we model each signal by a *random process*, $\boldsymbol{s}(\eta, t)$, where η represents the result of a random experiment, and t is the time. This is the most general description of a signal. Nevertheless, one cannot deal with a random process per se. Thus, it is usually described by its statistical properties, which in turn can be determined if the joint *probability density function (pdf)* of ar-

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bitrary order N is known:

$$F_{\boldsymbol{s}\cdots\boldsymbol{s}}(\vec{s},\vec{t}) = P\left(\bigcap_{n=1}^{N}\{\eta\,|\boldsymbol{s}(\eta,t_n)\le s_n\}\right)\forall N\in\mathbb{N}\,, \quad (1)$$

with $\vec{s} = (s_1,...,s_N)$ and $\vec{t} = (t_1,...,t_N)$. This is usually not the case and the pdf up to order $N = 4$ is used for statistical signal processing [5]. Nevertheless, the signal properties which are of interest for this work can be extracted from the pdf of order $N = 1$, $f_{\boldsymbol{s}}(s,t)$. Hence, we use this one as signal representation during this work. Consequently, the term pdf refers in the following to this first order pdf unless otherwise stated.

Consider as an example that you know the (time dependent) pdf of an instationary random process at the output of a logic circuit. In addition you know what values are expected at which time instance. Thus, you can easily determine the probability of error as a function of time and from that the average error (e. g. due to process variations and noise) at the output of the circuit. These results may be used to accomplish a reliability-yield trade-off.

Boolean gates are modeled by networks of several basic building blocks (BBB) throughout this work. These blocks are in particular *random delay, nonlinear transfer characteristic, min- and max-operators*. The pdf of the individual signals are then transfered through this BBB-network which can in turn be derived from a gate level schematic.

2.1. Transfer of the signal's pdf through BBBs

In this section we consider the transfer of the random processes through the individual basic building blocks used for gate modeling particulary with regard to how the signal's pdf is affected by each BBB.

Transfer of pdf through random delay Consider a instationary random process $\boldsymbol{x}(\eta,t)$ at the input of a delay element. The delay of the delay element is not known exactly but can be described by a random variable $\boldsymbol{T}(\eta)$ which may or may not be statistically independent from $\boldsymbol{x}$. The output of the delay element is – as the input – described by an instationary random process $\boldsymbol{y}(\eta,t)$.

In order to find the pdf $f_{\boldsymbol{y}}(y,t)$, we consider at first the cumulative distribution function (cdf) $F_{\boldsymbol{y}}(y,t)$:

$$\begin{aligned} F_{\boldsymbol{y}}(y,t) &= P\left(\{\eta\,|\boldsymbol{y}(\eta,t)\le y)\}\right)\\ &= P\left(\{\eta\,|\boldsymbol{x}(\eta,t-\boldsymbol{T}(\eta))\le y)\}\right)\\ &= \int_{-\infty}^{y}\int_{-\infty}^{\infty} f_{\boldsymbol{xT}}(x,\tau,t-\tau)d\tau dx\,, \end{aligned} \quad (2)$$

where $f_{\boldsymbol{xT}}(x,T,t)$ denotes the joint pdf of $\boldsymbol{x}(\eta,t)$ and $\boldsymbol{T}(\eta)$.

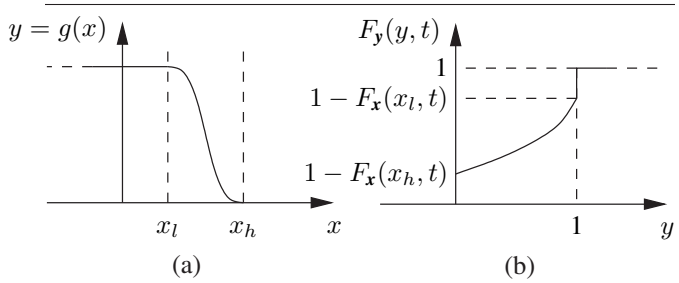

Figure 1. (a): Nonlinear transfer characteristic as used for this work, (b): Sample output cdf with steps at y=0 and y=1.

From this expression the pdf can be derived:

$$f_{\boldsymbol{y}}(y,t) = \frac{\partial F_{\boldsymbol{y}}(y,t)}{\partial y} = \int_{-\infty}^{\infty} f_{\boldsymbol{xT}}(y,\tau,t-\tau)d\tau\,. \quad (3)$$

In the case that $\boldsymbol{x}$ and $\boldsymbol{T}$ are statistically independent Eq. (3) simplifies to:

$$f_{\boldsymbol{y}}(y,t) = \int_{-\infty}^{\infty} f_{\boldsymbol{x}}(y,t-\tau)f_{\boldsymbol{T}}(\tau)d\tau\,. \quad (4)$$

Thus, if statistical independence can be assumed, the pdf of the output signal solely depends on the pdf of the input signal and the statistical properties of the delay element itself. The joint pdf is not needed anymore.

Transfer of pdf through nonlinear transfer characteristic In this section we deal with the transfer of a given pdf through a certain subset of memoryless systems exhibiting a nonlinear transfer characteristic $y = g(x)$, i.e. the considered systems have a transfer characteristic given by:

$$g(x) = \begin{cases} 1 & \text{if } x < x_l \\ \tilde{g}(x) & \text{if } x_l \le x \le x_h \\ 0 & \text{if } x > x_h \end{cases} \quad (5)$$

where $\tilde{g}(x)$ is a strictly monotonic decreasing function with $\tilde{g}(x_l) = 1$ and $\tilde{g}(x_h) = 0$ as depiceted in Fig. 1a. Under these constraints, the cdf of the output signal $\boldsymbol{y}(\eta,t)$ can be derived as:

$$F_{\boldsymbol{y}}(y,t) = \begin{cases} 0 & \text{if } y < 0 \\ P\left(\{\eta\,|\boldsymbol{x}(\eta,t)\ge h(y))\}\right) & \text{if } 0 \le y \le 1 \\ 1 & \text{if } y > 1 \end{cases}, \quad (6)$$

where $h(y)$ denotes the inverse function of $\tilde{g}(x)$. With $P\left(\{\eta\,|\boldsymbol{x}(\eta,t)\ge h(y))\}\right) = 1 - F_{\boldsymbol{x}}(h(y),t)$ the cdf $F_{\boldsymbol{y}}(y,t)$ exhibits two steps. The first one occurs at $y = 0$ with height $1 - F_{\boldsymbol{x}}(x_h,t)$ and the second one at $y = 1$ with height

$1-(1-F_{\boldsymbol{x}}(x_l,t)) = F_{\boldsymbol{x}}(x_l,t)$ as can be seen in Fig. 1b. Thus, for the pdf of the output applies:

$$f_{\boldsymbol{y}}(y,t) = \delta(y)\left(1-F_{\boldsymbol{x}}\left(x_h,t\right)\right)+\delta(y-1)F_{\boldsymbol{x}}\left(x_l,t\right) - f_{\boldsymbol{x}}(h(y),t)\frac{\partial h}{\partial y}(H(y)-H(y-1))\,, \quad (7)$$

where $H(y)$ denotes the Heaviside and $\delta(y)$ the Dirac delta function.

Transfer of pdf through min- and max-operators The basic configuration considered in this section is as follows: The two signals $\boldsymbol{x}(\eta,t)$ and $\boldsymbol{y}(\eta,t)$ serve as inputs of a two-input one-output processing block. The output of this block is denoted with $\boldsymbol{z}(\eta,t)$ and adopts the input value which is either less or greater than the other one, depending on the type of processing block. The *min-operator* propagates the less input value whereas the *max-operator* propagates the greater one to the output.

The cdf of the output of the *max-operator* is given by:

$$F_{\boldsymbol{z}}(z,t) = P\left(\{\eta\,|\boldsymbol{x}(\eta,t)\le z)\,\}\cap\{\eta\,|\boldsymbol{y}(\eta,t)\le z)\,\}\right)\,, \quad (8)$$

which yields the pdf of $\boldsymbol{z}(\eta,t)$:

$$f_{\boldsymbol{z}}(z,t) = \frac{\partial}{\partial z}\left(\int_{-\infty}^{z}\int_{-\infty}^{z} f_{\boldsymbol{xy}}(x,y,t,t)dxdy\right) = \int_{-\infty}^{z} f_{\boldsymbol{xy}}(z,y,t,t)dy+\int_{-\infty}^{z} f_{\boldsymbol{xy}}(x,z,t,t)dx\,, \quad (9)$$

where $f_{\boldsymbol{xy}}(x,y,t_1,t_2)$ denotes the joint pdf of the instationary random processes $\boldsymbol{x}$ and $\boldsymbol{y}$.

In the case that $\boldsymbol{x}$ and $\boldsymbol{y}$ are statistically independent, the result from Eq. (9) becomes:

$$f_{\boldsymbol{z}}(z,t) = f_{\boldsymbol{x}}(z,t)\int_{-\infty}^{z} f_{\boldsymbol{y}}(y,t)dy + f_{\boldsymbol{y}}(z,t)\int_{-\infty}^{z} f_{\boldsymbol{x}}(x,t)dx \quad (10)$$

For the cdf of the *min-operator* output holds accordingly:

$$F_{\boldsymbol{z}}(z,t) = P\left(\{\eta\,|\boldsymbol{x}(\eta,t)\le z)\,\}\cup\{\eta\,|\boldsymbol{y}(\eta,t)\le z)\,\}\right)\,, \quad (11)$$

resulting in a pdf

$$f_{\boldsymbol{z}}(z,t) = \frac{\partial}{\partial z}\left(1-\int_{z}^{\infty}\int_{z}^{\infty} f_{\boldsymbol{xy}}(x,y,t,t)dxdy\right) = \int_{z}^{\infty} f_{\boldsymbol{xy}}(z,y,t,t)dy+\int_{z}^{\infty} f_{\boldsymbol{xy}}(x,z,t,t)dx\,, \quad (12)$$

which finally leads to

$$f_{\boldsymbol{z}}(z,t) = f_{\boldsymbol{x}}(z,t)\int_{z}^{\infty} f_{\boldsymbol{y}}(y,t)dy + f_{\boldsymbol{y}}(z,t)\int_{z}^{\infty} f_{\boldsymbol{x}}(x,t)dx \quad (13)$$

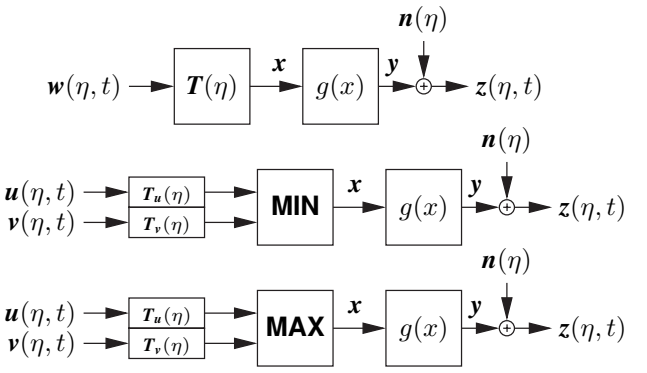

Figure 2. Composition of logic gates from presented BBBs. From top down: NOT-, NAND- and NOR-gate.

in the case of statistical independence.

2.2. Composition of logic gates from BBBs

This section deals with the idea to replace the gates of a Boolean network with the BBB discussed in the previous section. In the scope of this paper we will limit our consideration to *NOT*, *NAND* and *NOR* gates, whereas the latter two have two inputs.

The BBB representation of these three types of gates is depepicted in Fig. 2 and is self-explanatory.

For convenience, we use the same nonlinear characteristic for all gates. This idealized characteristic, $g(x)$, outputs a '1' as long as the input signal, x, is less than a certain threshold, x_t, and '0' otherwise. Thus, it can be described in analogy to Eq. (5) by:

$$g(x) = \lim_{\varepsilon\to 0}\begin{cases} 1 & \text{if } x < x_t-\varepsilon \\ -\frac{1}{2\varepsilon}x+\frac{x_t+\varepsilon}{2\varepsilon} & \text{if } x_t-\varepsilon\le x\le x_t+\varepsilon \\ 0 & \text{if } x > x_t+\varepsilon \end{cases}\,, \quad (14)$$

which yields the inverse function $h(y)$ as introduced with Eq. (6) and the pdf of the output signal from Eq. (7):

$$h(y) = \lim_{\varepsilon\to 0} -2\varepsilon y + x_t + \varepsilon = x_t \Rightarrow \frac{\partial h}{\partial y} = 0 \quad (15)$$

$$f_{\boldsymbol{y}}(y,t) = \delta(y)\left(1-F_{\boldsymbol{x}}\left(x_t,t\right)\right) +\delta(y-1)F_{\boldsymbol{x}}\left(x_t,t\right)\,. \quad (16)$$

This expression reflects the property of logic gates to restore the logic value of the signal, i. e. additive noise on the input signal may lead to wrong logic values at the output but the output of the this transfer characteristic is either '0' or '1' (apart from the singularity occuring at $x = x_t$).

The additive stationary noise at the output of each gate is treated by simply convolving the noise's pdf with the signal's pdf, i. e. by replacing $\delta(y)$ with $f_{\boldsymbol{n}}(z)$ and $\delta(y-1)$

with $f_{\boldsymbol{n}}(z-1)$ in Eq. (16):

$$f_{\boldsymbol{z}}(z,t) = f_{\boldsymbol{n}}(z)\left(1 - F_{\boldsymbol{x}}\left(x_t,t\right)\right) + f_{\boldsymbol{n}}(z-1)F_{\boldsymbol{x}}\left(x_t,t\right). \tag{17}$$

Thus, in this model, the output signal is corrupted only by the noise generated by the gate itself. The noise from the input(s) only has an influence on the probability that the output adopts its correct value.

3. Simplified Signal Model

The previous section reflects the fact that the pdf of all signals at the output of the gates (i. e. after the idealized nonlinear transfer characteristic) can be expressed by Eq. (17). Note that signals at the output of the *min-* or *max-operator*, respectively, cannot be described by Eq. (17). Nevertheless, this is again possible for the output signal of the subsequent nonlinear transfer block.

In addition we now make the assumption that all stationary noise processes are Gaussian distributed with power $N_{\boldsymbol{x}}$ and zero mean. Thus, each signal's pdf is fully determined by the noise power and a conventional time dependent function $E_{\boldsymbol{x}}(t) = F_{\boldsymbol{x}}(x_t,t)$.

It is interesting to note, that the function $E_{\boldsymbol{x}}$ directly reflects the time dependent expected value of the random process $\boldsymbol{x}(\eta,t)$:

$$E\{\boldsymbol{x}(\eta,t)\} = \int_{-\infty}^{\infty} x f_{\boldsymbol{x}}(x,t)dx = F_{\boldsymbol{x}}(x_t,t) = E_{\boldsymbol{x}}(t)\,. \tag{18}$$

Thus, the function $E_{\boldsymbol{x}}(t)$ directly describes how the signal changes *on an average* over time.

Consider as an example a signal $\boldsymbol{x}(\eta,t)$ which changes its state from '0' to '1' at a time instance $\boldsymbol{T}(\eta)$, which is not known exactly but can be described by a random variable determined by its pdf $f_{\boldsymbol{T}}(T)$. In addition, this signal is corrupted by additive noise. The noise process is assumed to be stationary and defined by its pdf $f_{\boldsymbol{n}}(n)$. Thus, the pdf of the signal $\boldsymbol{x}(\eta,t)$ is given by

$$f_{\boldsymbol{x}}(x,t) = f_{\boldsymbol{n}}(x)\underbrace{\int_{t}^{\infty} f_{\boldsymbol{T}}(\tau)d\tau}_{1-E_{\boldsymbol{x}}(t)} + f_{\boldsymbol{n}}(x-1)\underbrace{\int_{-\infty}^{t} f_{\boldsymbol{T}}(\tau)d\tau}_{E_{\boldsymbol{x}}(t)}\,. \tag{19}$$

In this section we analyse how the function $E_{\boldsymbol{x}}(t)$ is affected by our model gates.

In the case of the delay the following holds from Eq. (4) and Eq. (17):

$$\begin{aligned} f_{\boldsymbol{y}}(y,t) \;&=\; f_{\boldsymbol{n}}(y)\int_{-\infty}^{\infty}\left(1 - E_{\boldsymbol{x}}(t-\tau)\right) f_{\boldsymbol{T}}(\tau)d\tau \\ &\quad + f_{\boldsymbol{n}}(y-1)\int_{-\infty}^{\infty} E_{\boldsymbol{x}}(t-\tau) f_{\boldsymbol{T}}(\tau)d\tau \\ &=\; f_{\boldsymbol{n}}(y)\left(1 - \int_{-\infty}^{\infty} E_{\boldsymbol{x}}(t-\tau) f_{\boldsymbol{T}}(\tau)d\tau\right) \\ &\quad + f_{\boldsymbol{n}}(y-1)\int_{-\infty}^{\infty} E_{\boldsymbol{x}}(t-\tau) f_{\boldsymbol{T}}(\tau)d\tau \\ &\Rightarrow\; E_{\boldsymbol{y}}(t) = E_{\boldsymbol{x}}(t) * f_{\boldsymbol{T}}(t)\,, \end{aligned} \tag{20}$$

where "*" denotes the linear convolution. Thus, the expected value of the output is just the expected value of the input convolved with the pdf of the delay, whereas the noise power remains unchanged.

If this signal is now passed through the nonlinear transfer charactersitic, the function $E_z(t)$ is obtained, where $\boldsymbol{z}(\eta,t)$ is the output random process of our model inverter:

$$\begin{aligned} E_{\boldsymbol{z}}(t) \;&=\; \int_{-\infty}^{x_t} f_{\boldsymbol{y}}(y,t)dy \\ &=\; F_{\boldsymbol{n}}(x_t)\left(1 - E_{\boldsymbol{y}}(t)\right) + F_{\boldsymbol{n}}(x_t - 1)E_{\boldsymbol{y}}(t) \end{aligned} \tag{21}$$

Things become more complicated in the case of the NAND and the NOR gate. This is because the output of the *min-* and *max-operator* cannot be expressed by Eq. (17). Thus, we will derive the output of these gates the following way: The output pdf, $f_{\boldsymbol{x}}(x,t)$, of the *min-* and *max-operator* is derived as a function of $N_{\tilde{\boldsymbol{u}}}$, $N_{\tilde{\boldsymbol{v}}}$, $E_{\tilde{\boldsymbol{u}}}$ and $E_{\tilde{\boldsymbol{v}}}$, where $\tilde{\boldsymbol{u}}(\eta,t)$ and $\tilde{\boldsymbol{v}}(\eta,t)$ are the input signals to the *min-* and *max-operator*, respectively. The function E_z for the output of the entire gate can than be derived from $f_{\boldsymbol{x}}(x,t)$.

For the output's pdf of the *max-operator* arises from Eq. (10):

$$\begin{aligned} f_{\boldsymbol{x}}(x,t) \;=\; &\left[f_{\boldsymbol{n}\tilde{\boldsymbol{u}}}(x)(1 - E_{\tilde{\boldsymbol{u}}}(t)) + f_{\boldsymbol{n}\tilde{\boldsymbol{u}}}(x-1)E_{\tilde{\boldsymbol{u}}}(t)\right] \\ &\times\left[F_{\boldsymbol{n}\tilde{\boldsymbol{v}}}(x)(1 - E_{\tilde{\boldsymbol{v}}}(t)) + F_{\boldsymbol{n}\tilde{\boldsymbol{v}}}(x-1)E_{\tilde{\boldsymbol{v}}}(t)\right] \\ &+\left[f_{\boldsymbol{n}\tilde{\boldsymbol{v}}}(x)(1 - E_{\tilde{\boldsymbol{v}}}(t)) + f_{\boldsymbol{n}\tilde{\boldsymbol{v}}}(x-1)E_{\tilde{\boldsymbol{v}}}(t)\right] \\ &\times\left[F_{\boldsymbol{n}\tilde{\boldsymbol{u}}}(x)(1 - E_{\tilde{\boldsymbol{u}}}(t)) + F_{\boldsymbol{n}\tilde{\boldsymbol{u}}}(x-1)E_{\tilde{\boldsymbol{u}}}(t)\right] \end{aligned} \tag{22}$$

From that result, the function E_z for the output of the entire NOR gate can be derived:

$$\begin{aligned} E_{\boldsymbol{z}}(t) \;=\; &\int_{-\infty}^{x_t} f_{\boldsymbol{x}}(x,t)dx = (1 - E_{\tilde{\boldsymbol{u}}})(1 - E_{\tilde{\boldsymbol{v}}})\alpha_{\tilde{\boldsymbol{u}}\tilde{\boldsymbol{v}}} \\ &+E_{\tilde{\boldsymbol{u}}}(1 - E_{\tilde{\boldsymbol{v}}})\beta_{\tilde{\boldsymbol{u}}\tilde{\boldsymbol{v}}} + (1 - E_{\tilde{\boldsymbol{u}}})E_{\tilde{\boldsymbol{v}}}\gamma_{\tilde{\boldsymbol{u}}\tilde{\boldsymbol{v}}} + E_{\tilde{\boldsymbol{u}}}E_{\tilde{\boldsymbol{v}}}\delta_{\tilde{\boldsymbol{u}}\tilde{\boldsymbol{v}}}, \end{aligned} \tag{23}$$

where the constants $\alpha_{\tilde{u}\tilde{v}}$, $\beta_{\tilde{u}\tilde{v}}$, $\gamma_{\tilde{u}\tilde{v}}$ and $\delta_{\tilde{u}\tilde{v}}$ are given by:

$$\alpha_{\tilde{u}\tilde{v}} = \int_{-\infty}^{x_t} f_{n\tilde{u}}(x)F_{n\tilde{v}}(x) + f_{n\tilde{v}}(x)F_{n\tilde{u}}(x)dx$$

$$\beta_{\tilde{u}\tilde{v}} = \int_{-\infty}^{x_t} f_{n\tilde{u}}(x-1)F_{n\tilde{v}}(x) + f_{n\tilde{v}}(x)F_{n\tilde{u}}(x-1)dx$$

$$\gamma_{\tilde{u}\tilde{v}} = \int_{-\infty}^{x_t} f_{n\tilde{u}}(x)F_{n\tilde{v}}(x-1) + f_{n\tilde{v}}(x-1)F_{n\tilde{u}}(x)dx$$

$$\delta_{\tilde{u}\tilde{v}} = \int_{-\infty}^{x_t} f_{n\tilde{u}}(x-1)F_{n\tilde{v}}(x-1) + f_{n\tilde{v}}(x-1)F_{n\tilde{u}}(x-1)dx.$$

Accordingly, the function E_z for the output of the NAND gate is also given by Eq. (23), when $\alpha_{\tilde{u}\tilde{v}}$ is replaced by $\hat{\alpha}_{\tilde{u}\tilde{v}}$, $\beta_{\tilde{u}\tilde{v}}$ by $\hat{\beta}_{\tilde{u}\tilde{v}}$ and so on. Here, the constants $\hat{\alpha}_{\tilde{u}\tilde{v}}$, $\hat{\beta}_{\tilde{u}\tilde{v}}$, ... follow the same definition as $\alpha_{\tilde{u}\tilde{v}}$, $\beta_{\tilde{u}\tilde{v}}$, ... but with $F_{n\tilde{u}}(x)$ replaced by $(1-F_{n\tilde{u}}(x))$ and $F_{n\tilde{v}}(x)$ by $(1-F_{n\tilde{v}}(x))$, respectively.

These results merge into classical Boolean logic, when no noise is present and the functions $E_{\tilde{u}}$ and $E_{\tilde{v}}$ take the (constant) value '0' or '1', respectively. In this case holds: $\alpha_{\tilde{u}\tilde{v}} = 1$, $\beta_{\tilde{u}\tilde{v}} = \gamma_{\tilde{u}\tilde{v}} = \delta_{\tilde{u}\tilde{v}} = 0$ and $\hat{\alpha}_{\tilde{u}\tilde{v}} = \hat{\beta}_{\tilde{u}\tilde{v}} = \hat{\gamma}_{\tilde{u}\tilde{v}} = 1$, $\hat{\delta}_{\tilde{u}\tilde{v}} = 0$. The output of the NOR gate is then given by $E_z = (1-E_{\tilde{u}})(1-E_{\tilde{v}})$ and for the output of the NAND gate holds accordingly $E_z = (1-E_{\tilde{u}})(1-E_{\tilde{v}}) + E_{\tilde{u}}(1-E_{\tilde{v}}) + (1-E_{\tilde{u}})E_{\tilde{v}}$.

The preceding results can consequently be summerized as follows: Each signal at the ouput of a model of a Boolean gate is described by one parameter, the power N_x of the additive noise at the gates output which reflects the corrution of the signal due to (thermal) noise, and the time dependent expected value E_x which reflects the average change of the signal over time. This function also incoperates the uncertainty of the time instance when the signal changes its state.

Analyzing Boolean network is now performed the following way: The input signals are represented as explained above. These signals are then propagated from gate to gate through the network. This is very easy for the noise power because this only depends on the outout of the gate under consideration. The main task encompasses the propagation of the function E_x.

As can be seen from Eq. (21) and Eq. (23), the expected value function(s) of the input(s) is weighted with certain constants which can be determined either analytically or, if this is not possible or desirable, by means of numerical integration. In addition, algebraic operations are performed with the input functions. These operations are collected in a special data type together with the corresponding constants. Thus, after performing this kind of analysis, the pdf of each signal in the Boolean network is known implicitly. From that, many properties of the signals of interest can be derived by evaluating the corresponding data structure. Thus, it is e. g. possible to derive the probability of error at a certain time instance, or the average error probability, or the expected value at a certain time instance, etc. These results can subsequently be used to both analyze and optimize the circuits reliability and timing properties.

4. Experimental Results

We applied our theory to a model NAND gate as depicted in Fig. 2. The inputs have been chosen to be a Heaviside function and a shifted Heaviside function, respectively. That is, the first input changes its state from '0' to '1' at $t = 0$ whereas the second input performs the same transition at $t = 1$.

Each of these signals is corrupted by additive white Gaussian noise with noise power $N_u = 0.1$ and $N_v = 0.2$, respectively, followed by passing the signals through random delays. Both random delay elements are statistical independent and Gaussian distributed with mean $\mu_{T_u} = 0.1$ and $\mu_{T_v} = 0.2$ as well as a standard deviation of $\sigma_{T_u} = \sigma_{T_v} = 0.01$, respectively.

The threshold of the subsequent nonlinear transfer characteristic has been chosen to be $x_t = 0.5$ and the power of the output noise is given by $N_z = 0.04$.

This operation has been performed by two different methods. In the first place, we derived the pdf of the output by the methods described in this paper especially in section 3. Secondly, the statistics of the output have been derived using the straight forward way: The input signals are represented by vectors of samples to which the corresponding noise vectors are added. Each resulting vector is delayed by a random number of samples and the minimum is derived on a sample by sample basis. Finally, the elements of the accrued vector are either set to '0' or to '1' depending on if the element is greater or less than $x_t = 0.5$. This procdure is repeated for 10000 times and the output pdf $f_z(z,t)$ can finally be estimated by determining a time dependent histogram. The calculated and the estimated pdf of the output are depicted in Fig. 3a and Fig. 3b, respectively.

The expected value $E_z(t)$ can also be estimated by averaging the result for each time instance. This is shown in Fig. 4. The solid (blue) line represents the estimated expected value derived by conventional simulation methods whereas the dashed line (red) is determined from Eq. (23).

5. Conclusions and Future Work

In this paper an approach for the statistical analysis of combinatorial circuits is presented taking into account both timing uncertainty and noise. This is especially important for emerging technologies which are expected to be very

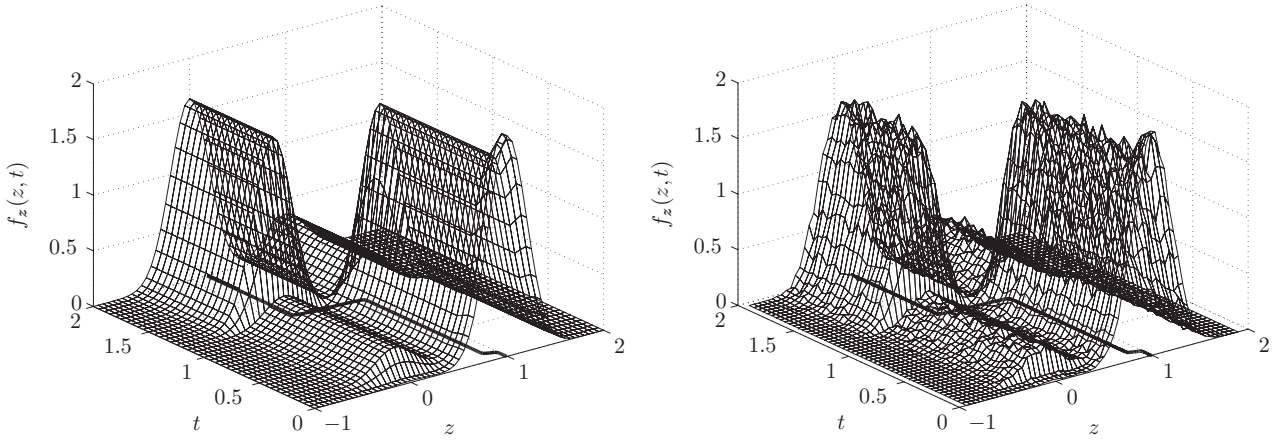

Figure 3. Pdf of output signal derived (a) analytically and (b) simulated.

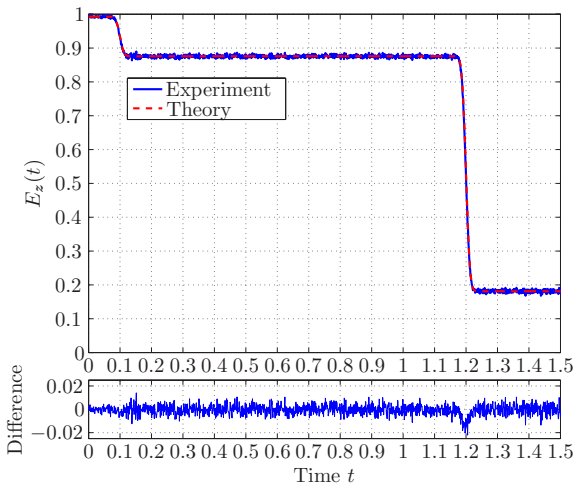

Figure 4. Comparison between analytical solution and simulation results.

sensitive to disturbances and noise and to be subject to process variations. The presented theoretical models make no restriction to correlation between signals and the shape of nonlinear transfer characteristics of the combinatorial gates except that the latter have to be monotonic decreasing within a certain interval. The model is simplified by choosing a certain type of this characteristic and assuming that all signals are statistical independent. This simplified model is applied to a sample gate and compared with conventional statistical analysis resulting in perfect agreement.

The future work includes the comparison of the results obtained by the model gates used in this work with that achieved with real logic circuits of different technologies. In addition, a method has to be developed to deal with correlation between signals. Even though this is already included in the general theory the required joint pdf are usually not known in practice. Thus a method is needed to either propagate them through the network or model the network in a manner that the assumption of statistical independence can be applied.

References

[1] R. I. Bahar, J. Mundy, and J. Chen. A Probabilistic-Based Design Methodology for Nanoscale Computation. In *IEEE/ACM International Conference on Computer Aided Design (ICCAD'03)*, 2003.

[2] M. Breuer, S. Gupta, and T. Mak. Defect and Error Tolerance in the Presence of Massive Number of Defects. *IEEE Design and Test of Computers*, pages 216–227, May–June 2004.

[3] H. Chang, V. Zolotov, S. Narayan, and C. Visweswariah. Parameterized Block-Based Statistical Timing Analysis with Non-Gaussian Parameters, Nonlinear Delay Functions. In *Proc. of 42th Design Automation Conference (DAC'05)*, 2005.

[4] A. Devgan and C. Kashyap. Block-Based Static Timing Analysis with Uncertainty. In *IEEE/ACM International Conference on Computer Aided Design (ICCAD'03)*, 2003.

[5] E. Hänsler. *Statistische Signale – Grundlagen und Anwendungen*. Springer Verlag, 1997.

[6] J. von Neumann. Probabilistic Logics and the Synthesis of Reliable Organisms from Unreliable Components. In C. E. Shannon and J. McCarthy, editors, *Automata Studies*, pages 43–98. Princeton University Press, 1956.