

Modeling Multiple Input Switching of CMOS Gates in DSM Technology Using HDMR

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Abstract—Continuing scaling of CMOS technology has allowed aggressive pursuit of increased clock rate in DSM chips. The ever shorter clock period has made switching times of different inputs on a logic gate ever closer to each other. The traditional method of static timing analysis assuming single input switching is no longer adequate enough to capture gate level delays accurately. Gate delay models considering multiple input switching are needed for DSM chips. We propose a new method of systematically modeling gate delays using the high dimensional model representation (HDMR) method. The proposed method models gate delays with respect to the relative signal arrival times (RSAT) of its inputs. The systematic nature of the proposed algorithm allows gate delay characterization with more inputs switching close to each other. This paper will show, for the first time, gate delay models of up to 5 inputs. In addition, the proposed model is extended to allow the input signal slope and process variations to be taken into account for statistical static timing analysis. Our results show that the proposed HDMR model gives an error between 2.2% to 12.9% for a variety of static and dynamic logic gates as compared to SPICE results, depending on the number of inputs involved in switching.

I. INTRODUCTION

Static Timing Analysis (STA) is a crucial part of the modern VLSI chip design process because it is fast and maintains a relatively high accuracy compared to dynamic timing simulations such as SPICE. When calculating the delay from input to output of a given circuit, STA assumes that all the side inputs are at their non-controlling values. This assumption has made the overall STA methodology much simpler to handle complex VLSI chip designs, while not causing significant errors in gate level delay modeling. However, continuing scaling of CMOS technology has allowed aggressive pursuit of increased clock rate in DSM chips beyond 90nm. The ever shorter clock period has made switching times of different inputs on a logic gate ever closer to each other. When multiple inputs switch simultaneously or close to each other, the gate delay can increase or decrease significantly compared to that of single input switching. A preliminary study in [1] showed up to 20% error using a single input switching model when modeling gate delays with multiple input switching.

With CMOS process technology moving towards 65nm and beyond, precise control of critical dimensions and process parameters such as transistor channel length and channel doping density is becoming difficult. Small changes in transistor channel length and channel doping density can cause a more dramatic change in transistor behavior compared to older technologies. Therefore, process variations in DSM technology have become a matter of concern. ITRS [2] predicts aggressive scaling down of gate length, transistor threshold voltage and

oxide thickness to meet the growing demands for performance. Such scaling will result in large variability in threshold voltage both within and across dies. It is well known [3][4] that gate length, channel doping density, and oxide thickness are some of the key parameters whose variation can have significant impact on circuit performance. The conventional method to deal with process variations in the past was to consider design corners. When process variations were not severe and there are plenty design margins, such a method can alleviate design uncertainties while not compromising the overall goals of performance, power consumption, quality, and time-to-market. However, with increasing leakage power and process variations and shrinking design margins, competing design requirements such as performance and power consumption can no longer be met simultaneously under any conventional design corner scenarios. Recent designs tend to fudge the design corners to "fit" the designs in a predetermined design goal. It is widely believed [3] [5] [6] that the use of statistical analysis and design techniques is crucial for future chip designs to fundamentally accommodate design uncertainty in the design flow. One of the important aspects of delay modeling for STA as well as static statistical timing analysis (SSTA) is to incorporate multiple input switching (MIS) in the delay models to improve the accuracy of existing gate delay models.

The delay of a gate depends upon the relative signal arrival time (RSAT) of all of its input signals. If the input signal arrival times of different inputs are far apart, the existing single input switching models predict the delay accurately. This can be illustrated by the example of a two input NAND gate shown in Figure 1(a). Figure 2(a) shows SPICE simulations of the NAND gate delay with different RSATs in a $0.18\mu m$ CMOS process. The delay increases when both inputs having falling transitions and with an increasing difference in their RSATs. This happens because the pMOS transistors go into saturation one after the other when there is a difference in arrival times. When inputs are falling at the same time, the output is charged through multiple pMOS transistors that go into saturation. The delay decreases when both inputs have rising transitions and with an increasing difference in arrival times. This is because one of the nMOS transistors can get into the saturation earlier than the other transistor to allow increased driving current when the pull-down tree finally turns on.

Figure 2(b) shows the gate delay variation under MIS for a complex gate shown in Figure 1(b). Each curve in Figure 2(b) represents two out of the three inputs switching with varying relative switching time. The simulation results show significantly different delays with different RSATs. These results reinforce the importance of incorporating multiple input

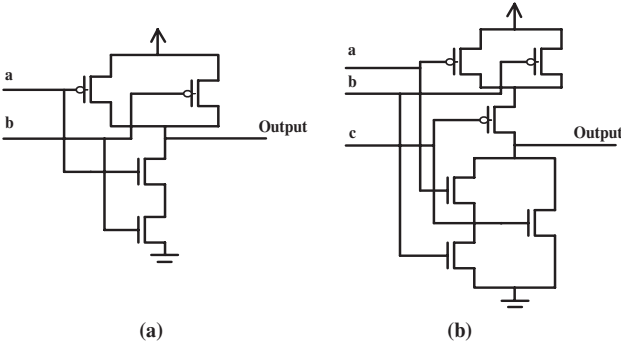


Fig. 1. (a) a NAND gate and (b) a Complex CMOS gate

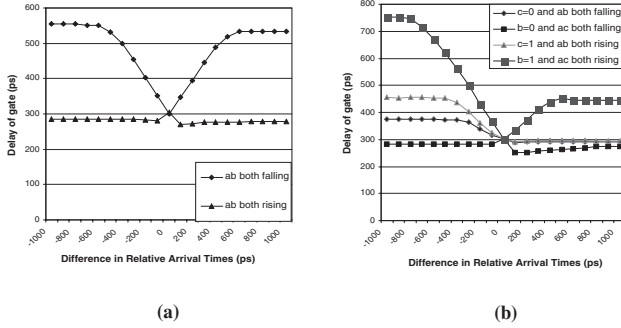


Fig. 2. Effect of RSATs on delay for (a) a NAND and (b) a complex gate

switching in gate delay models.

Most existing research in statistical timing [7], [5], [6], [8], [9], [10] deal with modeling statistical behavior of transistors, gates, and interconnects to derive analytically the delay variations of signal paths in a given circuit. However, when dealing with statistical gate delay modeling, most of the existing work derive the gate delay variability based on the Prob(max(a, b)) formulation which is based on the timing of the latest arrival input. Thus, most of the existing research in statistical timing failed to consider multiple input switching. Earlier attempts by Nabavi [11] and Young [12] to model gate delays with MIS focused on reducing circuits to a basic inverter and then approximated the delay as a product of polynomials of input waveform slope, output loading capacitance and device configuration ratio. This procedure can be proven to be very complicated for complex logic blocks. More recently, Agarwal et.al. [1] attempted to address the issue of SSTA of gates including the multiple input switching effect. In their proposed model, gate delay variations due to transistor gate length variation were considered. Using a 2-input gate, an analytical model was proposed. The extension of the approach for higher fan-in gates was discussed by applying the 2-input gate model iteratively. However, the approach in [1] only produces arrival time pdfs along a signal path. It is not suitable for conventional static timing analysis. In addition, it is not clear how scalable this approach is for higher fan-in gates. [13] uses orthogonal polynomial based PCM method to construct a delay equation from the circuit timing performance to solve for process variations and multiple input switching. Both models in [1] and [13] do not consider the impact of

slope variations. With increasing process variation, input slope variations can significantly contribute to overall gate delay variations. In addition, the results presented in [1] and [13] only showed no more than 3 inputs simultaneous switching. The ability of the proposed models in [1] and [13] to handle more than 3 switching inputs was not discussed.

We present a new modeling method for gate delays using the high dimensional model representation (HDMR) approach [14]. Our goal is to provide a more systematic approach to gate delay modeling that allows 1) proper capturing of MIS in the delay model extending it to capture process variations in static and dynamic logic circuits, 2) better scalability to high fan-in gates, 3) natural extension to SSTA in terms of providing standard deviations of gate delays, and 4) incorporation of input slope and process variations in the delay model.

The HDMR approach provides a complexity of $O(n^2)$ where n is the number of samples needed to build the HDMR model. The systematic nature of the HDMR method allows better handling of high fan-in gates. Deriving statistical information from the HDMR models is a straightforward extension of the conventional HDMR models. Therefore, the proposed HDMR method not only can be used for conventional gate level STA, but also be used for SSTA. The proposed method can be an integral part of the library characterization process. Our results show that the proposed HDMR model gives an error of 2.2% to 12.9% for several static and dynamic logic gates, with up to 5-inputs, depending on the number of inputs and the number of variation sources to be included.

The remainder of the paper is organized as follows. Section II provides some background information about HDMR. Section III illustrates the details of the proposed gate level delay models using HDMR. Section IV presents the simulation results using the proposed approach. Concluding remarks and discussions are given in Section V.

II. BACKGROUND

HDMR [14], [15], [16] is a general set of quantitative model assessment and analysis tools for capturing high-dimensional input-output system behavior. HDMR can be applied to a variety of modeling building applications such as constitution of a computational model directly from *lab/field* data, creating an efficient fully equivalent operational model for existing mathematical model, identification of key model variables, etc. Let the input variables be

$$X = (x_1, x_2, \dots, x_n), \quad (1)$$

where n is the number of inputs. Let $f(Y)$ be the output. HDMR expresses the model output as a finite hierarchical cooperative expansion in terms of its input variables:

$$f(Y) = f_0 + \sum_{i=1}^n f_i(x_i) + \sum_{1 \leq i < j \leq n} f_{ij}(x_i, x_j) + \sum_{1 \leq i_1 < \dots < i_l \leq n} f_{i_1 i_2 \dots i_l}(x_{i_1}, x_{i_2}, \dots, x_{i_l}) + \dots + f_{1,2,\dots,n}(x_1, x_2, \dots, x_n) \quad (2)$$

where

$$f_0 = f(\bar{x}) \quad (3)$$

$$f_i(x_i) = f(x_i, \bar{x}^i) - f_0 \quad (4)$$

$$f_{ij}(x_i, x_j) = f(x_i, x_j, \bar{x}^{ij}) - f_i - f_j - f_0 \quad (5)$$

The zeroth order component function in Equation 3 denotes the mean value of $f(Y)$ at a reference point given by:

$$\bar{x} = (\bar{x}_1, \bar{x}_2, \dots, \bar{x}_n)$$

The first order term, in Equation 4 captures the effect of any input variable on the output function $f(Y)$, keeping the remaining variables at their reference point. Thus, the higher order terms indicate the cooperative effects of the increasing number of input variables on the output function. One of the important properties of HDMR is that it produces optimum functions $f_0, f_i(x_i), f_{ij}(x_i, x_j), \dots$ that can be fitted to a given $f(x)$ over the entire desired domain Ω of x .

HDMR can also be viewed as Sobol's decomposition of function $f(Y)$ [17]. That is

$$\begin{aligned} f_i(x_i) &= f(E(Y|x_i)) \\ f_{ij}(x_i, x_j) &= f(E(Y|x_i, x_j)) - f(x_i) - f(x_j) \\ &\dots \end{aligned} \quad (6)$$

When $i=j$, $f_{ij}(x_i, x_j)$ reduces to $f_i(x_i)$. Therefore, there is no explicit x_i^2 terms in the second order terms.

There are two types of HDMR methods, Cut-HDMR and RS-HDMR. Cut-HDMR is generally constructed when ordered sampling for output $f(Y)$ at chosen points of x is possible. This is more suitable when lab data is available. For RS-HDMR, the component functions are determined through an averaging process on a set of randomly sampled points over the entire domain Ω . In Cut-HDMR, the reference point can be a randomly chosen point which is a contrast to RS-HDMR, where f_0 is the average value of $f(Y)$ over the whole domain. Cut-HDMR saves a huge amount of sampling, that is otherwise necessary. It converts an exponential amount of sampling to a polynomial amount of sampling. On the other hand, RS-HDMR requires a large amount of random sampling for the determination of the component functions at different values by Monte Carlo integration. The complexity of RS-HDMR increases by the factor of the integrals, that is required for the computation of its component functions. Therefore, Cut-HDMR is chosen in our proposed approach. Moreover, Cut-HDMR is also more appropriate in terms of ordered sampling, which suits our application, where we want to cover the entire space in an orderly manner to obtain exact delay variations.

III. GATE DELAY MODELING USING HDMR

The proposed HDMR model for gate delays is based on RSAT between a pair of signals. For a logic gate with n inputs, a signal is chosen as the anchoring signal and rest of the signals are associated with the anchoring signal to form pairs of RSATs. Let X be the set of independent pairs of RSATs, signal 'o' be the anchoring signal, and signals i, j, p, \dots are the remaining signals, i.e.

$$X = \{t_{rsat,oi}, t_{rsat,oj}, t_{rsat,op}, \dots\} \quad (7)$$

For simplicity, the anchoring signal will be omitted from RSATs in the remaining part of this paper. Therefore the input variables can be written as:

$$X = \{t_{rsat,i}, t_{rsat,j}, t_{rsat,p}, \dots\} \quad (8)$$

This set of RSATs can capture any combinations of input signal arrival times, and, therefore, forms the basis variables in the proposed HDMR model. For example, a 4-input gate with inputs a, b, c , and d will have three RSATs with input a being the anchoring input, namely, $t_{rsat,b}$, $t_{rsat,c}$, and $t_{rsat,d}$. Using the Cut-HDMR method to build the model, a reference point of RSAT=0 for all the input signal pairs is chosen as the starting point. The gate delay at this reference point can be obtained using SPICE. In the process of building a model, the RSATs between each pair is varied. For the model to capture the individual effect of RSAT between a given pair of input signals, $F_i(t_{rsat,i})$, the RSAT related to this pair of signals is varied discretely while keeping all the remaining RSATs among other signals at their reference value. This will generate new points on a "cut" line with f_i being the i^{th} sample along a cut line and $F_i(t_{rsat,i})$ being the i^{th} sample along the cut line for input pair between input i and the anchoring input. A SPICE simulation is performed under each point on a cut line to obtain the gate delay under the given set of RSATs. The cooperative effect of two RSATs, $F_{i,j}(t_{rsat,i}, t_{rsat,j})$, can be included in the HDMR model in a similar way by varying two RSATs in an ordered manner while keeping the remaining points at their reference points. These are referred to as *the second order terms*. This process is repeated to include all the RSATs for a gate. We believe, and our results confirm, that a HDMR model including up to second order terms is sufficient to capture the non-linear dynamics of CMOS gate delay. The resulting HDMR equation is given by:

$$\begin{aligned} F(Y) &= F_0 + \sum_i F_i(t_{rsat,i}) \\ &+ \sum_{1 \leq i < j} F_{i,j}(t_{rsat,i}, t_{rsat,j}) \end{aligned} \quad (9)$$

where,

$$F_i(t_{rsat,i}) = f_i(t_{rsat,i}) - F_0 \quad (10)$$

$$\begin{aligned} F_{i,j}(t_{rsat,i}, t_{rsat,j}) &= f_{i,j}(t_{rsat,i}, t_{rsat,j}) - f_i(t_{rsat,i}) \\ &- f_j(t_{rsat,j}) - F_0 \end{aligned} \quad (11)$$

Each term in the HDMR model in Equation 9 is a set of discrete simulation points of gate delays along a cut line minus the mean value F_0 . This set of delay values can be stored in a form of look-up table. Figure 3 shows the look-up table for second order components $t_{rsat,b}, t_{rsat,c}$ with input "a" being the anchoring input, for the complex gate shown in Figure 1(b). The load capacitance and the input signal slope are fixed in this case. The graph shows the various delay values for respective variations in RSATs. To reduce the amount of memory storage, the look-up tables can be reduced to analytical equations using the response surface method [18] as shown in Equations 12,13,14,15 for the complex gate in Figure 1(b). This process

can be part of the library characterization process to model the gate delay by considering multiple input switching.

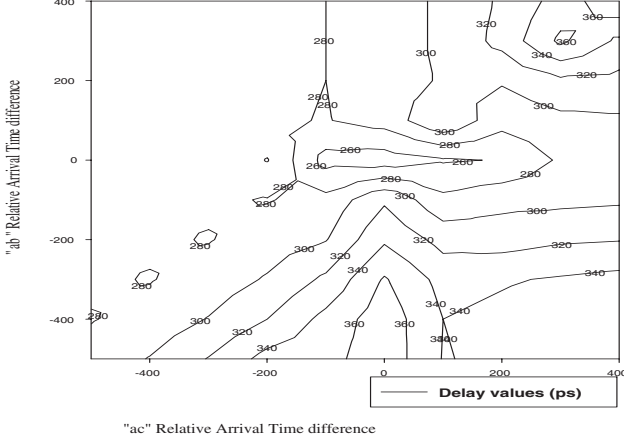


Fig. 3. Look-up table for a 2nd-order RSAT term in an HDMR model

$$F_0 = 301.05 \quad (12)$$

$$F_b(t_{rsat,b}) = 7.8 - 0.14t_{rsat,b} + 0.000234t_{rsat,b}^2 \quad (13)$$

$$F_c(t_{rsat,c}) = 10.38 - 0.095t_{rsat,c} - 0.000451t_{rsat,c}^2 \quad (14)$$

$$F_{b,c}(t_{rsat,b}, t_{rsat,c}) = 6.78 - 0.12t_{rsat,b} + 0.09t_{rsat,c} - 0.000115t_{rsat,b}^2 - 0.000143t_{rsat,c}^2 - 0.000274t_{rsat,b}t_{rsat,c} \quad (15)$$

$$F(X) = F_0 + F_b(t_{rsat,b}) + F_c(t_{rsat,c}) + F_{b,c}(t_{rsat,b}, t_{rsat,c}) \quad (16)$$

We will use the same process to include other parameters, such as input slope and load capacitance, in the HDMR model. We also extend the model to capture the effect of process variations such as channel length. Let $t_{r/f,i}$ be the rise/fall time of the i^{th} input; C_L be the load capacitance at the output; and $L_{eff,n}$ be the effective channel length of the n^{th} transistor. Equation 17 shows the HDMR model that includes the other parameters. The process of building the HDMR model shown in Equation 17 to include more parameters is similar to that described earlier.

To apply the proposed method to SSTA, a set of RSATs for a given gate is randomly generated. We assume that the statistical characteristics of the input signals are known. Therefore, the randomly generated RSATs must conform to the input's statistical characteristics. The statistical characteristics

of gate delays can then be derived by evaluating gate delays with the HDMR model using randomly generated RSAT samples and by extracting the standard deviation from the gate delay values. Compared to circuit-level Monte Carlo simulations, this approach is much faster. This process can be easily extended to the model in Equation 17 by including random inputs with respect to input slope, load capacitance and process parameters, such as L_{eff} .

$$\begin{aligned} F(X) = & F_0 + \sum_i F_i(t_{r/f,i}) + \sum_i F_i(t_{rsat,i}) + F(C_L) \\ & + \sum_n F_n(L_{eff,n}) + \sum_{1 \leq i < j} F_{i,j}(t_{r/f,i}, t_{r/f,j}) \\ & + \sum_i F_i(t_{r/f,i}, C_L) + \sum_{1 \leq i < j} F_{i,j}(t_{r/f,i}, t_{rsat,j}) \\ & + \sum_i F_i(C_L, t_{rsat,i}) + \sum_{1 \leq i < j} F_{i,j}(t_{rsat,i}, t_{rsat,j}) \\ & + \sum_i \sum_n F_{i,n}(L_{eff,n}, t_{r/f,i}) + \sum_n F_n(L_{eff,n}, C_L) \\ & + \sum_i \sum_n F_{i,n}(L_{eff,n}, t_{rsat,i}) \end{aligned} \quad (17)$$

where,

$$F_i(t_{r/f,i}) = f_i(t_{r/f,i}) - F_0 \quad (18)$$

$$F(C_L) = f(C_L) - F_0 \quad (19)$$

$$F_i(t_{rsat,i}) = f_i(t_{rsat,i}) - F_0 \quad (20)$$

$$F_n(L_{eff,n}) = f_n(L_{eff,n}) - F_0 \quad (21)$$

$$F_{i,j}(t_{r/f,i}, t_{r/f,j}) = f_{i,j}(t_{r/f,i}, t_{r/f,j}) - f_i(t_{r/f,i}) - f_j(t_{r/f,j}) - F_0 \quad (22)$$

$$F_i(t_{r/f,i}, C_L) = f_i(t_{r/f,i}, C_L) - f_i(t_{r/f,i}) - f(C_L) - F_0 \quad (23)$$

$$F_{i,j}(t_{r/f,i}, t_{rsat,j}) = f_{i,j}(t_{r/f,i}, t_{rsat,j}) - f_i(t_{r/f,i}) - f_j(t_{rsat,j}) - F_0 \quad (24)$$

$$F_i(C_L, t_{rsat,i}) = f_i(C_L, t_{rsat,i}) - f(C_L) - f_i(t_{rsat,i}) - F_0 \quad (25)$$

$$F_{i,j}(t_{rsat,i}, t_{rsat,j}) = f_{i,j}(t_{rsat,i}, t_{rsat,j}) - f_i(t_{rsat,i}) - f_j(t_{rsat,j}) - F_0 \quad (26)$$

$$F_{i,n}(L_{eff,n}, t_{rsat,i}) = f_{i,n}(L_{eff,n}, t_{rsat,i}) - f_i(t_{rsat,i}) - f_n(L_{eff,n}) - F_0 \quad (27)$$

$$F_{i,n}(L_{eff,n}, t_{r/f,i}) = f_{i,n}(L_{eff,n}, t_{r/f,i}) - f_n(L_{eff,n}) - f_i(t_{r/f,i}) - F_0 \quad (28)$$

$$F_n(L_{eff,n}, C_L) = f_n(L_{eff,n}, C_L) - f_n(L_{eff,n}) - f(C_L) - F_0 \quad (29)$$

IV. SIMULATION AND RESULTS

The proposed model was implemented on a set of static and dynamic logic gates in a commercial $0.18\mu m$ CMOS process. At each point on the cut line, a SPICE simulation was performed to obtain gate delay. The input waveform to each gate in the SPICE simulations was generated by a CMOS driver to produce a realistic waveform shape. The arrival time of the input to the CMOS driver was varied to produce variations of the input arrival time at the gate to be modeled. The maximum range for RSAT changes that has an effect on the output delay was observed to be ± 500 ps. The capacitance at each input of the gate that was used to obtain slope variations was varied from 10fF to 150fF. In order to capture process variations we varied the effective channel length of each transistor in the circuit with a standard deviation of 3% of the nominal channel length. The load capacitance for each logic gate is fixed at 100fF. A sample size of 100 points for the 1st-order terms and 10 points for the 2nd-order terms was chosen to effectively capture the input variation without taking too much computation time. The 10-point sample size for the 2nd-order terms will give a total of 100 cooperative sampling points for each 2nd-order term. Table I lists all the gates including the number of inputs along with their Boolean functions for both static and dynamic logic.

We examine the accuracy of the proposed HDMR models in the context of STA. When using the HDMR models for SSTA, the straightforward approach is to use the input arrival time and slope pdfs to generate random inputs accordingly, assuming the arrival time and slope pdfs at the inputs are known. The gate delay pdf can be obtained numerically by evaluating the random inputs on the HDMR models. For each gate, two sets of HDMR models were built, one without considering the effect of input slope and variations in channel length, and the other considering the effect of input slope and channel length variations. This is intended to determine the impact of input slope and process variations on the gate delay and its variations. The delay values from the HDMR models are compared with those obtained through SPICE simulations. Tables II and III show the percentage errors of 1000 random samples produced by the HDMR models compared to the SPICE simulations for static and dynamic logic, respectively. It is clear that there is a significant reduction in the amount of error when the effect of input slope is considered.

To validate the HDMR models for SSTA, a 1000-point Monte-Carlo simulations were performed using the HDMR models for all the logic gates listed in Table I. The parameters varying in the Monte-Carlo simulations include L_{eff} , input signal slope, and RSAT. The standard deviations from the

HDMR models were compared to those obtained from SPICE-based Monte-Carlo simulations to obtain the errors. Tables IV and V show average percentage error of standard deviations for the HDMR models where the effect of input slope and process variations is compared. A similar trend as in Tables II and III can be observed in Tables IV and V, that the models show significantly better accuracy when considering input slope and process variations. Overall, the percentage errors of the HDMR models range from 2.2% for the 2-input gates to 12.9% for the 5-input gates and the overall standard deviation error for the proposed HDMR model ranges from 2.2% for a 2-input gate to 12.5% for a 5-input gate.

The results show an increase in error from 2-input to 5-input gates. However, it is worth noting that this is the first time the delay of a 5-input gate has been modeled. The overall error under 13% is a significant improvement over the potential errors of over 20% in the existing static timing analysis for significantly simpler circuits where only single input switching is considered. Moreover, the error for the 2-input gates in using our models is smaller compared to [13] of 5.29%.

TABLE I
LOGIC GATES USED TO BUILD HDMR MODELS

Gate	No. of inputs	logic function (static logic)	logic function (dynamic logic)
C1	2	$A + B$	$A + B$
C2	2	$A + B$	\overline{AB}
C3	2	\overline{AB}	\overline{AB}
C4	3	ABC	$\overline{AB + C}$
C5	3	$\overline{A + B + C}$	$\overline{(A + B)C}$
C6	3	$\overline{AB + C}$	$\overline{AC + B}$
C7	4	$\overline{A + B(C + D)}$	$\overline{AB + CD}$
C8	4	\overline{ABCD}	$\overline{A + BCD}$
C9	4	$\overline{A(BC + D)}$	$\overline{ABC + D}$
C10	5	\overline{ABCDE}	$\overline{ABC + DE}$
C11	5	$\overline{A + BCDE}$	$\overline{AB + CDE}$
C12	5	$\overline{(A + BCD)E}$	\overline{ABCDE}

TABLE II
PERCENTAGE ERROR OF GATE DELAY FOR STATIC CMOS GATES

Gate	Model with RSAT, w/o slope	Model with RSAT and slope
C1	10.67	2.3
C2	9.98	2.16
C3	8.82	2.75
C4	7.74	4.55
C5	10.48	5.65
C6	10.4	7.92
C7	16.75	8.93
C8	8.9	6.6
C9	16.99	8.44
C10	17.7	9.21
C11	21.4	8.38
C12	17.5	9.15

V. CONCLUSIONS AND DISCUSSIONS

We presented a novel method of modeling multiple input switching of CMOS gates using the HDMR modeling approach. The proposed method provides a systematic approach

TABLE III

PERCENTAGE ERROR OF GATE DELAY FOR DYNAMIC LOGIC

Gate	Model with RSAT, w/o slope	Model with RSAT and slope
C1	11.06	3.45
C2	15.06	4.72
C3	10.8	4.04
C4	16.2	7.62
C5	17.4	7.7
C6	17.16	7.06
C7	15.45	8.34
C8	16.23	9.21
C9	11.39	8.85
C10	17.82	12.9
C11	18.32	12.59
C12	16.32	10.01

TABLE IV

STANDARD DEVIATION ERROR OF GATE DELAY FOR STATIC LOGIC

	Model with RSAT, w/o slope and Leff	Model with RSAT, slope and Leff
C1	60.47	2.3
C2	90.7	2.2
C3	59.9	3.16
C4	63.8	7.10
C5	48.8	3.85
C6	63.7	6.75
C7	51.1	5.9
C8	25.8	5.93
C9	44.9	7.4
C10	71.6	8.92
C11	56.6	9.54
C12	59.7	7.5

to characterize gate delays considering the multiple input switching, slope and process variations. Such a systematic approach is suitable to be part of the library characterization process. Our simulation results on a $0.18\mu m$ CMOS process show the proposed approach has a percentage error from 2.2% to 12.9% and a standard deviation error from 2.2% to 12.5% for both static and dynamic gates. There are two trends that need to be pointed out here. One trend is that by including input slope, the HDMR models are significantly more accurate compared to the ones without including the input slope; and the other trend is the model error tends to increase with the increase in model complexity. Therefore, tradeoffs are needed to determine the number of parameters and the degree of their cooperativity to be included in the HDMR models.

One potential drawback of the proposed approach is the amount of SPICE simulations required during the library characterization process. Given the complexity of the proposed model of $O(n^2)$, where n is the number of sample points. One can trade run time of library cell characterization with model accuracy by reducing the number of samples on the cut line and relying more on interpolation. However, this amount of SPICE simulations is a one-time occurrence during library characterization.

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TABLE V

STANDARD DEVIATION ERROR OF GATE DELAY FOR DYNAMIC LOGIC

	Model with RSAT, w/o slope and Leff	Model with RSAT, slope and Leff
C1	68.0	6.37
C2	36.4	5.0
C3	55.7	3.3
C4	43.9	7.3
C5	35.3	6.03
C6	24.0	8.51
C7	46.12	8.33
C8	32.7	8.06
C9	39.02	6.45
C10	52.67	12.5
C11	40.81	11.7
C12	68.5	9.00

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