Power-Constrained Test Scheduling for Multi-Clock Domain SoCs

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Abstract

This paper presents a wrapper and test access mechanism design for multi-clock domain SoCs that consists of cores with different clock frequencies during test. We also propose a test scheduling algorithm for multi-clock domain SoCs to minimize test time under power constraint. In the proposed method, we use virtual TAM to solve the frequency gaps between cores and the ATE, and also to reduce power consumption of a core during test while maintaining the test time of the core. Experimental results show the effectiveness of our method not only for multi-clock domain SoCs, but also for single-clock domain SoCs with power constraints.
keywords: *multi-clock domain SoC, test scheduling, test access mechanism, power consumption*

1 Introduction

The systems-on-chip (SoC) design strategies help us to reduce the time-to-market and design cost for new products significantly. However, testing of SoC is a crucial and time consuming problem due to the increasing design complexity[1]. Therefore, the goal is to develop techniques for wrapper design, test access mechanism (TAM) design and test schedule that minimizes test application time under given constraints such as the number of test pins and power consumption. A number of approaches have addressed wrapper design [2, 3, 4] which are IEEE 1500 [5] compliant. Similarly, several TAM architectures have been proposed such as *TestBus* [6, 7], *TESTRAIL* [8], *transparency based TAM* [9, 10, 11]. Moreover, many approaches for test scheduling problem have been proposed [12, 13, 14, 15, 16, 17].

However, these previous approaches are applicable only to single-clock domain SoCs that consist of embedded cores working at the same clock frequency during test. Today's SoC designs in telecommunications, networking and digital signal processing applications consist of embedded cores working with different clock frequencies. The clock frequency of some embedded cores during test is limited by its scan chain frequencies. On the other hand, other cores may be testable at-speed in order to increase the coverage of non-modeled and performance-related defects. The at-speed testable cores might be non-scan designed sequential circuits and require functional vectors or ordered test sequence at the rated clock frequency. Moreover, there also exists a frequency gap between each embedded core and ATE used to test the SoC. From these facts, we conclude that the previous approaches have the following two problems: 1) in the case when test clock frequency of a core is higher than that of ATE, the ATE cannot provide test sequences at the same speed of the test clock frequency of the core, and 2) in the case when test clock frequency of a core is lower than that of ATE, testing of the core by lowering the frequency of ATE does not make use of ATE capability effectively. Therefore, it is necessary to develop a technique that can solve the above problems for the multi-clock domain SoCs.

Recently, virtual TAM based on bandwidth matching [18] has been proposed in [19] to increase ATE capability when the clock frequency of a core is lower than that of ATE. Xu et al. extended the virtual TAM technique to the multi-frequency TAM design to reduce the test time for the single-clock domain SoCs in [22]. Moreover, a wrapper design for cores with multiple clock domains was proposed in [20, 21] to achieve at-speed testing of the cores by using virtual TAM technique. However, the test scheduling problem for the multi clock domain SoCs is not addressed in these literatures.

To the best of our knowledge, this paper gives a first discussion and a formulation of the test scheduling problem for multi-clock domain SoCs. We present a wrapper and TAM design for multi-clock domain SoCs and propose a test scheduling algorithm to minimize test time under power constraint. In the proposed method, we use virtual TAM for each core to solve a frequency gap between each core and a given ATE while the approach in [22] uses a virtual TAM for each test bus (i.e., all the cores assigned to the same test bus must be tested at the same frequency). Therefore, the proposed method in this paper has more flexibility for the test scheduling. Moreover, we also use virtual TAM in order to reduce the power consumption of the cores during test. Therefore, the proposed method is effective for the power-constrained test scheduling. Experimental results show the effectiveness of our method not only for multi-clock domain SoCs, but also for single-clock domain SoCs with power constraints.

The rest of this paper is organized as follows. We discuss multi-clock domain SoCs in Section 2. Section 3 shows a power-conscious virtual TAM technique. After formulating

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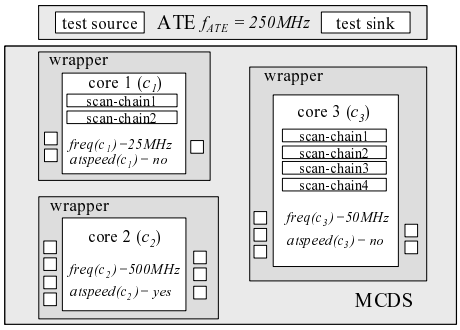

Figure 1. Multi-clock domain SoC.

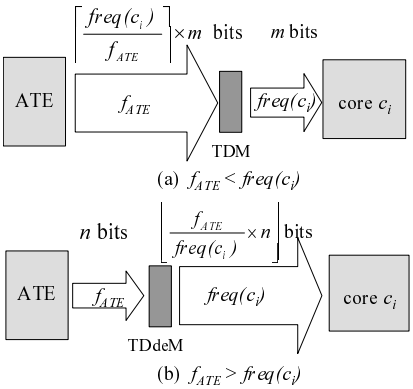

Figure 2. Test data multiplexing/de-multiplexing.

a test scheduling problem for multi-clock domain SoCs in Section 4, we present a power-constrained test scheduling algorithm in Section 5. Experimental results are discussed in Section 6. Finally, Section 7 concludes this paper.

2 Multi-Clock Domain SoCs

This section describes the formal notation we use to model the multi-clock domain SoC under test. An example of an SoC is shown in Figure 1 where each core is wrapped to ease test access. Test pattern source and test response sink are implemented off-chip as an ATE. The SoC can be modeled as a multi-clock domain SoC, $MCDS = (C, R, P_{max})$, where:

$C = \{c_1, c_2, ..., c_n\}$ is a set of cores;

Each core c_i is characterized by:

- $freq(c_i)$: maximum test frequency of core $c_i \in C$;
- $power(c_i)$: power consumption of core $c_i \in C$ at test frequency $freq(c_i)$;
- $atspeed$: $C \rightarrow \{yes, no\}$: at-speed test requirement

$R = \{R_1, R_2, ..., R_n\}$ is a set of wrapper lists;

Each wrapper list R_i is characterized by:

- $R_i = \{r_{i1}, r_{i2}, ..., r_{ij}\}$ is a set of wrapper designs for core c_i;
- Each wrapper design r_{ij} is characterized by:
  - $pin(r_{ij})$: number of pins to test core c_i with j-th wrapper design ;
  - $cycle(r_{ij})$: number of clock cycles to test core c_i with j-th wrapper design;

P_{max}: maximum allowed power at any time;

We consider that an SoC consists of the maximum allowed power consumption and cores working at different test frequencies. However, we assume that each core has been designed with single-clock domain during test. For each core, a maximum test frequency and a power consumption at the given maximum frequency are given. Each core also has an information about the requirement of at-speed testing. $atspeed(c_i) = yes$ means that c_i must operate at $freq(c_i)$ during test (i.e., we cannot change the test frequency of c_i for test scheduling). $atspeed(c_i) = no$ means that c_i can be tested at lower frequencies than $freq(c_i)$ (i.e., we can decrease the test frequency of c_i for test scheduling). Moreover, each core has a wrapper list that consists of possible wrapper designs for the core. Each wrapper design has a number of test pins and a number of clock cycles required to test the core with the wrapper design. The test time for c_i working at $freq(c_i)$ can be calculated as $cycle(c_i)$ / $freq(c_i)$.

3 Virtual TAM for Power Minimization

The frequency gaps between ATE and cores can be solved by using virtual TAM techniques based on bandwidth matching. When $freq(c_i)$ (clock frequency of core c_i during test) is higher than f_{ATE} (clock frequency of ATE) (Fig. 2(a)), we insert a TDM (test data multiplexing) circuit between ATE outputs and the core inputs, and multiplex $\lceil freq(c_i)/f_{ATE} \rceil \cdot m$ TAM wires at f_{ATE} into m virtual TAM wires at $freq(c_i)$. On the other hand, when $freq(c_i)$ is lower than f_{ATE} (Fig. 2(b)), we insert a TDdeM(test data de-multiplexing) circuit between ATE output and the core inputs, and de-multiplex n TAM wires at f_{ATE} into $\lfloor n \cdot f_{ATE}/freq(c_i) \rfloor$ virtual TAM wire at $freq(c_i)$. To observe test responses, we need to insert TDM/TDdeM between the core output and ATE inputs in the similar fashion.

In this paper, we also utilize virtual TAM technique to reduce power consumption of a core while maintaining the same test time of the core. The dynamic power $P(k)$ (which is the dominant source of power consumption in CMOS circuits) consumed in the circuit on application of consecutive two test vectors (V_{k-1}, V_k) is as follows [23].

$$P(k) = 1/2 \cdot f \cdot V_{DD}^2 \cdot \sum C_i \cdot S_i(k) \quad (1)$$

Here, f is the clock frequency, V_{DD} is the power supply voltage, C_i is the output capacitance at node i and $S_i(k)$ is the number of switchings provoked by V_k at node i. From the equation(1), we observe that the power consumption of a core during test can be reduced by lowering its test frequency. However, this increases test time of the core proportionally to the power reduction ratio. Here, we insert TDdeM circuit between the ATE outputs and the core inputs. Then, more virtual TAM wires become available for the core, and test time can be reduced. In the best case, we can achieve the same test time with 50% reduction of power consumption for a core by using the above power-conscious virtual TAM technique. For example, we consider the wrap-

Table 1. Power-conscious virtual TAM for core7 in d695.

frequency(MHz)	# virtual TAM wires	test time(μs)	# cycles
50	10	264.86	13243
25	20	268.68	6717

per design for core7 in d695 from ITC'02 SoC benchmarks [24]. Table 1 shows that we can achieve a 50% power reduction with an 1.4% test time overhead by decreasing the frequency from 50MHz to 25MHz and increasing the number of virtual TAM wires from 10 to 20.

4 Problem Formulation

We formulate the power-constrained test scheduling problem for multi-clock domain SoCs P_{mcds} that we address in this paper as follows.

Definition 1 P_{mcds}: Given a multi-clock domain SoC $MCDS$, the number of available test pins W_{max} and the clock frequency of ATE f_{ATE}, is there a test schedule for $MCDS$ that satisfies all the following conditions?

1. the total number of test pins used at any moment does not exceed W_{max},
2. the total power consumption used at any moment does not exceed P_{max},
3. each core satisfies at-speed test requirement (i.e., if $atspeed(c_i) = yes$, c_i must be tested at $freq(c_i)$. Otherwise, c_i can be tested at frequencies lower than $freq(c_i)$),
4. the overall SoC test time is minimized

If there is such a test schedule, determine a wrapper design and test frequency of each core for the test schedule.

5 Scheduling Algorithm

This section presents a heuristic algorithm for P_{mcds} that consists of the following three stages: 1) testability analysis, 2) test scheduling at time 0 for cores with large amount of test data, and 3) test scheduling based on Best Fit Decreasing (BFD) heuristic [25] for remaining cores. The example of the generated test schedule is shown in Figure 3. The shaded cores and the unshaded cores in Figure 3 are scheduled in stage 2 and stage 3, respectively. The following subsections describe the details of each stage.

5.1 Testability Analysis (Stage 1)

If $MCDS$ cannot satisfy the following two conditions for the given parameters: f_{ATE} and W_{max}, then there is no solution for P_{mcds}.

For each $c_i \in C$ such that $atspeed(c_i) = yes$,

[power limitation]

$$P_{max} \geq power(c_i) \tag{2}$$

[pin limitation]

$$W_{max} \geq \min_j(pin(r_{ij})) \cdot \lceil freq(c_i)/f_{ATE} \rceil \tag{3}$$

For a core c_i such that $atspeed(c_i) = yes$, we cannot change the test frequency $freq(c_i)$ and power consumption $power(c_i)$ during test. Therefore, the core that cannot satisfy equation(2) exceeds a given power limitation even if it is tested alone. Moreover, as explained before, TDM/TDdeM circuits can be uniquely determined when f_{ATE}, a wrapper design r_{ij} and a test frequency for c_i are given. Therefore, the core that doesn't satisfy equation(3) cannot be assigned enough wrapper pins to achieve at-speed test at $freq(c_i)$.

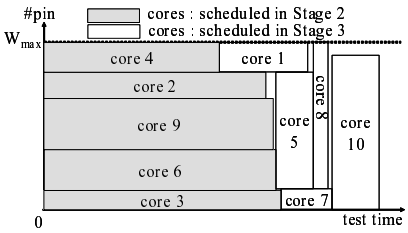

Figure 3. A test schedule example.

5.2 Test scheduling at time 0 with minimum test frequency (Stage 2)

This stage consists of the following three steps.

Step 1: *determine a wrapper design and test frequency for each core*

Main idea in this step is to increase test concurrency for power-constrained test scheduling by lowering the test frequencies of cores which do not require at-speed test. For each core c_i, we determine a wrapper design r_i^{test} and a multiplicity m_{c_i} such that

1. $T_{LB} \geq cycle(r_i^{test})/(freq(c_i)/m_{c_i})$,
2. $pin(r_i^{test}) \leq W_{max} \cdot f_{ATE}/(freq(c_i)/m_{c_i})$,
3. $pin(r_i^{test})$ is maximized, and
4. m_{c_i} is maximized.

Here, lower bound T_{LB} on the SoC test time is defined as follows.

$$T_{LB} = \max\{\max_i(T_{LB}^{c_i}), TotalData/(W_{max} \cdot f_{ATE})\} \tag{4}$$

Lower bound $T_{LB}^{c_i}$ on the core test time and $TotalDate$ are defined as follows.

$$T_{LB}^{c_i} = cycle(r_{ij})/freq(c_i) \text{ s.t.}$$
$$1.\ pin(r_{ij}) \text{ is maximized, and}$$
$$2.\ pin(r_{ij}) \leq W_{max} \cdot f_{ATE}/freq(c_i). \tag{5}$$

$$TotalData = \sum_i pin(r_{ij}) \cdot cycle(r_{ij}) \text{ s.t.}$$
$$pin(r_{ij}) \text{ is minimized.} \tag{6}$$

Then, we determine test frequency $f_{c_i}^{test}$ for c_i as follows.

$$f_{c_i}^{test} = \begin{cases} freq(c_i)/m_{c_i} & \text{if } atspeed(c_i) = no \\ freq(c_i) & \text{if } atspeed(c_i) = yes \end{cases} \tag{7}$$

Step 2: *determine cores which start their tests at time 0*

First, we sort cores in the descending order based on its $T_{LB}^{c_i}$. Then, we schedule a core c_i in the above order at time 0 with wrapper r_i^{test} and test frequency $f_{c_i}^{test}$. This process repeats until 1) the power consumption at time 0 (P_0) does not exceed P_{max}, 2) the pin usage at time 0 (W_0) does not

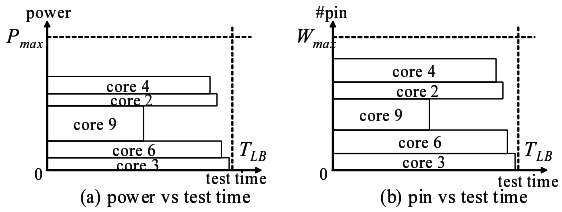

Figure 4. Test schedule after Step 2.

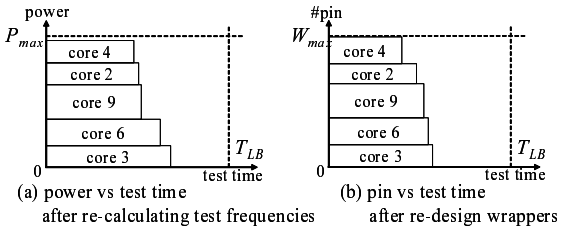

Figure 5. Test schedule after Step 3.

exceed W_{max}, and 3) $T_{LB}^{c_i}$ is less than $T_{LB}/|C|$. Here, $|C|$ denotes the number of cores in the SoC. The third condition can prevent us from scheduling cores with small amount of test data to time 0. Instead of scheduling such small cores at time 0, Step 3 re-designs wrappers and re-calculates test frequencies for the cores scheduled in this step to reduce the overall test time of the SoC.

Figure 4 shows a current test schedule generated after Step 2. In Figure 4(a), the horizontal axis denotes the test time, and the vertical axis denotes the power consumption used in each test time. In Figure 4(b), the horizontal axis denotes the test time, and the vertical axis denotes the number of test pin used in each test time.

Step 3: *re-calculate test frequencies and re-design wrappers for cores scheduled at time 0*

There exists a case where P_0 (power consumption at time 0) does not reach P_{max} after Step 2 (Fig. 4(a)) since Step 2 stops the above three conditions. In this case, we find a core c_i that satisfies all the following conditions.

1. $cycle(r_i^{test})/f_{c_i}^{test}$ is maximized (8)
2. $m_{c_i} > 1$ (9)
3. $P_{max} \geq P_0 - power(c_i)\{1/m_{c_i} + 1/(m_{c_i} - 1)\}$ (10)
4. $P_{max}/2 \geq power(c_i)/(m_{c_i} - 1)$ (11)

If there exists such a core c_i, we update m_{c_i} to $m_{c_i} - 1$, and reduce the test time of c_i by increasing $f_{c_i}^{test}$ according to equation (7). The fourth condition (equation(11)) can prevent one core from dominating power consumption, and help us to increase the test concurrency at time 0. This process repeats until 1) P_0 does not exceed P_{max} and 2) there exists a core that satisfies the above conditions. Figure 5(a) shows a result where we apply this process to the current schedule generated after Step 2 corresponds to Figure 4. In this figure, frequencies for core 2, 3, 4 and 6 are increased. Consequently, the test time for these cores are reduced.

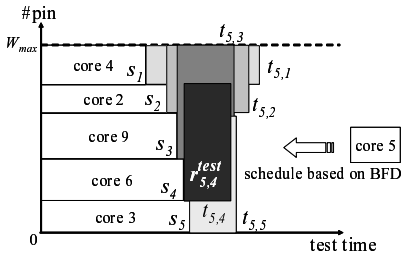

Figure 6. An example of test scheduling for core 5.

Similarly, there exists a case where W_0 (pin usage at time 0) does not reach W_{max} after Step 2. In this case, we find a core c_i with maximum test time, then assign 1 test pin to c_i. This process repeats until W_0 does not exceed W_{max}. Figure 5(b) shows a result where we apply this process to the current schedule corresponding to Figure 5(a).

5.3 Test scheduling for remaining cores based on BFD (Stage 3)

In this stage, we determine a test schedule for the remaining cores based on BFD heuristic. First, we pick a core c_i in the descending order based on $T_{LB}^{c_i}$. Then, we find the best start time, wrapper design and test frequency for c_i such that the total test time of the given SoC is minimized as follows.

1. Let S be a set of start time candidates that consists of the end time of scheduled cores in the current schedule. For each candidate $s \in S$, we calculate available power consumption P_s and available test pin W_s from the current schedule.
2. For each candidate $s \in S$,
   (a) Determine a maximum test frequency $f_{c_i,s}^{test}$ such that $power(c_i) \cdot f_{c_i,s}^{test}/freq(c_i)$ does not exceed P_s.
   (b) Determine a wrapper design $r_{i,s}^{test}$ such that 1) $pin(r_{i,s}^{test})$ does not exceed $W_s \cdot f_{ATE}/f_{c_i,s}^{test}$ and 2) $pin(r_{i,s}^{test})$ is maximized.
   (c) Calculate the end time $t_{i,s}$ when c_i starts its test at time s with wrapper $r_{i,s}^{test}$ at frequency $f_{c_i,s}^{test}$.
3. Schedule c_i at time s with wrapper $r_{i,s}^{test}$ at frequency $f_{c_i,s}^{test}$ such that 1) $t_{i,s}$ is minimized and 2) the test of c_i does not overlap the tests of cores already scheduled in the current schedule.

Figure 6 shows an example of the test scheduling for core 5. Here, a set of start time candidates S consists of five elements: s_1, s_2, s_3, s_4, s_5. For each candidate $s \in S$, we calculate a end time $t_{5,s}$ by determining a test frequency $f_{c_5,s}^{test}$ and a wrapper design $r_{5,s}^{test}$ shown as a rectangle in Figure 6. In this example, core 5 is scheduled to start its test at time s_4 with a wrapper $r_{5,4}^{test}$ at frequency $f_{c_5,4}^{test}$ since the end time $t_{5,4}$ has a minimum value.

This process repeats until all the remaining cores are scheduled in the descending order based on $T_{LB}^{c_i}$. Through the above processes, we can generate a final test schedule.

6 Experimental Results

In Section 6.1, we show experimental results for a multi-clock domain SoC with power constraint. Section 6.2 presents experimental results for single-clock domain SoCs with power constraint ("d695" and "h953" from ITC'02 SoC benchmarks [24]) in order to show the effectiveness of our approach compared to previous works. All the experimental results can be obtained within 0.1 sec. on a SunBlade 2000 workstation (1.05 GHz with 8GB RAM).

6.1 Results for a multi-clock domain SoC

Since there exists no approach that has tackled the test scheduling problem for multi-clock domain SoCs, it is difficult to compare with previous works. We have decided to analyze the trade-offs of the proposed method in terms of the number of available test pin, the clock frequency of ATE, maximum allowed power consumption and test time for a hypothetical multi-clock domain SoC. Table 2 shows the multi-clock domain SoC $MCDS_1$ used in this experiment. This SoC consists of 14 cores. First 10 cores are from "d695" in ITC'02 SoC benchmarks. "flexible(≥ 2)" in column "wrapper list" denotes that we can design any wrapper (wrapper with any number of test pins) by the procedure proposed in [2, 3]. We use the same power consumption shown in [15], and assume that $freq(c_i) = 50$ MHz and $atspeed(c_i) = no$ for these 10 cores. The wrappers for core 11 and core 12 are already designed (i.e., 64 pins, 32 pins, respectively). We assume that these two cores are tested at higher frequencies than other cores, and $atspeed(c_i) = yes$. Core 13 and core 14 are copies of core 7 and core 5, respectively. However, we assume that these two cores are tested at lower frequencies than other cores.

For this SoC, Table 3 shows test time results when f_{ATE} = 200MHz, 100MHz and 50MHz. In this table, the test time results are shown as "μsec.", and "untestable" denotes that there exists no solution for the given parameters. In this SoC, since core 11 should be tested at 100MHz with 64 pins, we observe that there exists no solution for three cases: 1) f_{ATE} = 100MHz and W_{max} = 32, 2)f_{ATE} = 50MHz and W_{max} = 32, and 3) f_{ATE} = 50MHz and W_{max} = 64. We also observe that test time depends on the product of f_{ATE} and W_{max}. Therefore, when we use a high speed ATE, we can test SoCs with small number of test pins. On the other hand, even when we use a low speed ATE, we can achieve the same test time by using more test pins. From this results, the designer can decide the number of test pins and the speed of the test pin considering the total cost for them.

6.2 Comparison with other approaches

The proposed test data de-multiplexing technique is also effective for the power-constrained test scheduling of the single-clock domain SoCs as well as for that of the multi-clock domain SoCs. In order to show the effectiveness of our approach compared to previous works, we present experimental results for the single-clock domain SoCs with power constraint. We use "d695" and "h953" from ITC'02 SoC benchmarks [24] as the single-clock domain SoCs by assuming that $f_{ATE} = 50$ MHz, and $freq(c_i) = 50$ MHz and $atspeed(c_i) = no$ for all core $c_i \in C$. This is because only these two SoCs have power information in the benchmarks (for "d695", we use the same power consumption shown in [15]). Table 4 shows the test time results of the proposed method and the previous power-constrained approaches [15, 16] which are applicable only to the single-clock domain SoCs. In this table, test time results are shown as the number of clock cycles. "NA" denotes that the approach is not applicable for the constraint. "-" denotes that no result is shown for the constraint in the approach. For d695, we observe that the proposed approach can achieve a 6.9% reduction in average test time compared to [15]. Moreover, for h953, we observe that the proposed approach can achieve the lower bound (119357) on the SoC test time [14] under all power constraints. From these results, we conclude that the proposed power-conscious virtual TAM technique and test scheduling algorithm are also effective for single-clock domain SoCs.

Table 2. An multi-clock domain SoC $MCDS_1$.

core	at-speed requirement	wrapper list (pins)	test freq. (MHz)	power (unit)
1	no	flexible(≥ 2)	50	660
2	no	flexible(≥ 2)	50	602
3	no	flexible(≥ 2)	50	823
4	no	flexible(≥ 2)	50	275
5	no	flexible(≥ 2)	50	690
6	no	flexible(≥ 2)	50	354
7	no	flexible(≥ 2)	50	530
8	no	flexible(≥ 2)	50	753
9	no	flexible(≥ 2)	50	641
10	no	flexible(≥ 2)	50	1144
11	yes	fixed (64)	100	480
12	yes	fixed (32)	200	940
13	no	flexible(≥ 2)	20	212
14	no	flexible(≥ 2)	25	345

7 Conclusions

This paper has presented a power-conscious wrapper and TAM design for multi-clock domain SoCs, and proposed a test scheduling algorithm to minimize test time under power constraint. To the best of our knowledge, a test scheduling problem for multi-clock domain SoCs has been addressed and formulated for the first time in this paper. Moreover, we have presented a technique to reduce power consumption of a core during test while maintaining the test time by utilizing virtual TAM technique which is applicable to both single and multi clock domain SoCs.

Acknowledgments

This work was supported in part by Japan Society for the Promotion of Science (JSPS) under Grants-in-Aid for Scientific Research B(2)(No. 15300018). The authors would like to thank Prof. Kewal K. Saluja, Michiko Inoue, Dr.

Table 3. Test time results [μs] for multi-clock domain SoC $MCDS_1$.

P_{max}	f_{ATE} = 200MHz			f_{ATE} = 100MHz			f_{ATE} = 50MHz		
	W_{max}			W_{max}			W_{max}		
	32 pin	64 pin	128 pin	32 pin	64 pin	128 pin	32 pin	64 pin	128 pin
1500	431.05	351.22	351.22	untestable	431.05	351.22	untestable	untestable	431.05
2000	325.29	278.55	278.55	untestable	325.29	278.55	untestable	untestable	325.29
2500	324.05	234.24	221.70	untestable	324.05	234.34	untestable	untestable	324.05

Table 4. Test time results (# cycles) for single-clock domain SoCs.

SoC	P_{max}	W_{max}								
		32 pin			64 pin			128 pin		
		3D[15]	EA[16]	proposed	3D[15]	EA[16]	proposed	3D[15]	EA[16]	proposed
d695	1000	NA	NA	**44528**	NA	NA	**27482**	NA	NA	**24707**
	1500	45560	-	**42981**	27573	-	**22690**	16841	-	**16239**
	2000	43221	-	**42632**	24171	-	**21838**	14128	-	**12753**
	2500	43221	-	**42564**	23721	-	**21616**	12993	-	**11180**
h953	5×10^9	NA	NA	**119357**	NA	NA	**119357**	NA	NA	**119357**
	6×10^9	122636	122636	**119357**	122636	122636	**119357**	122636	122636	**119357**
	7×10^9	**119357**	**119357**	**119357**	**119357**	**119357**	**119357**	**119357**	**119357**	**119357**

Satoshi Ohtake and members of Fujiwara Laboratory (Nara Institute of Science and Technology) for their valuable comments.

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