Efficient Temperature-Dependent Symbolic Sensitivity Analysis and Symbolic Performance Evaluation in Analog Circuit Synthesis

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Abstract

We present a new methodology for fast analog circuit synthesis, based on the use of temperature-dependent symbolic sensitivity analysis and symbolic performance evaluation in synthesis loop. Fast sensitivity analysis achieved and performance estimation are based on element-coefficient diagrams (ECDs). Sensitivity and performance evaluation expressions are generated from ECDs at the same time which reduces overall runtime greatly. The experimental results demonstrate that the speed and convergence of analog synthesis are improved significantly.

1. Introduction

Sensitivity of an analog circuit is the mathematical measurement of variations in the performance metrics due to small perturbations of circuit parameter values, which plays a very important role in determining the critical design variables. Sensitivity analysis has been used extensively for performance driven layout synthesis. The methods which use SPICE iteratively to optimize circuits and calculate sensitivities are computationally expensive and limit the size of the circuit. It is important to develop a technique that can obtain sensitivity efficiently during each synthesis iteration process. We propose temperature-dependent symbolic sensitivity analysis and symbolic performance evaluation in synthesis loop which is introduced in the analog circuit synthesis framework to reduce the overall number of iterations and runtime. Both sensitivity calculation and circuit performance evaluation expressions are obtained from ECDs with a bottom-up differentiation of each coefficient graph [1]. We apply those pre-compiled expressions in circuit synthesis loop instead of introducing simulation tools like Spice, Ngspice or Spectre again and again to do calculation numerically.

2. Proposed Circuit Synthesis Approach

The proposed circuit synthesis environment is shown in Figure 1. Circuit topology and search range for each parameter value of the circuit are the inputs to the optimization engine. In this case simulated annealing is core algorithm used for optimization which generates a new set of parameter values. Optimization engine then pass those new set of parameter values to Ngspice (or other simulator) to perform operating point (OP) analysis and the small-signal values for all active devices generated by OP analysis are passed to the symbolic performance evaluator and the symbolic sensitivity evaluator. The symbolic performance evaluator processes the simulation data to obtain the values of the desired performance parameters. These parameters are passed to the cost function evaluator to evaluate the cost which is used by the optimization engine to determine the new device size in each iteration process of optimization. Meanwhile, the symbolic sensitivity evaluator updates the performance sensitivity values by pre-compiled expresses with respect to all active and passive devices based on small-signal values taken from Ngspice. It generates a sensitivity weight vector including each device in the circuit. The sensitivity weight of each parameter is proportional to its sensitivity value. For example, n variables in a circuit are described as $V\{V_1, V_2, ..., V_n\}$, symbolic sensitivity evaluator generates a sensitivity weight vector for all variables

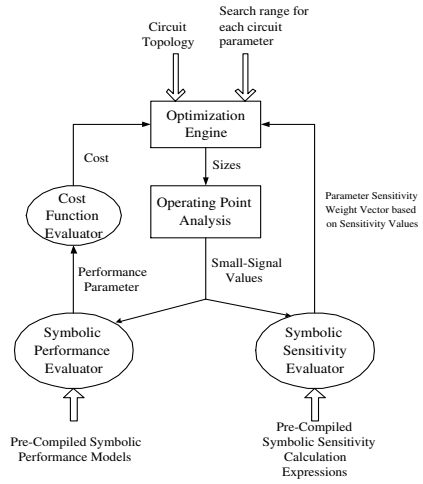

Figure 1. Proposed synthesis approach

according to their sensitivity values, which is described as $W\{W_1 * V_1, W_2 * V_2, ..., W_n * V_n\}$. W_i is proportional to the sensitivity value of V_i. The sensitivity weight vector is passed to optimization engine to update new set of parameter values. Instead of randomly choosing the parameter to be perturbed, the odds of devices being chosen for tuning are determined by this sensitivity weight vector in the optimization loop. In the different synthesis phases, the sensitivity weight vectors applied to determine the device to be tuned vary by multiplying a sensitivity rate. This process is repeated until the desired performance goals are achieved.

2.1. Symbolic performance evaluator

Symbolic performance evaluator is used to estimate analog circuit performance and represented by symbolic expressions obtained from symbolic transfer functions (represented by ECDs). In analog circuit synthesis, symbolic performance evaluator is used for repetitive performance estimation during the optimization iterations. Symbolic performance evaluator is different from numerical simulators which introduce simulation and analysis in every iteration process. This results in a significant speedup of the performance estimation time.

2.2. Temperature-dependent symbolic sensitivity methodology

Simulated annealing based optimization engine determines device sizes in each iteration process of the optimization loop. The core of temperature-dependent symbolic sensitivity methodology is to assign various sensitivity weight vectors in different annealing procedure based on the temperature. In high temperature phase, we assign large sensitivity weights on the devices with high sensitivity values and small weights on those devices with low sensitivity values. In other words, the device with high sensitivity value has high possibility to be chosen for tuning in next sizing iteration. In moderate temperature phase, we lower the sensitivity weights of the devices with high sensitivity values and increase the weights of the devices with low sensitivity values. In low temperature phase, we disable weight vector based on sensitivity analysis and choose the device to be tuned randomly.

3. Analog circuit synthesis Implementation

The algorithm was implemented and synthesis experiments were performed on three benchmark circuits. The first and second benchmarks are two stage opamp with different parameters. The third one (Single-ended opamp) is the device model of CMOS operational amplifier. For all performance specifications only gain has been observed for simplified purpose. Table 1 gives an account of the number of transistors, capacitors and resistors included in the benchmark circuits. Table 2 presents the speedup of iteration and runtime results between traditional method and proposed methodology. In Table 2, WS stands for the traditional synthesis process without sensitivity analysis and PS is the proposed synthesis with temperature-dependent sensitivity analysis. From Table 2 we can see that the average iteration speedup for three benchmark circuits is around 27% because of the application of temperature-dependent sensitivity analysis. Symbolic performance evaluation only can reduce the total runtime which cannot increase or decrease the total iterations. The results show that the average runtime is 59.5% which reduces greatly by using symbolic performance evaluation and temperature-dependent sensitivity analysis.

Circuit Name	MOS(#) (#)	C (#)	R (#)	ECD Vertices(#)	ECD Edges(#)
TSO1	6	2	0	352	1193
TSO2	9	0	1	770	4453
SEO	9	1	0	406	1982

Table 1. ECD Sizes of Benchmark Circuits

Circuit Name	Perf. Spec.	Iterations WS/PS	Iteration Speedup	Runtime(s) WS/PS	Runtime Speedup
TSO1	gain$\geq$ 40	714/510	28.57%	306/121	60.5%
TSO2	gain$\geq$50	1481/1063	28.2%	636/255	59.9%
SEO	gain $\geq$45	624/471	24.5%	270/113	58.1%

Table 2. Iteration and Runtime Comparison without/with Temperature-Dependent Sensitivity Synthesis Method

4. Conclusions

We proposed a new methodology for temperature-dependent symbolic sensitivity in analog synthesis. Pre-compiled symbolic performance evaluation and sensitivity calculation expressions are generated at the same time which reduces runtime greatly. The use of symbolic performance evaluation and temperature-dependent symbolic sensitivity analysis speeds up the synthesis process significantly and the overall synthesis speed is faster by 58%-60%.

References

[1] H. Yang, M. Ranjan, W. Verhaegen, M. Ding, R. Vemuri, and G. Gielen. Efficient symbolic sensitivity analysis of analog circuits using element-coefficient diagrams. *ASPDAC05*, pages 230–235, January 2005.