

Arbitrary Design of High Order Noise Transfer Function for A Novel Class of Reduced-Sample-Rate Sigma-Delta-Pipeline ADCs

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Abstract

A novel noise transfer function (NTF) for high order reduced-sample-rate sigma-delta-pipeline (SDP) ADCs is presented. The proposed NTF determines the location of the non-zero poles improving the stabilization of the loop and implementing the reduced-sample-rate structure, concurrently. A design methodology based on simulated-annealing-algorithm is developed to design the optimum NTF. To verify the usefulness of the proposed NTF and design procedure, two different modulators are presented. Simulation results show that with a 4th order modulator, designed making use of the proposed approach, the maximum SNDR of 115dB and 124.1dB can be achieved with only OSR of 8, and 16 respectively.

1. Introduction

Sigma-delta converters rely on high over sampling ratios to achieve high resolution and more relaxed analog circuit requirements. Hence the extending of these converters to high-speed applications requires reducing the OSR which results in degrading the dynamic range (DR) of the converter. The loss in the modulator performance due to reduction of the OSR can be compensated by increasing the order of the modulator noise shaping, keeping in mind the stability considerations, or increasing the resolution of the internal quantizer at the cost of the nonlinearity of the multibit feedback DAC. Another introduced way to cancel this effect is to use high-resolution quantizer in the cascaded forward path instead of the feedback path. The well-known architecture of this family is the cascaded SDP topologies. The cascaded SDP ADCs which appeared earlier in [1], and [2], are based on same noise cancellation principle with MASH ADCs. These works combine the high speed and noise shaping property of the pipeline and sigma-delta converters respectively and simultaneously. The structures proposed in [1] requires a multibit quantizer, operating at the full over sampling speed which makes it power hungry to implement. Based on successive decimation strategy, a sigma-delta ADC with reduced sample rate multibit quantizer has been proposed in [2], which N-fold decimates the output word stream of the Mth

-order modulator with an Mth-order sinc filter. Based on the rotated sinc (RS) filter introduced in [3], a modified reduced sample rate structure has been proposed in [4] which eliminates the SNR loss inherent in [2]. But it also noted that the reduced-sample-rate architecture can not realize modulators with none zero poles due to stabilization issue of the first stage.

In this paper we propose an efficient SDP ADC architecture employing a novel high-order noise transfer function with none zero poles which could stabilize the loop and realize reduced-sample-rate architecture, concurrently. The proposed NTF utilizes the novel pole-zero locations instead of conventional ones such as Butterworth or Chebyshev. Hence it is not possible to use conventional design toolboxes such as Schreier toolbox [5]. In order to overcome this problem a toolbox based on the simulated-annealing algorithm is developed to design the optimum NTF. Since making use of high order modulators in low OSR (e.g. OSR=4) designs are inefficient, we have focused our work on low to medium OSRs such as OSR=8~16. The rest of the paper is organized as follows: Section 2 describes the novel noise transfer function and NTF design methodology. In section 3 two design examples and simulation results are considered, section 4 discusses about the analog circuit requirements and finally section 5 contains the conclusions.

2. Proposed NTF and Design Methodology

2. 1. Proposed NTF

As demonstrated in [4] the reduced sample rate architecture can not realize the modulators with non-zero poles stabilizing the loop. Our proposed method introduces a high order IIR NTF with non-zero poles helping to stabilize the modulator and realizes the RSR architecture simultaneously; it is enough to locate the poles of the NTF such that the denominator of the NTF is only a function of z^N where N is the folding ratio in the first stage of the decimation filter. Since we have focused on low OSR (8~16) designs, the low folding ratio such as N=2 is a good candidate for the first stage of the decimation filter. Based on these assumptions the proposed IIR NTF and the first stage of the RS decimation filter can be written as follows:

$$NTF(z) = \frac{(1 - 2\cos(\alpha_1)z^{-1} + z^{-2})(1 - 2\cos(\alpha_2)z^{-1} + z^{-2})}{1 + \beta_2^2 z^{-2} + \beta_4^2 z^{-4}} \quad (1)$$

$$H_{dec}(z) = \frac{(1 - 2\cos(2\alpha_1)z^{-2} + z^{-4})(1 - 2\cos(2\alpha_2)z^{-2} + z^{-4})}{(1 - 2\cos(\alpha_1)z^{-1} + z^{-2})(1 - 2\cos(\alpha_2)z^{-1} + z^{-2})} \quad (2)$$

Where α_1 and α_2 determine the position of the zeros, β_2^2 and β_4^2 are determine by the locations of the poles with the following relations:

$$\beta_2^2 = d_1^2 + d_2^2, \quad \beta_4^2 = d_1^2 \times d_2^2 \quad (3)$$

The two possible pole-zero locations for the proposed NTF is shown in Fig. 1. Making use of Fig. 1 (a) leads to some higher out of band gain for NTF in comparison with Fig. 1 (b). This is because in the former case the high frequency poles are closer to the unit circle than the second one. Hence the pole-zero location of Fig. 1 (b) is chosen. The main specification of the proposed NTF is the higher out of band gain in comparison with conventional ones such as Butterworth's or Chebyshev pole locations. Hence if sufficient stability criterions are provided, it results in a stable and aggressive noise shaping NTF with large SNDR.

The main problem that that should be addressed, is how to place the poles of the NTF so that the SNR is maximized while that the system dos not goes to unstable and overload state. In multibit systems, it is possible to prevent to overload the quantizer by ensuring that the input signal plus the accumulation of the quantization noise does not

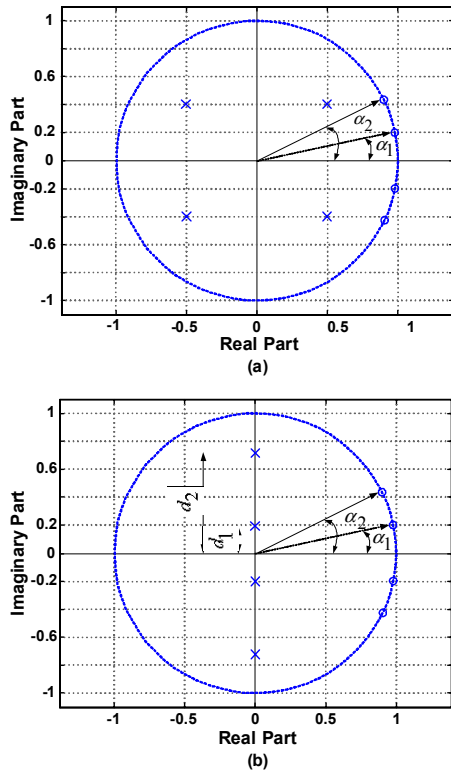


Fig. 1. Two possible pole-zero location of the proposed NTF.

exceed the full scale range of the modulator. An overload criterion based on the l_1 norm of the NTF[6] is used to place the poles of the NTF by minimizing the inband quantization noise and guaranteeing the stability. Making use of the additive white noise source model:

$$V(z) = STF(z) \cdot U(z) + \{NTF(z)-1\} \cdot E(z) \quad (4)$$

Where $V(z)$ is the z-domain expression of the quantizer input signal, $U(z)$ the z-domain expression of the input signal, $STF(z)$ the signal transfer function, $NTF(z)$ the noise transfer function and $E(z)$ the quantization noise. In low-distortion architectures, STF is unity, independent of the NTF characteristics. Since $ntf(0)=1$, the time domain expression for (4) can be written as follows:

$$v(n) = u(n) + \sum_{j=1}^{\infty} ntf(j) \cdot e(n-j) \quad (5)$$

Where account for the time-domain convolution. In a B-bit quantizer with reference voltage of V_{ref} , the worst case quantization error is characterized as follow:

$$\forall n \quad |e(n-j)| \leq \frac{\Delta}{2} = \frac{V_{ref}}{2^{B+1}} \quad (6)$$

Thus:

$$\begin{aligned} |v(n)| &\leq |u(n)| + \left| \sum_{j=1}^{\infty} ntf(j) \cdot e(n-j) \right| \\ &\leq |u(n)| + \frac{\Delta}{2} \sum_{j=1}^{\infty} |ntf(j)| \end{aligned} \quad (7)$$

The quantizer is not overloaded at the time n if $|v(n)| < V_{ref}$. Hence the following condition is sufficient to guarantees the stability of the modulator:

$$\begin{aligned} \frac{\Delta}{2} \sum_{j=1}^{\infty} |ntf(j)| &\leq V_{ref} - \|u\|_{\infty} \\ \frac{\Delta}{2} \{ \|ntf(n)\|_1 - 1 \} &\leq V_{ref} - \|u\|_{\infty} \end{aligned} \quad (8)$$

Where $\|ntf\|_1$ represents the l_1 norm of the NTF which accounts for the fraction of the dynamic range of the B-bit quantizer, dedicated to accumulation of the quantization noise. The modulator NTF not only has to meet the condition in (8), but also it should minimize the power of the inband quantization noise at the modulator output. The noise power is:

$$P_{er} = \int_0^{\pi/OSR} |NTF(e^{j\omega})|^2 \cdot \frac{\Delta^2}{12} d\omega \quad (9)$$

Where $\Delta^2/12$ accounts for the uniformly distributed power spectral density of the quantization noise. In higher order $NTFs$ usually it is not possible to derive a closed form solution for (9). Therefore numerical integration can be used to evaluate the inband noise power. It is clear from (8) that the maximum allowable peak-to-peak input signal range of the modulator is:

$$\|u\|_{\infty} \leq V_{ref} - \frac{\Delta}{2} \{ \|ntf(n)\|_1 - 1 \} \quad (10)$$

The maximum SNR excluding the circuit thermal noise can be expressed as follows:

$$SNR = \frac{\|u\|_{\infty}^2}{(2\sqrt{2})^2 \cdot P_{er}} \quad (11)$$

Equations (9), (10), and the reciprocal of the SNR in (11) will be used in a nonlinear multivariable optimization procedure to determine the optimum pole-zero locations of the proposed NTF .

2. 2. Design Methodology

In lower order $NTFs$ (e.g. second and third order) closed form solutions can be derived to achieve the optimum performance. But unfortunately there is no closed form solutions in higher order cases such as the one introduced in this work. In order to satisfy the design specification described above, a nonlinear optimization toolbox is developed in MATLAB making use of the optimization algorithm known as Simulated-Annealing (SA) [7]. The SA algorithm which has been adopted from the process of annealing of metals is a method for solving optimization problems where the minimum of a function of many variables is desired. This algorithm, whose flowchart is given in Fig. 2, works by first finding an initial temperature. Then the value of the cost function, the reciprocal of the calculated SNR in (11), is evaluated for a directed random set of input variables (here d_1 , d_2 , α_1 , and α_2). It is compared with the previous value. If it is smaller, the new set of data is accepted; otherwise it is accepted or rejected based on a probability function. The set of data is accepted if the following is satisfied:

$$Rand(0,1) < \exp\left(\frac{Old\ cost - New\ cost}{Temp}\right) \quad (12)$$

The SA algorithm has a parameter $Temp$ which is the cooling temperature of the metal. In (12) the higher the temperature is, the acceptance probability of the data increases. With decreasing temperature, this probability decreases. This causes the algorithm to have a ‘‘hill climbing’’ property and it does not get stuck in local minima. It has been proven in [7] that the SA algorithm has a very high chance of finding the global minimum. To start the following parameters must be determined: initial temperature, scaling factor of temperature at each iteration, range of input variables, neighborhood size of input variables, scaling factor of neighborhood size, and markov chain length. The procedure to determine the initial temperature is as follows: First an initial temperature is chosen, and then with 50 sets of random input variables the cost function is calculated. If all 50 sets are accepted, then the initial temperature is finalized. Otherwise the initial temperature is incremented. If the increment is too low then it will take a long time to find the initial temperature. On the other hand, a large increment causes the time to reach the final result to increase. The last issue is the stopping criterion. Here the optimization algorithm is stopped when the cost function evaluates to the same number to

two decimal places. Simulation results show that the developed procedure has a good convergence property and converges to same value for design parameters in several hundred runs of methodology. Table. 1 shows the optimum design parameters of a 4th-order NTF with $OSR=8$, and 16, designed by the SA algorithm. These parameters have been used in the next section to realize the modulator in system level.

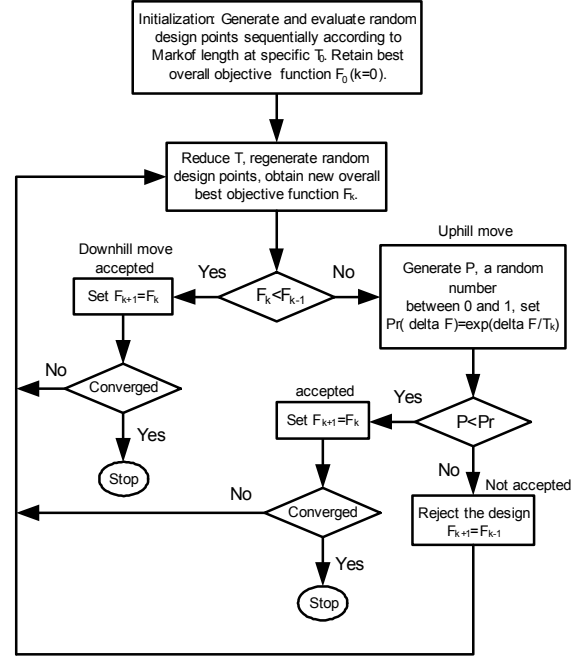


Fig. 2. Flowchart of the Simulated-Annealing algorithm.

Table. 1. Optimum coefficients of the 4th order NTF designed by SA.

4 th order NTF with $OSR=8$				4 th order NTF with $OSR=16$			
α_1	α_2	d_1	d_2	α_1	α_2	d_1	d_2
0.16	0.39	0.13	0.72	0.04	0.18	0.06	0.72

3. Design Examples

Fig. 3 shows the proposed ADC architecture. The first stage consists of a 4th order modulator with a 4-bit internal flash quantizer. The second stage is a multibit quantizer (here a K -bit D-stage pipeline ADC). It processes the down-sampled version of the quantization noise of the first stage. The digital filters are designed such that the output of the ADC only consists of the fine and shaped quantization noise of the K -bit pipeline ADC. The 4th order loop filter has been realized with two biquad sections: the integrator based biquad at the front-end of the loop, and IIR filter, $H_{IIR}(z)$, instead of a conventional integrator based or resonator based biquad sections, at the back-end of the loop with the following transfer function:

$$H_{IIR}(z) = \frac{b_3 z^{-1} + b_4 z^{-2}}{1 - a_3 z^{-1} - a_4 z^{-2}} \quad (13)$$

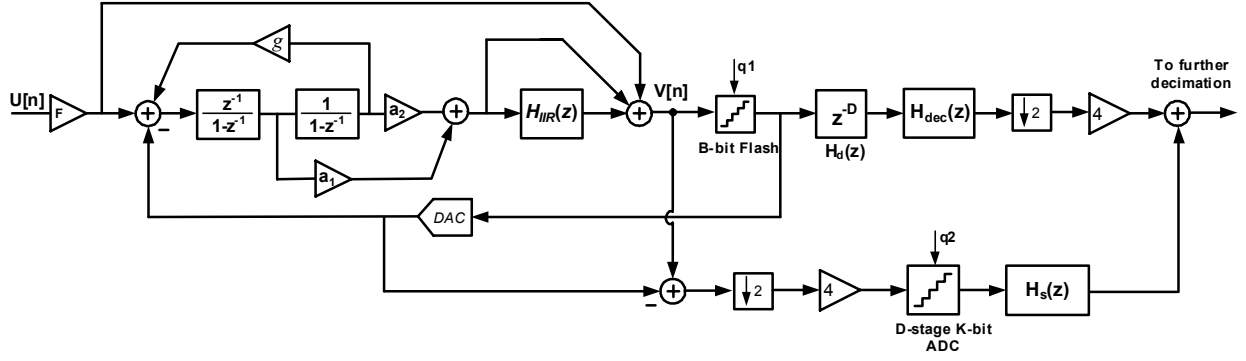


Fig. 3. Realization of the proposed NTF (B=4, and F=0.5).

As will be described in the next section, the transfer function of (13) can be realized with only a single OTA. The scaling factor of four has been used in the front of the K-bit ADC in order to recover the input signal of the ADC to the full-scale reference voltage. Additional delay element, $H_d(z)$, is inserted to compensate for latency of the D-stage pipeline ADC. The $H_{dec}(z)$ demonstrates the first stage of the RS decimation filter expressed in (2).

Since unity gain STF created by the forward path, is used to transfer the input signal independently of the loop filter, SNDR performance is not suffered from the phase nonlinearity of the IIR filter [8]. Unity gain STF not only reduces the harmonic distortion resulted from analog circuits imperfections, but also decreases the signal swing at the integrators and IIR block outputs. Hence it extends the stable input range of the modulator which results in an improved DR. Making use of the IIR block with a single OTA implementation that will be introduced in section (4), leads to a smaller feedback factor in the closed-loop amplifier. Therefore it is not recommended to use the IIR block in the front-end biquad section too, especially at high-speed applications. In the other hand, if the conventional implementation of the IIR filters [8] is used instead of the single OTA implementation employed in this work, it results in multiple feedback DAC and complex implementation especially if the linearization techniques such as Data-Weighted-Averaging (DWA) are used.

It can be easily shown that the NTF of the proposed architecture is as follows:

$$NTF = \frac{(1 - (2 - g)z^{-1} + z^{-2})(1 - a_3z^{-1} - a_4z^{-2})}{1 + \eta_1z^{-1} + \eta_2z^{-2} + \eta_3z^{-3} + \eta_4z^{-4}} \quad (14)$$

Where

$$\eta_1 = -2 + g + a_2 - a_3 + a_1 \quad (15)$$

$$\eta_2 = b_3a_2 - a_1 - a_4 + b_3a_1 - a_3g - a_3a_2 + 1 + 2a_3 - a_3a_1$$

$$\eta_3 = -b_3a_1 + a_3a_1 + b_4a_2 + b_4a_1 - a_4a_2 - a_4a_1 + 2a_4 - a_3 - a_4g$$

$$\eta_4 = -a_4 + a_4a_1 - b_4a_1$$

Comparing (14) with the equivalent one in (1) results in:

$$\eta_1 = \eta_3 = 0, a_4 = -1 \quad (16)$$

$$g = 2 - 2\cos(\alpha_1), a_3 = 2\cos(\alpha_2)$$

Hence parameters g , a_3 , η_2 , and η_4 can be obtained making use of optimum pole-zero location. The other remaining parameters are a_1 , a_2 , b_3 , and b_4 which can be obtained by solving the equation set (15) simultaneously.

In order to verify the usefulness of the proposed *NTF*, the design methodology, and proposed architecture two case studies are considered. The first one is a 4th-order modulator with OSR=16, 4-bit quantizer in the first stage, cascaded with a 6-bit ADC in the second stage. The second one is a 4th-order modulator with OSR=8, 4-bit quantizer in the first stage, cascaded with a 9-bit pipeline ADC in the second stage. The modulator coefficients for both OSR=8 and 16 are given in Table. 2. As it is shown the proposed architecture results in a small coefficients spread especially at lower OSRs which make it more suitable for high-resolution, high-speed with low OSR applications. The *NTFs* out of band gain of the designed modulators is about 20dB for both OSR=8 and 16 in comparison with 16 dB for a 4th-order modulator with OSR=16 proposed in [8]. As shown in Fig. 4 this results in more aggressive *NTF* at the cost of the some increase in *NTF* out of band gain. Fig. 5 represents the power spectral density of the proposed modulators in comparison with the 4th-order and 6th-order modulators proposed in [8] with ideal DAC unit elements. The resultant maximum SNDRs are about 115dB and 124.1dB in comparison with 103 dB and 100.5 dB for OSR=8, and 16 respectively. The cascaded architectures rely on the perfect matching between analog and digital noise transfer functions; this can be assured by using high precision analog building blocks, increasing the quantizer number of bits or digital calibration techniques which are implemented to adaptively tune the digital *NTF*

Table. 2. Modulator coefficients.

4 th order NTF with OSR=8						
g	a_1	a_2	b_3	b_4	a_1	a_2
0.15	1.974	-1	1.059	-0.387	1.617	2.207
4 th order NTF with OSR=16						
g	a_1	a_2	b_3	b_4	a_1	a_2
0.032	1.998	-1	1.049	-0.394	1.67	2.319

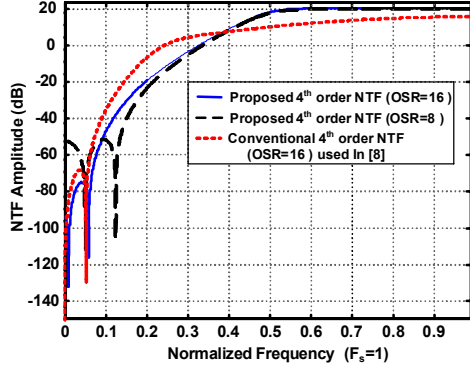


Fig. 4. NTFs of the proposed modulator for OSR=8, and 16.

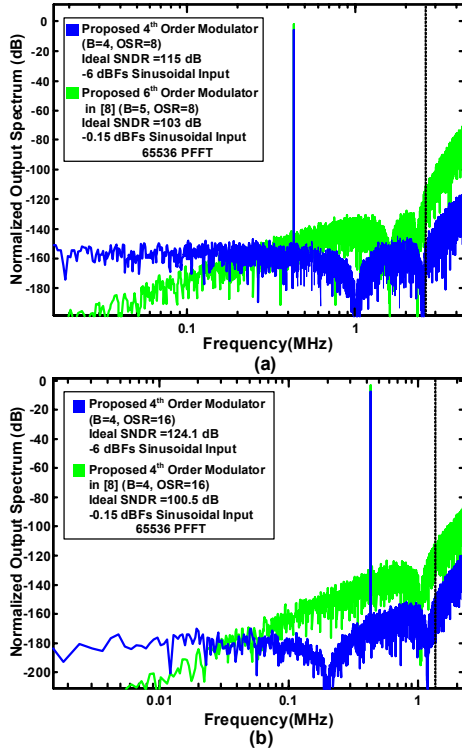


Fig. 5. Power spectral density of the proposed modulator (a) OSR=8, (b) OSR=16, dotted lines show the desired signal bandwidth.

coefficients to match the unknown analog *NTF* [9]. Since in the designed modulator a 4-bit quantizer is used in the first stage, the SNDR degradation due to the leakage of the 4-bit quantization noise is not very important. This fact is shown in Fig. 6. Simulation results show that with 0.4% mismatch in modulator coefficients that is well achievable in today's modern CMOS technologies, the SNDR degradation is only about 8dB and 12 dB with OSR=16 and 8 respectively. As we have expected the SNDR drop in OSR=16 is less than OSR=8. For this simulation the mismatch was considered as three times of the standard deviation of the Gaussian random distributed coefficients. For each mismatch value one hundred simulations were performed and the average SNDR was considered. One of the major circuit requirements is the amplifiers

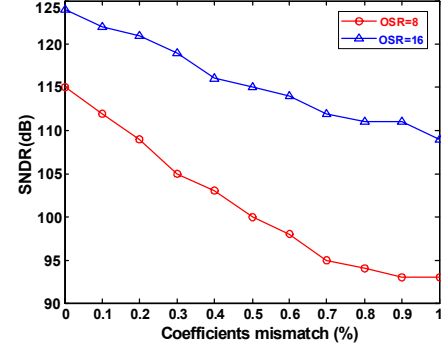


Fig. 6. SNDR versus mismatch in the modulator coefficients.

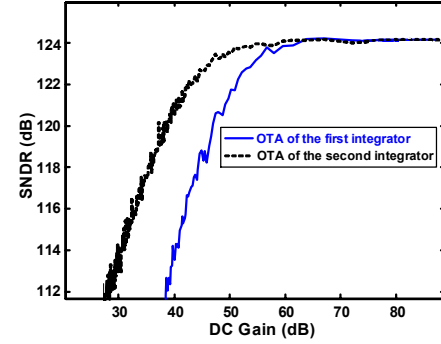


Fig. 7. SNDR versus DC gain of the OTA of the first and the second integrators.

DC gain. As shown in fig. 7 simulation results demonstrate that only 60 dB of DC gain in the OTA of the first integrator and 50 dB of DC gain in the OTA of the second integrator are sufficient to prevent degradation of the SNDR with enough margins. In multibit quantization the performance of the modulator is usually limited by the linearity of the DAC unit elements. Conventional linearization techniques such as DWA can be used to mitigate the performance degradation.

4. Analog Circuit Realization

The front-end biquad section of the loop filter consists of two integrators and can be realized making use of the conventional switched-capacitor integrators. The back-end biquad section with IIR transfer function can be realized making use of the conventional structures such as the one proposed in [8]. But conventional methods require at least two OTAs to implement a second order transfer function. Single OTA realization of the IIR filter can be achieved with some modifications in (13): $H_{IIR}(z)$ can be rearranged as follows:

$$H_{IIR}(z) = H_1(z) \cdot H_2(z) \quad (17)$$

$$= \frac{b_3 z^{-1}}{1 - a_3 z^{-1} - a_4 z^{-2}} \left(1 + \frac{b_4}{b_3} z^{-2} \right)$$

Where the second term, $H_2(z)$, can be mixed as a summation network in front of the quantizer. The first

one, $H_1(z)$, forms the feedback paths and denominator coefficients. Based on the work proposed in [10], $H_1(z)$ can be realized with only one OTA. Fig. 8 shows the single ended realization of the second order loop filter including the timing diagram. For simplicity non overlapping clock phases are not shown in timing diagram. The q path is realized by means of C_{f1} that samples the output of the OTA in F_1 and transfers the relative charge to the output in F_2 . The p path is realized with two paths capacitors, C_{f2} , sampling the OTA output alternately. While one capacitor samples the output in F_{S1} , the second one transfers $v_o(n-2)$ to the integrating capacitor, C_I , in F_{H2} and realizes the second order denominator. It can be easily shown that the structure presented in Fig. 8 realizes the following transfer function:

$$w(z) = \frac{C_s}{C_I} \frac{z^{-1}}{1 - \left(\frac{C_{f1} + C_I}{C_I} \right) z^{-1} + \left(\frac{C_{f2}}{C_I} \right) z^{-2}} \quad (18)$$

Comparing (18) and $H_1(z)$ in (17) results:

$$b_1 = \frac{C_s}{C_I}, a_3 = \frac{C_I + C_{f1}}{C_I}, a_4 = -\frac{C_{f2}}{C_I} \quad (19)$$

The main drawback of this technique is the capacitors mismatch in the p path moving the NTF zeros away from the unit circle and limiting the attenuation of the quantization noise. But since the error caused by this effect is shaped by the previous biquad section, the degradation of the modulator performance is negligible. The resulting system level simulations shown in Fig. 8 indicate that with 0.5% mismatch error in two paths, the SNDR degradation is less than 3.2 dB and 5 dB for OSR=16 and 8, respectively.

5. Conclusions

A RSR 4th-order sigma-delta-pipeline ADC architecture making use of a high-order NTF with a novel pole-zero location was presented. It determines the location of the non-zero poles improving the stability of the loop and implementing the reduced-sample-rate architecture, simultaneously. An NTF design methodology based on the l_1 norm criterion was developed in MATLAB to facilitate the design of the optimum NTF. Aggressive and yet stable NTF to achieve higher peak SNDR, and simplified analog circuit realization making use of a single OTA to realize the IIR transfer function, are the main advantages of the proposed architecture and NTF. System level simulations in MATLAB were used to verify the usefulness of the proposed architecture and NTF. Simulations results show that the SNDR of 115dB and 124.1dB can be achieved with only OSR of 8, and 16 respectively. It makes the proposed architecture suitable for high-resolution and medium to high-speed applications.

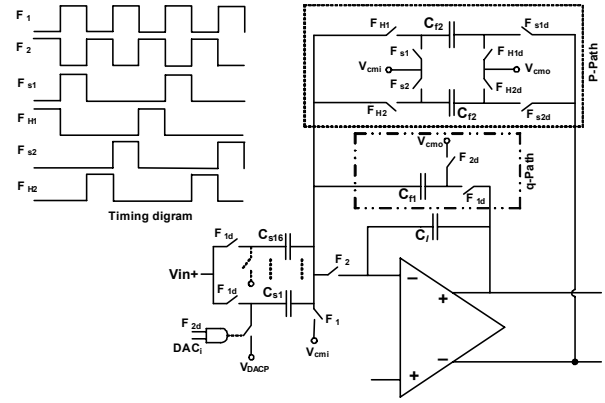


Fig. 8. Single OTA realization of the $H_1(z)$

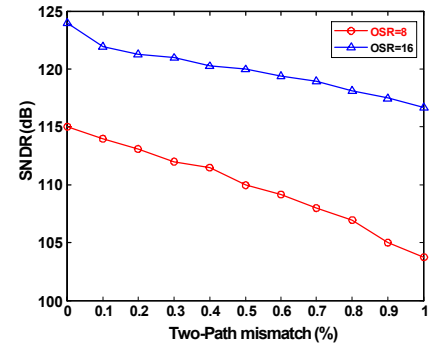


Fig. 9. SNDR versus two-path mismatch.

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