Large Scale RLC Circuit Analysis Using RLCG-MNA Formulation

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Abstract

A fast method for timing analysis of large scale RLC networks using the RLCG-MNA formulation, which provides good properties for fast matrix solvers, is presented. The proposed method is faster than INDUCTWISE and more general than the RLP algorithm, where INDUCTWISE and RLP algorithm are known as the state-of-art simulation methods. In the numerical example, good performances of the proposed method are illustrated compared with the previous works.

1. Introduction

Increasing clock speed and low resistance metal on high performance integrated circuits make on-chip inductance effects prominent. The interconnects in the integrated circuits are expressed by RLC circuits. Since the RLC circuits are extremely large scale, the timing simulations for evaluating the inductance effects waste huge CPU times.

It has been known that inverse inductance matrix is useful for large scale RLC network analysis. This concept is effectively realized on INDUCTWISE [2]. Recently, the RLP algorithm attains several ten times faster than INDUCTWISE utilizing the inverse capacitance matrix [3] rather than the inverse inductance matrix. However, the RLP algorithm is restricted to a special class of RLC networks.

In this paper, we present a fast simulation method using the RLCG-MNA formulation which provides good properties for fast matrix solvers. The proposed method can be applied to wider class of RLC circuits. Therefore, this method is more general than the RLP algorithm and faster than INDUCTWISE, which would allow us to built a fast simulator for large scale RLC networks.

2. Timing Analysis via RLCG-MNA Formulation

The idea of RLCG-MNA formulation to RLC circuits is related to how the resistors and inductors as a model of multi-conductor system are treated. In this formulation, KCL is not applied to nodes connecting resistors and inductors. Instead, the branches consisting of resistor and inductor are formulated by KVL. Then, the RLC circuits are expressed by

$$\mathcal{G}\boldsymbol{x}(t) + \mathcal{C}\frac{d}{dt}\boldsymbol{x}(t) = \boldsymbol{b}, \tag{1}$$

where

$$\boldsymbol{x}(t) = \begin{bmatrix} \boldsymbol{v}(t) \\ \boldsymbol{i}(t) \end{bmatrix}, \quad \boldsymbol{b} = \begin{bmatrix} \boldsymbol{I}(t) \\ \boldsymbol{0} \end{bmatrix},$$
$$\mathcal{G} = \begin{bmatrix} \boldsymbol{G} & \boldsymbol{A}^T \\ -\boldsymbol{A} & \boldsymbol{R} \end{bmatrix}, \quad \mathcal{C} = \begin{bmatrix} \boldsymbol{C} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{L} \end{bmatrix}.$$

$\boldsymbol{x}(t)$ is the circuit variable vector consisting of the node voltages $\boldsymbol{v}(t) \in \mathcal{R}^l$ and inductor currents $\boldsymbol{i}(t) \in \mathcal{R}^n$. $\boldsymbol{I}(t) \in \mathcal{R}^l$ is the independent current source vector. $\boldsymbol{G}, \boldsymbol{C} \in \mathcal{R}^{l\times l}$, $\boldsymbol{R}, \boldsymbol{L} \in \mathcal{R}^{n\times n}$ are the conductance, capacitance, resistance, and inductance matrices, respectively. $\boldsymbol{A} \in \mathcal{R}^{n\times l}$ is the incident matrix associated with the inductor branches. The RLCG-MNA formulation (1) provides more compact MNA equation than the original one which is used in INDUCTWISE [2] since the nodes connecting the resistors and inductors are not taken into account.

For the timing analysis of RLC networks, MNA equation is solved by using an implicit numerical integration method. The analysis at each time point is reduced to DC analysis. In INDUCTWISE, $\boldsymbol{L}^{-1}$ is used and the voltage vector at each time point is obtained by solving the nodal equation. In our method, the nodal analysis approach is also taken. Using the midpoint rule, we can write the update rule of voltages and

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	INDUCTWISE		RLCG		
elements	SCD	PCG	SCD	PCG	RLP
341	0.29	6.44	0.29	0.45	0.85
1281	1.08	26.58	0.49	0.96	2.36
4961	7.02	118.23	2.44	3	10.58
19521	104.4	632.88	24.16	22.27	48.91
77441	1910.18	4001.73	496.97	463.88	588.18

Table 1. Comparison of CPU times for a plane circuit analysis.

currents at a discrete time as

$$\left\{\boldsymbol{G}+\frac{2}{h}\boldsymbol{C}+\boldsymbol{A}^T\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\boldsymbol{A}\right\}\boldsymbol{v}^{k+1} = -\left\{\boldsymbol{G}-\frac{2}{h}\boldsymbol{C}+\boldsymbol{A}^T\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\boldsymbol{A}\right\}\boldsymbol{v}^k -\boldsymbol{A}^T\left\{\boldsymbol{I}-\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\left(\boldsymbol{R}-\frac{2}{h}\boldsymbol{L}\right)\right\}\boldsymbol{i}^k +\boldsymbol{I}^{k+1}+\boldsymbol{I}^k, \quad (2)$$

$$\boldsymbol{i}^{k+1} = -\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\left(\boldsymbol{R}-\frac{2}{h}\boldsymbol{L}\right)\boldsymbol{i}^k + \left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\boldsymbol{A}\left(\boldsymbol{v}^{k+1}+\boldsymbol{v}^k\right). \quad (3)$$

The coefficient matrix $\boldsymbol{G}+\frac{2}{h}\boldsymbol{C}+\boldsymbol{A}^T\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\boldsymbol{A}$ is corresponding to the nodal admittance matrix which is more compact than one used in INDUCTWISE. Therefore, our method is faster than INDUCTWISE. Furthermore, the condition number of the nodal admittance matrix is better than one in INDUCTWISE. This means that if the preconditioning conjugate gradient method is introduced for solving (2), the convergence is more rapid than that of INDUCTWISE [2] in which this method is used.

The proposed method is applicable to wider class of RLC networks, since $\boldsymbol{G}+\frac{2}{h}\boldsymbol{C}+\boldsymbol{A}^T\left(\boldsymbol{R}+\frac{2}{h}\boldsymbol{L}\right)^{-1}\boldsymbol{A}$ is generally non-singular. On the other hand, the RLP algorithm is only applicable to the circuit with non-singular matrix $\boldsymbol{G}+\frac{2}{h}\boldsymbol{C}$ so that it is obviously restrictive. From this fact, the proposed method is more general than the RLP algorithm.

3. Example

The plane circuit which is corresponding to one layer of packaging system [4], was analyzed by the proposed method. The plane circuit is modeled by the passive RLC elements. Table 1 shows the comparison of CPU times. In this table, "INDUCTWISE" and "RLCG" indicate that the network is expressed by the original- and RLCG-MNA equations, respectively, and "elements" is corresponding to the numbers of total passive elements. "SCD" and "PCG" imply that the nodal equations for updating the voltage vectors at each time point are solved by the sparse Cholesky decomposition [2] and the preconditioning conjugate gradient method [1], respectively. "RLP" means the RLP algorithm [3]. The time step size is 10 [ps] except for the RLP algorithm. Since the RLP algorithm diverged using this time step, 1 [ps] was taken. The simulations were done by Matlab 7 on Federa Core 3, using Pentium 4 with 3 GHz clock and 1 GByte memory.

For the plane circuit composed of 10×10 cells, the ratios between maximum and minimum eigen values of the nodal admittance matrix are $\kappa = 1.780853 \times 10^{-6}$ for INDUCTWISE and $\kappa = 1.003195 \times 10^{-1}$ for the RLCG-MNA formulation. This means that the condition number of the nodal admittance matrix in (2) is better than one in INDUCTWISE. Therefore, it is considered that the preconditioning conjugate gradient method incorporated with the solution of (2) converges more quickly than INDUCTWISE as shown in Tab. 1. When the sparse Cholesky decomposition is used, the CPU time is about four times faster than INDUCTWISE. The CPU times of the RLP algorithm are comparable to the proposed methods. However, it should be noted that the RLP algorithm is not only restricted by the circuit structures but also a stable time step size is unknown.

4. Conclusions

In this paper, a fast simulation method for the large scale RLCG network analysis has been proposed. This method is based on the RLCG-MNA formulation, where the RLCG-MNA formulation accelerates the speeds of matrix solvers. From the comparison with the state-of-art methods, the effectiveness of the proposed method has been illustrated.

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